

Self-consistent 30-band simulation approach for (non-)uniformly strained confined heterostructure tunnel field-effect transistors

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Abstract—Heterostructures of III-V materials under a mechanical strain are being actively researched to enhance the performance of the tunnel field-effect transistor (TFET). In scaled III-V device structures, however, the interplay between the effects of strain and quantum confinement on the semiconductor band structure and hence the performance is highly non-trivial. We have therefore developed a computationally efficient quantum mechanical simulator Pharos, which enables self-consistent full-zone $\mathbf{k}\cdot\mathbf{p}$ -based simulations of III-V TFETs under a general non-uniform strain. We present the self-consistent procedure and demonstrate it on confined staggered bandgap GaAs_{0.5}Sb_{0.5}/In_{0.53}Ga_{0.47}As TFETs. We find a large performance degradation due to size-induced quantum confinement compared to non-confined devices. We show that some performance can be regained either by applying a uniform biaxial tensile strain or through the non-uniform strain profile at a lattice-mismatched heterostructure.

I. INTRODUCTION

Thanks to the principle of band-to-band-tunneling (BTBT), the tunnel field-effect transistor (TFET) is capable of a subthermionic subthreshold swing (SS) and is therefore a promising successor to the metal-oxide-semiconductor field-effect transistor (MOSFET) for future low-voltage applications [1], [2], [3]. Unfortunately, TFET implementations in silicon suffer from insufficient drive currents due to the large Si bandgap at the tunnel junction, which decreases the tunneling probability. A higher tunneling probability can be achieved with a III-V heterostructure, because the band alignment of the two materials provides an extra degree of freedom to reduce the effective bandgap at the tunnel junction ($E_{g,\text{eff}}$). The range of available band alignments is limited, however, to existing and processable material combinations. The application of strain therefore provides an additional way to tune $E_{g,\text{eff}}$ [4], [5]. However, III-V structures exhibit significant quantum confinement as compared to Si configurations, also for larger body thicknesses (T_{body}). The interplay of the effects of confinement and strain on the band structure and electrostatic potential, and hence the TFET performance, is thereby highly non-trivial. This is especially the case for non-uniform strain profiles, in which the strain varies along the tunnel junction and throughout the device. Such non-uniform profiles are

present e.g. at a heterojunction between two materials with different lattice constants.

To predict the effects of various strain profiles on the performance of confined TFETs, a self-consistent quantum mechanical simulation approach that accurately captures the band structure is therefore desired. Existing quantum approaches for strained TFETs, however, are either not self-consistent [5], not full-zone [6], [4], [7], or have very large computational demands as T_{body} increases to 5 nm due to their atomistic nature [8]. We have therefore developed a computationally efficient self-consistent quantum simulator, called Pharos, which can calculate transport based on $\mathbf{k}\cdot\mathbf{p}$ band structure models that capture the full first Brillouin zone, including the effects of spin-orbit coupling. Pharos can be used to investigate strained heterostructure III-V TFETs with 2D potentials and a confined but not atomistic T_{body} .

In this paper, we first discuss the self-consistent procedure and then apply it to confined staggered bandgap heterostructure TFETs. Next, we investigate the possibility of improving the TFET performance by applying a uniform strain, or by switching to a lattice-mismatched material combination.

II. SELF-CONSISTENT PROCEDURE

The first part of the self-consistent procedure is the calculation of the free carrier densities in the device. The carrier densities are calculated based on the solutions of a 30-band spectral envelope function system with a position dependent $\mathbf{k}\cdot\mathbf{p}$ strain term [9]. The strain term enables the simulation of general non-uniform profiles. Quantum transmitting boundary conditions are imposed at the open source and drain contacts. Use of the spectral method for the confined direction enables to filter the spurious solutions of the full-zone model and greatly reduces the computational burden [10]. The envelope functions obtained from solving the system are first normalized and then used to calculate the free carrier densities by summing and integrating the probability density of the individual envelope functions F over all quantum numbers, weighted with the

appropriate Fermi-Dirac distribution. This can be expressed as follows:

$$p(\mathbf{r}) + n(\mathbf{r}) = \int_{k_x} dk_x \int_{k_y} dk_y \sum_{\gamma, N} |F_{N, k_x, k_y, \gamma}(\mathbf{r})|^2 f_{\text{inj}}(\Delta E_{\text{inj}}(k_x, k_y, \gamma)) \quad (1)$$

where x is the transport direction, z a confined direction and translational invariance is assumed in y . k_x and k_y are the wave numbers in x and y respectively. n (p) is the free electron (hole) charge density and f_{inj} is the Fermi-Dirac of electrons (holes) if the carrier is injected from the conduction (valence) band, with ΔE_{inj} the energy relative to the quasi-Fermi level in the contact of injection. The temperature is assumed to be 300 K. The indices γ, N run over all subband modes and bands respectively.

With the calculated free carrier densities from Eq. (1) and the known acceptor and donor concentrations in the device, Poisson's equation is then solved with Neumann boundary conditions at the open contacts to obtain a new electrostatic potential. For a stable loop with the carrier density calculation, we employ an adaptive Gummel scheme, combined with successive underrelaxation. In the Gummel scheme, one extra term is added at each side of Poisson's equation, which mixes the electrostatic potential of the previous (ϕ_{old}) and current (ϕ_{new}) iteration:

$$\begin{aligned} \nabla^2 \phi_{\text{new}}(\mathbf{r}) - \frac{q(p(\mathbf{r}) + n(\mathbf{r}))}{\epsilon V_{\text{ref}}} \phi_{\text{new}}(\mathbf{r}) \\ = -\frac{\rho(\mathbf{r})}{\epsilon} - \frac{q(p(\mathbf{r}) + n(\mathbf{r}))}{\epsilon V_{\text{ref}}} \phi_{\text{old}}(\mathbf{r}) \end{aligned} \quad (2)$$

with ϵ the semiconductor permittivity and ρ the total charge density:

$$\rho(\mathbf{r}) = q(p(\mathbf{r}) - n(\mathbf{r}) + N_{\text{D}}(\mathbf{r}) - N_{\text{A}}(\mathbf{r})) \quad (3)$$

with q the elementary charge and N_{A} (N_{D}) the acceptor (donor) concentration. V_{ref} is a damping parameter which can be tuned to increase or decrease the amount of damping in the self-consistent loop. To provide extra damping in case overshoot occurs, the Gummel scheme is complemented with successive underrelaxation:

$$\phi_{\text{new}}(\mathbf{r}) = \omega \phi_{\text{new}}(\mathbf{r}) + (1 - \omega) \phi_{\text{old}}(\mathbf{r}) \quad (4)$$

where ω is again a tuneable damping parameter. The full self-consistent procedure is summarized in Fig. 1.

In contrast to atomistic approaches, the continuum nature of the envelope functions allows to speed up the first few iterations by reducing the number of mesh points and then progressively refining the mesh. For the TFETs in this work, one iteration of the self-consistent loop takes around 1.5h on just ten cores of a state-of-the-art server, with an iteration count typically around five.

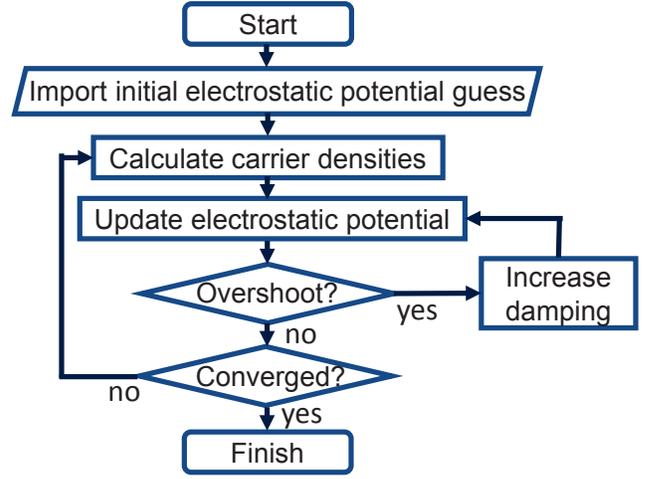


Fig. 1. Flowchart of the self-consistent procedure. The initial guess comes from a previous bias point if available, or a semi-classical electrostatic potential otherwise. Damping is increased by increasing ω and/or V_{ref} in Eqs. (2) and (4). Convergence is deemed achieved when the maximal value of the relative potential error between iterations is smaller than 0.01% throughout the device. For speed, the number of mesh points is halved as long as the residual remains above 0.05%.

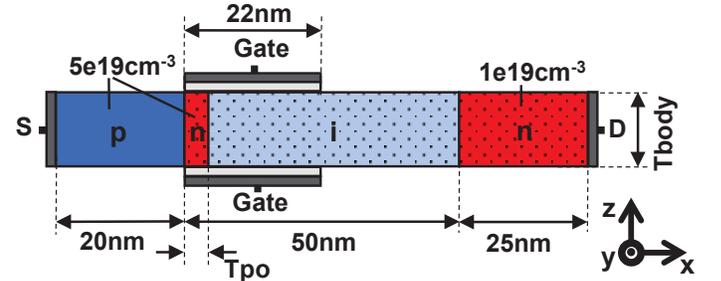


Fig. 2. Simulated TFET configuration. The solid and dotted regions indicate different materials. Dopant profiles are assumed to be uniform and abrupt. The gate stack has an equivalent oxide thickness of 0.6 nm and a metal workfunction of 4.5 eV. Translational symmetry is assumed in the y -direction. The mesh consists of 3500 x -points, 10 k_y -points, 3 spectral components and 500 adaptively chosen energy points.

III. APPLICATION TO III-V HETEROSTRUCTURE TFET

A. Unstrained

We now demonstrate our self-consistent procedure with staggered bandgap (GaAs_{0.5}Sb_{0.5} / In_{0.53}Ga_{0.47}As) TFETs with a confined T_{body} of 5 nm. The configuration details are shown in Fig. 2. 30-band $\mathbf{k}\cdot\mathbf{p}$ parameters for the simulated materials have been fitted to bandgaps and effective masses for the Γ -valley and bandgaps for the X- and L-valleys [11].

The transfer characteristics in Fig. 3 show a strong deterioration in performance compared to the 10 nm T_{body} case, with I_{60} , the highest I_{DS} at which SS is below 60 mV/dec, decreasing from $4 \times 10^{-1} \mu\text{A}/\mu\text{m}$ to $2 \times 10^{-2} \mu\text{A}/\mu\text{m}$ and I_{ON} decreasing from $5 \mu\text{A}/\mu\text{m}$ to $1 \mu\text{A}/\mu\text{m}$ for a V_{DD} -window of 0.3 V and an I_{OFF} of 10 pA/ μm . Since the source degeneracy remains similar to the 10 nm T_{body} case, the deterioration can be attributed to an increase in $E_{\text{g,eff}}$ at

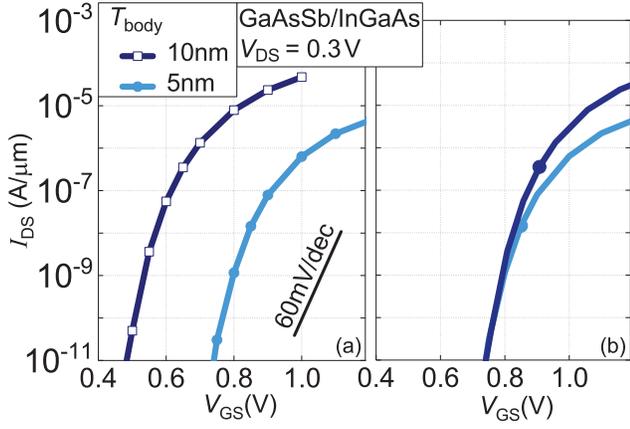


Fig. 3. Transfer characteristics of staggered gap p-i-n TFETs with varying T_{body} , self-consistent (5 nm) and non-self-consistent (10 nm). (a) Unshifted and (b) shifted curves such that V_{GS} at an I_{OFF} of 10 pA/ μm coincides. The dots indicate I_{60} , the highest I_{DS} at which SS is sub-60 mV/dec.

the tunnel junction of 0.21 eV due to size-induced quantum confinement. The increase in $E_{g,\text{eff}}$ significantly deteriorates the tunneling probability, which is reflected in the transfer characteristics.

B. Uniform strain

To improve the performance of the confined 5 nm T_{body} configuration, we apply 500 MPa of uniform biaxial tensile stress in the y and z -directions. The corresponding strain tensor is diagonal, the elements of which are calculated with Hooke's law for zinc blende crystals [12]. Biaxial tensile stress has been found in previous work to reduce $E_{g,\text{eff}}$ for this material system [5], and also here we see a reduction in $E_{g,\text{eff}}$ by 40 meV. As Fig. 4 shows, this results in roughly a doubling of I_{ON} to 2 $\mu\text{A}/\mu\text{m}$.

Important to notice is that the strain does not deteriorate the SS, contrary to findings for wider bodies and non-full-zone models [5], [7]. Fig. 5 shows that the interplay between strain and confinement results in only a marginal decrease in valence band DOS in the source. Because of the strong confinement, only one subband contributes significantly to the transport. The effect of the strain can be seen to be limited to a warping of the top of the subband. There is no band degeneracy splitting, which is a major source of the valence band DOS reduction in wider body configurations. An important consequence of the retention of the SS is that there is no need to implement a pocketed source design for this configuration, unlike for wider bodies [5].

C. Non-uniform strain

Since uniform strain is challenging to realize experimentally, our implementation also allows us to investigate the more realistic case of a lattice-mismatched heterostructure. The heterostructure under investigation (GaSb/In_{0.53}Ga_{0.47}As) has been selected in previous work [9] and exhibits a 3.7% lattice mismatch. The mismatch gives rise to a strongly non-uniform strain profile around the tunnel junction. These strain

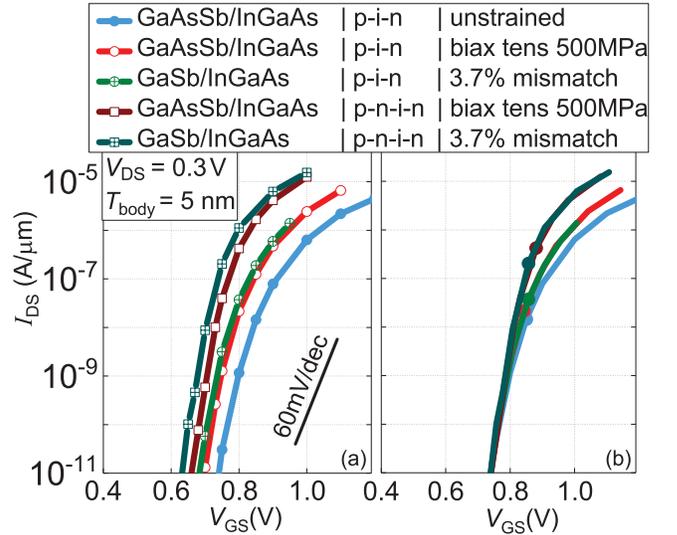


Fig. 4. Self-consistent transfer characteristics, comparing an unstrained staggered gap p-i-n TFET to uniformly strained and lattice-mismatched p-i-n and p-n-i-n configurations. T_{po} is 3 nm in the p-n-i-n TFETs. (a) Unshifted and (b) shifted curves such that V_{GS} at an I_{OFF} of 10 pA/ μm coincides in all curves. The dots indicate I_{60} .

profiles are calculated with finite-element based simulations in Synopsys Sentaurus Process [13], and are then imported into our quantum mechanical simulator Pharos through a position dependent strain term in the spectral envelope function system.

Fig. 4 shows that the non-uniform strain provides a similar performance gain as the uniform strain case. Again, the strain locally reduces $E_{g,\text{eff}}$ at the tunnel junction. Although the $E_{g,\text{eff}}$ reduction is non-uniform along the junction, it is on average similar as in the case of uniform strain.

D. Dopant pocket

Performance in both the uniform and non-uniformly strained cases can be further improved by inserting a 3 nm highly doped n-type pocket at the tunnel junction. The pocket locally enhances the electric field, which improves the tunneling probability [5]. Fig. 4 shows that as a result, I_{ON} increases to around 8 $\mu\text{A}/\mu\text{m}$, while I_{60} increases to around 2×10^{-1} $\mu\text{A}/\mu\text{m}$ for both the uniform and non-uniformly strained configurations. This is comparable to the unstrained 10 nm T_{body} configuration in Fig. 3, which does not have a dopant pocket.

IV. CONCLUSION

To conclude, we demonstrated a 30-band self-consistent procedure that enables the investigation of confined heterostructure TFETs under uniform and non-uniform strain. We illustrated for a 5 nm T_{body} staggered gap TFET that the performance is significantly degraded due to size-induced quantum confinement and that both uniform and non-uniform strain similarly improve the performance. In contrast to wider body devices, this performance improvement comes without a degeneracy-induced SS deterioration. Together with a dopant pocket, performance similar to an unpocketed, unstrained

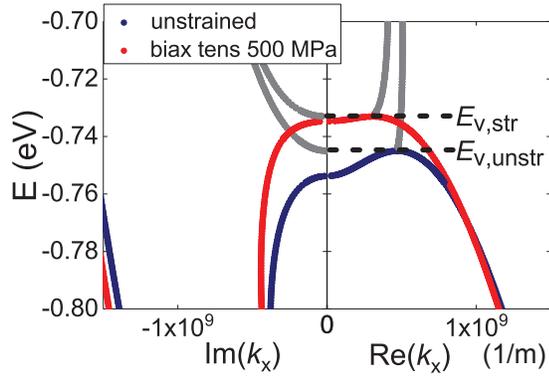


Fig. 5. Real (right) and imaginary (left) part of the first valence band subband of the 30-band $\mathbf{k}\cdot\mathbf{p}$ band structure for a T_{body} of 5 nm in unstrained $\text{Ga}_{0.5}\text{As}_{0.5}\text{Sb}$ and under biaxial tensile strain. The subbands show a similar DOS beyond 20 meV from the valence band edge ($E_{v,\text{str}}$ for the strained and $E_{v,\text{unstr}}$ for the unstrained case). In grey are the states with complex values of k_x .

10 nm T_{body} configuration could be obtained. This does show, however, that to retain the performance of the wider body configurations, confined staggered gap TFETs require a more complicated device structure, including performance boosters like strain and dopant pockets.

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REFERENCES

- [1] H. Lu and A. Seabaugh, "Tunnel field-effect transistors: State-of-the-art," *IEEE Journal of the Electron Devices Society*, vol. 2, no. 4, pp. 44–49, July 2014.
- [2] D. Verreck, G. Groeseneken, and A. Verhulst, *The Tunnel Field-Effect Transistor*. John Wiley & Sons, Inc., 2016, pp. 1–24.
- [3] U. Avci, D. Morris, and I. Young, "Tunnel field-effect transistors: Prospects and challenges," *IEEE Journal of the Electron Devices Society*, vol. 3, no. 3, pp. 88–95, May 2015.
- [4] S. Brocard, M. G. Pala, and D. Esseni, "Design options for hetero-junction tunnel FETs with high on current and steep sub-threshold voltage slope," in *2013 IEEE International Electron Devices Meeting (IEDM)*. IEEE, Dec. 2013, pp. 5.4.1–5.4.4.
- [5] D. Verreck, A. S. Verhulst, M. L. V. de Put, B. Sore, N. Collaert, A. Mocuta, A. Thean, and G. Groeseneken, "Uniform strain in heterostructure tunnel field-effect transistors," *IEEE Electron Device Letters*, vol. 37, no. 3, pp. 337–340, Mar. 2016.
- [6] F. Conzatti, M. G. Pala, D. Esseni, E. Bano, and L. Selmi, "Strain-induced performance improvements in InAs nanowire tunnel FETs," *IEEE Transactions on Electron Devices*, vol. 59, no. 8, pp. 2085–2092, Aug. 2012.
- [7] M. Visciarelli, E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, "Impact of strain on tunneling current and threshold voltage in III-V nanowire TFETs," *IEEE Electron Device Letters*, vol. 37, no. 5, pp. 560–563, May 2016.
- [8] R. Kotlyar, U. E. Avci, S. Cea, R. Rios, T. D. Linton, K. J. Kuhn, and I. A. Young, "Bandgap engineering of group IV materials for complementary n and p tunneling field effect transistors," *Applied Physics Letters*, vol. 102, no. 11, p. 113106, 2013.
- [9] D. Verreck, A. S. Verhulst, B. Sore, N. Collaert, A. Mocuta, A. Thean, and G. Groeseneken, "Non-uniform strain in lattice-mismatched heterostructure tunnel field-effect transistors," Sept. 2016, pp. 412–415.

- [10] D. Verreck, A. S. Verhulst, M. Van de Put, B. Sorée, W. Magnus, A. Mocuta, N. Collaert, A. Thean, and G. Groeseneken, "Full-zone spectral envelope function formalism for the optimization of line and point tunnel field-effect transistors," *Journal of Applied Physics*, vol. 118, no. 13, p. 134502, 2015.
- [11] M. Levinshtein, S. Rumyantsev, and M. Schur, *Handbook Series of Semiconductor Parameters*, 1999, vol. 1,2.
- [12] P. Yu and M. Cardona, *Fundamentals of Semiconductors*, 4th ed. Springer, 2010, ch. Appendix B, pp. 601–604.
- [13] Synopsys, *Sentaurus Process User Guide*, 2014.12.