DFT-based Analysis of the Origin of Traps at the InAs/Si (111) Interface

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***Abstract*— Trap-assisted tunneling is known to detrimentally affect the performance of TFETs. To find the origin of traps at the InAs/Si interface, Density Functional Theory (DFT) based modeling of the interface is performed using the DFT tool CP2K. Geometrically optimized atomic positions at the InAs/Si interface obtained by using structural minimization are in qualitative agreement with TEM images reported in the literature. Electronic structure calculations using the optimized atomic structure reveal highly localized trap states at the InAs/Si interface. The trap states originate from unsaturated atomic orbitals on As atoms and are primarily localized at As atoms.**

Keywords*— *InAs/Si hetero-junction, interface traps, density functional theory

I. Introduction

Tunnel Field Effect Transistors (TFETs) are considered as viable alternatives for MOSFETs in low-power electronic applications. Previous studies on InAs/Si hetero-junction TFETs have shown that traps at the InAs/Si interface degrade their performance and inhibit a sub-thermal slope [1]. The investigation into origin and nature of such interface traps using *ab-initio* atomistic modeling would be a useful first step in mitigating their detrimental impact.

In an earlier work, physics-based TCAD simulations of InAs/Si lateral nanowire TFETs (sketched in Fig. 1(a)) yielded good agreement with measured *IV*-data when the energy of the D_{it} peak was aligned with the valence band (VB) edge of InAs. Shifting the InAs/Si interface trap levels towards the conduction band (CB) edge results in a growing mismatch between experimental and simulated data as shown in Fig. 1(b). However, the I_D-V_{GS} plots barely change as long as the D_{it} peak stays in the lower half of the gap [2]. This suggests that the observed trap-assisted tunnel current originates from trap levels between VB edge and mid gap. In the present work, Density Functional Theory (DFT) based electronic structure calculations are performed to reveal the atomic structure at the InAs/Si interface. After geometrical optimization, the optimized structure was analyzed to find the origin of the localized states at the hetero-interface.

In the above TFET, an InAs nanowire was grown on Si (111) surface. This surface exhibits three types of reconstruction, viz. 1x1, 1x2, and 7x7 reconstruction [3]. Before the growth of InAs nanowires, the Si(111) substrate is dipped in Hydrogen Fluoride to etch the native oxide. This results in a hydrogen-passivated Si(111) surface [4]. Therefore, 1x1 reconstructed H-passivated Si(111) is most likely to be present during the growth phase and will be assumed to form the InAs/Si interface in this study.

This work was supported by the EU via FP7 project E2SWITCH under grant agreement No. 619509.

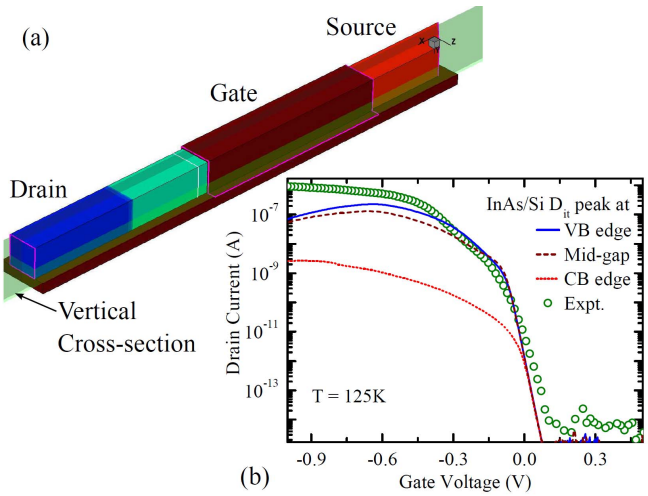

Figure 1: (a) Device structure of a lateral nanowire TFET (b) I_D-V_{GS} curves simulated with three different energetic positions of the D_{it} peak in the InAs gap. Figures taken from [2].

II. Simulation Set-up

Atomistic simulations were carried out using the mixed Gaussian-Plane-Wave (GPW) based DFT simulation package CP2K [5-7]. Perdew-Burke-Ernzerhof (PBE) pseudopotentials were used along with a double-zeta valence + one polarization (DZVP) basis set for In, As, and Si atoms for modeling the structure [8]. Structural minimization was performed on a InAs/Si slab which consists of a 4 monolayers (ML) thick InAs slab stacked over a 3 ML thick Si slab in growth direction (<111>). Periodic boundary conditions are used in the other two directions. The growth conditions had been tuned to create an InAs layer with As termination at the InAs/Si interface. Therefore, the InAs layer is assumed to be As-terminated. The open surfaces of the stacked slab in

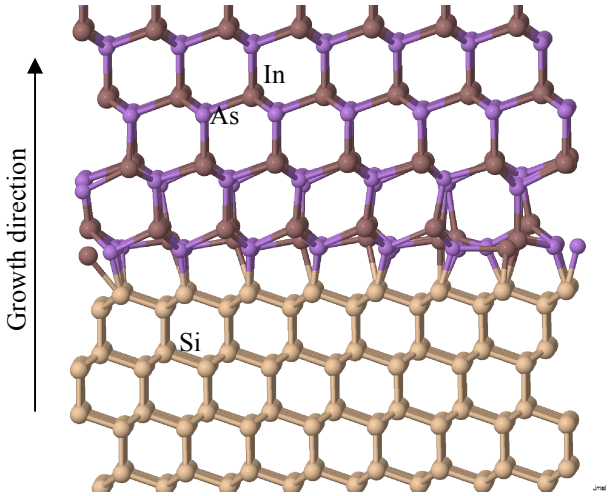

Fig. 2: Unit cell of the InAs/Si interface obtained by geometrical optimization of the first two layers of InAs.

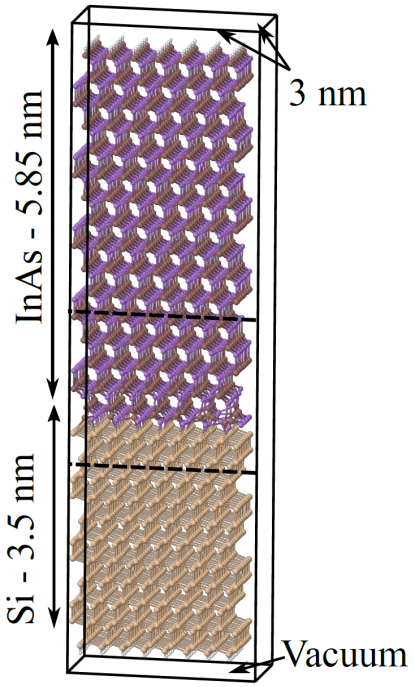

Figure 3: InAs/Si slab simulated to find interface trap levels. Note that the unit cell is periodic in the plane of the InAs/Si interface.

growth direction are padded with vacuum and passivated with Hydrogen. Both the InAs and Si slabs are assumed to be relaxed in the zinc-blende/diamond structure. The lattice constants of InAs and Si were set to 6.247 Å and 5.478 Å, respectively, after structural minimization of the unit cell of the individual elements. It can be shown that 7 unit cells of InAs in <110> direction are nearly lattice matched to 8 unit cells of Si. During structural minimization, all atoms except those of the first two monolayers of InAs adjacent to the InAs/Si interface were constrained. Since InAs is grown over a Si substrate, InAs atoms are not expected to alter the positions of Si atoms in the first monolayer. The root mean square (RMS) step as well as that of the RMS gradient and maximum gradient were set as convergence criteria. The convergence limits were the same as their default values in CP2K.

The positions of InAs atoms in the (110) plane after structural minimization are shown in Fig. 2(a). As mentioned earlier, 7 unit cells of InAs are nearly lattice-matched to 8 unit cells of Si. As seen in the figure, the first six unit cells of InAs at the interface are nearly intact after geometric optimization. A significant restructuring is observed at the last unit cell of InAs. Towards the left of the unit cell, Si atoms at the interface are nearly aligned with the As atoms. Due to the difference between the lattice constants of InAs and Si, the misalignment between Si atoms in the top layer and As atoms at the interface increases gradually towards left. Towards right of the unit cell, As atoms are maximally misaligned and therefore undergo a rearrangement to passivate the unsaturated orbitals. As a result, a discernible restructuring is observed at the right-end of the unit cell. Such structural rearrangement is observed periodically at the interface with the period of ~3 nm in InAs (110) plane. Filtered TEM images of the InAs/Si(111) interface reported in Ref. [9] show a region of high stress every ~3 nm in the (110) plane in agreement with the findings.

The material layers in a TFET are extremely thick i.e. bulk-like, and thus prohibitive for a DFT analysis. For the computation of the trap levels, the InAs and Si layers in the stacked slab were, therefore, clipped to 16 MLs and 11 MLs, respectively. The geometrically optimized structure was then used to model the InAs/Si interface in such a thick InAs/Si slab (shown in Fig. 2(b)). The top and bottom surfaces of the stacked slab were passivated with Hydrogen. This structure was simulated with CP2K to obtain the trap energy levels in the band gap of InAs. It is well-known that the PBE pseudopotentials do not open a band gap in bulk InAs and underestimate the gap in Si. For a more accurate band structure, a semi-empirical technique developed by Tao et al. (Tao-Perdew-Staroverov-Scuseria - TPSS) was used [10]. Fermi-Dirac smearing was activated, and the temperature was set to 300 K. Initially, the energy minimization was performed with PBE pseudopotentials to obtain the total wave function of the structure. This wave function was subsequently taken as initial guess to perform the energy minimization using the semi-empirical TPSS technique.

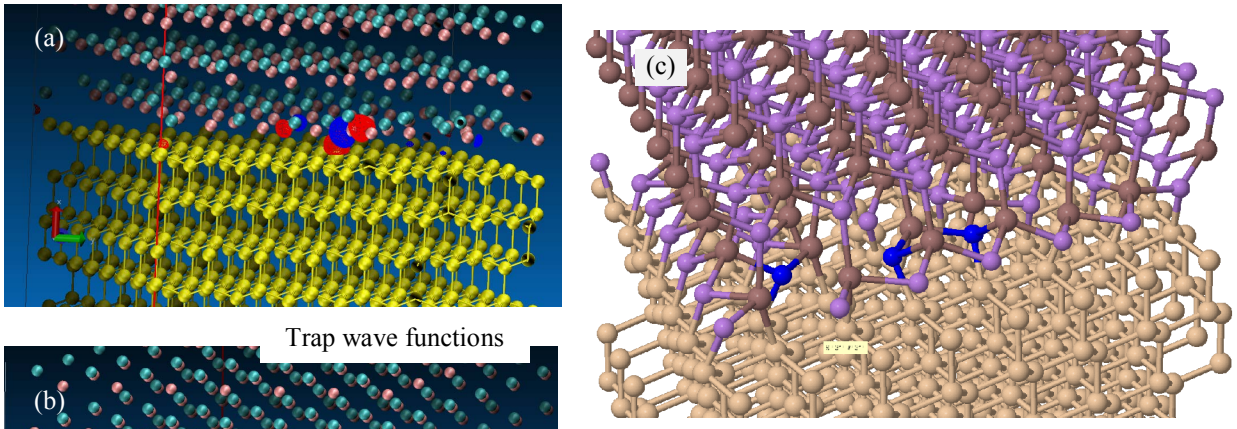

Figure 4: Contour representation of the wave functions of two representative trap levels at (a) E = -6.253 eV, (b) E = -6.135 eV. The trap wave functions are highly localized on As atoms at the interface (marked dark blue) shown in (c). Each of the As atoms has one unsaturated bonding orbital which creates the trap level.

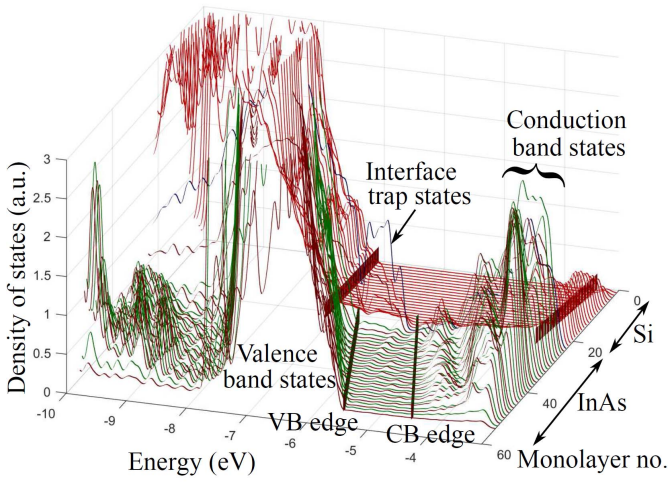

Figure 5: Ribbon plot of the aggregate atom-resolved DOS in each atomic plane of the InAs/Si slab along the z-axis.

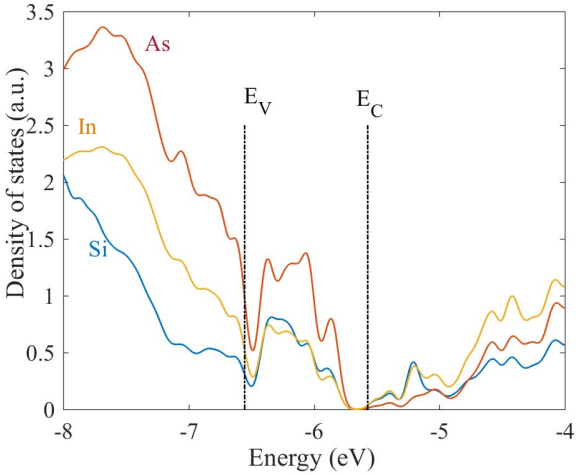

Figure 6: Aggregate DOS on Si, As, and In atomic layers at the interface. The plot shows that interface As atoms contribute most to the DOS of the trap levels adjacent to the VB.

III. Results and Discussion

The projection of the wave function of each energy level on spherical harmonics at each atomic position gives the atom-resolved DOS of that level. The atom-resolved DOS at each energy level and each atom was temperature-broadened with a Gaussian broadening (σ = 50 meV) and summed up to compute the energy-dependent DOS. The atom-resolved DOS of all atoms in each monolayer in the (111) plane was summed up and plotted as a ribbon plot in Fig. 3(a) vs. energy (In - brown, As - green, and Si - red). The ribbons are arranged in increasing order of the distance of the monolayer from the origin. The VB and CB states are seen in the InAs segment with a discernible band gap of ~1.1 eV due to quantum confinement (bulk value = 0.354 eV). Similarly, CB and VB states are separated in the Si slab by a band gap of ~3.5 eV. The strong increase compared to the experimental bulk value is due to both quantum confinement in <111> direction and the use of the semi-empirical TPSS technique which overestimates the gap of Si. The CB and VB edges of each ML are shifted linearly due to the electric field induced by the localized charges at the interface.

The blue ribbon representing the DOS on As atoms at the interface has an unusual shape with discernible trap levels present in the band gap of InAs, close to VB edge. The DOS on Si, As and In atomic layers at the InAs/Si interface are plotted in Fig. 4. The plot suggests that the trap levels at the interface are located close to the VB edge in the band gap of InAs. Also, As atoms contribute most to the DOS at each trap level. That is, the trap states close to the VB edge primarily originate from the As layer. Wave functions corresponding to two representative trap levels are shown as contour plots in Figs. 4(a) and 4(b). They are highly localized on certain As atoms marked blue in Fig. 4(c). As can be seen, all As atoms hosting a trap state have at least one unsaturated orbital. Examination of the wave functions of other trap levels reveals that all the trap states close to the VB edge are primarily localized at As atoms which carry one unsaturated orbital also called dangling bond. Thus, it may be inferred that unsaturated orbitals on As atoms at the interface give rise to the trap levels in the band gap of InAs, energetically located close to the valence band edge.

Shortcomings and assumptions made in the above DFT-based analysis must be noted. The lattice constants of Si and InAs used in the above analysis are slightly different from their experimental values. Had the experimental numbers been used, the relaxation of the interface after structural minimization using CP2K would have been caused by high hydrostatic strain, not by the misalignment. To avoid this, the lattice constants of individual materials were relaxed beforehand. With the new lattice constants, 7 unit cells of InAs are lattice-matched to 8 unit cells of Si. The calculation using experimental lattice parameters gives ~11% lattice mismatch, which implies 9 unit cells of InAs lattice-matched to 10 unit cells of Si. In the above analysis of defect formation at the interface, both InAs and Si slabs are assumed to be defect-free. However, the growth of a polar semiconductor such as InAs on a nonpolar substrate such as Si may result in the formation of antiphase domains. By tuning the growth conditions, a InAs nanowire can be grown from a single nucleation, and antiphase domains can be avoided.

IV. Conclusion

In summary, the relaxed InAs/Si interface was analyzed using a DFT simulation package. Structural minimization was performed on the InAs/Si slab to find the atomic arrangement at the interface. The geometrically optimized structure of the interface shows significant restructuring of InAs atoms every ~3 nm in qualitative agreement with filtered strain-mapping TEM images reported in the literature. Electronic structure calculations were performed on the structure to find the trap energy levels which are localized at the InAs/Si interface. The inspection of the wave functions of the trap levels suggests that the InAs/Si interface trap levels close to the VB edge originate from dangling bonds present on As atoms.

References:

[1] A. Schenk, S. Sant, K. Moselund, and H. Riel, "III-V-based Hetero Tunnel FETs: A Simulation Study with Focus on Non-ideality Effects", Proc. ULIS-EUROSOI 2016, pp. 9–12, 2016, doi: 10.1109/ULIS.2016.7440039.

[2] S. Sant, K. Moselund, D. Cutaia, H. Schmid, Mattias Borg, H. Riel, and A. Schenk, "Lateral InAs/Si p-type Tunnel FETs integrated on Si - Part 2: Simulation Study of the Impact of Interface Traps", IEEE Trans. Electron. Dev., vol. 63, p.4240, 2016.

[3] M. Hoegen, Surface and Interface Science: Properties of Elemental Surfaces, volume two, rst edition. Edited by Klaus Wandelt. Wiley-VCH Verlag GMBH, 815 (2012).

[4] G. S. Higashi, Y. J. Chabal, G. W. Trucks, and K. Raghavachari, “Ideal hydrogen termination of the Si(111) surface”, Appl. Phys. Lett., vol. 56, p. 656, 1990.
[5] CP2K version 5.0 (Development Version), the CP2K developers group (2016).
[6] G. Lippert, J. Hutter, and M. Parrinello, “A hybrid Gaussian and plane wave density functional scheme”, Molecular Physics, vol. 92, p. 477, 1997.
[7] J. Hutter, M. Iannuzzi, F. Schimann, and J. VandeVondele, “QUICKSTEP: Fast and accurate density functional calculations using a mixed Gaussian and plane waves approach”, Wiley Interdisciplinary Reviews - Computational Molecular Science, vol. 4, p. 15, 2014.
[8] S. Goedecker, M. Teter, and J. Hutter, “Separable dual-space Gaussian pseudopotentials”, Phys. Rev. B, vol. 54, p. 1703, 1996.
[9] K. Tomioka, M. Yoshimura, and T. Fukui, “Sub 60 mV/decade Switch Using an InAs Nanowire−Si Heterojunction and Turn-on Voltage Shift with a Pulsed Doping Technique” Nano Lett. 13, 5822 (2013).
[10] J. Tao, J. Perdew, V. Staroverov, and G. Scuseria, “Climbing the density functional ladder: Nonempirical meta-generalized gradient approximation designed for molecules and solids”, Phys. Rev. Lett., vol. 91, p. 146401, 2003.