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Modeling electrostatic doping and series resistance in Graphene-FETs

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***Abstract*—We model the source/drain series resistance and the electrostatic doping effects associated to the source and drain metals in graphene FETs using a Monte Carlo transport simulator. We compare the new model to simulations assuming chemical doping in the source/drain regions. A procedure to include the series resistance as part of the self–consistent Monte Carlo loop is proposed and verified against the widely employed method based on look–up tables.**

***Index Terms*—Graphene FET (GFET), Monte Carlo, electrostatic doping, series resistances.**

I. Introduction

Graphene FETs (GFET) have a great potential as high cutoff frequency devices [1]. However, far from ideal metal/graphene contacts and series resistances reduce the extrinsic transconductance and limit the GFET performance [1]. Since it is difficult to chemically dope graphene [2], metals are used to induce an electrostatic doping and to control the polarity of the source/drain (S/D) regions [3], [4]. Clearly, it is fundamental to account for these effects in GFET simulation tools in order to reliably assess the RF performance of GFETs. The Monte Carlo (MC) method has been used in [5], [6] to describe quasi–ballistic transport in short channel GFETs. Here, we extend the MC transport model of [6] to include the S/D contacts. In addition, the contribution of the series resistances is directly accounted for by dynamically adjusting the terminal voltages in the self–consistent loop for the calculation of device electrostatics as opposed to the time consuming generation of a look–up table based post-processing of the MC transport simulations [6], [7].

II. Modeling Electrostatic Doping

The MC simulator for GFET devices developed in [6] couples, in a self–consistent loop, the Boltzamnn transport equation for electrons and holes in the graphene sheet to the non–linear Poisson equation. A gapless energy dispersion relationship in the graphene is assumed and scattering with acoustic and optical phonons in the graphene as well as with remote phonons in the top–oxide and back–oxide (Fig. 1) are considered. A local model for the band-to-band tunneling (BBT) in graphene (generation–recombination based on the local electric field and occupation function) is also included.

Fig. 1 sketches GFETs with chemical doping (CD, a) and electrostatic doping (ED, b) in the S/D regions. The dashed box is the domain of the MC transport simulation. For the case of chemical doping, S/D regions are part of the domain

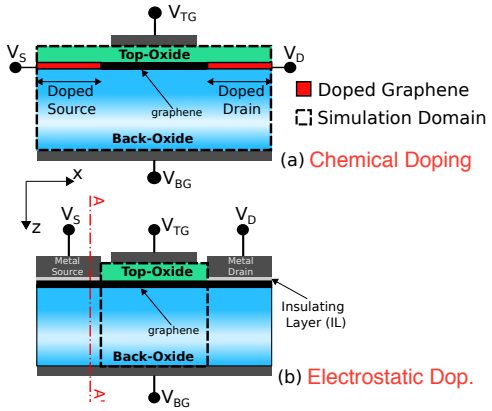

Fig. 1. Sketch of GFETs with chemical doping (a) and electrostatic doping (b) induced by the S/D metals. V_{TG}, V_{BG}, V_S and V_D are the top–gate, back–gate, source and drain biases, respectively.

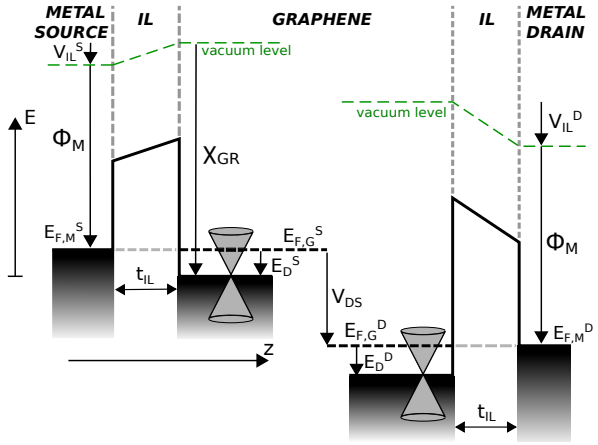

Fig. 2. Band diagram at the source contact along the section AA' of Fig. 1, neglecting the presence of the back–gate (on the left) and the analogous band diagram at the drain (on the right).

and Neumann boundary conditions are used in the Poisson equation [6].

For the case of electrostatic doping, instead, S/D regions are external, but coupled to the MC domain as follows. First, the electrostatics of the vertical metal/grafene stack is solved (see section AA' in Fig. 1(b)), assuming the presence of an insulating layer (IL, by default 0.2 nm of vacuum, consistently with [8], [9]) between metal and graphene, acting as a tunnel barrier [10].

Fig. 2 shows the band diagram of the stack at the source

$$\phi_M - \frac{Q_{GR}}{C_{IL}} = \chi_{GR} - E_D \quad (1)$$

$$Q_{GR} = q\left[\int_{-\infty}^{0} DoS(E)\cdot\left[1-f(E,E_D)\right]dE - \int_{0}^{\infty} DoS(E)\cdot f(E,E_D)dE\right] \quad (2)$$

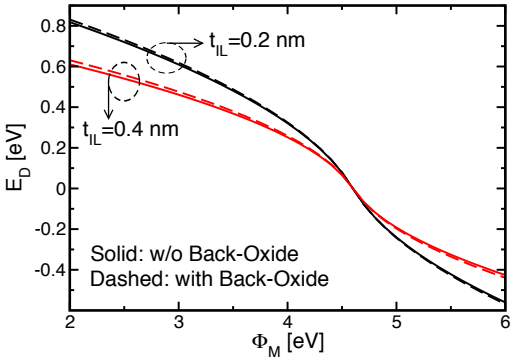

Fig. 3. Energy displacement E_D vs. the work–function of the S/D metal contact considering (dashed line) or neglecting (solid line) the presence of 20 nm of SiO_2 as back–oxide. The source to back–gate voltage is null.

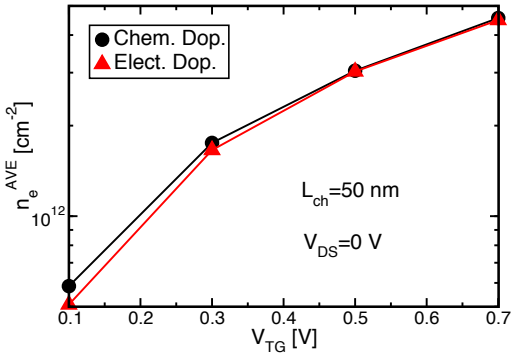

Fig. 4. Average electron density in the channel vs. V_{TG} for GFETs with chemical (circles) and electrostatic doping (triangles).

contact (on the left) and at the drain end of the channel (on the right). To simplify the description, Fig. 2 omits the back–gate insulator and metal, although the simulator implements the entire metal/IL/graphene/insulator/metal structure as in Fig. 1(b). Equations (1) and (2) describe the electrostatics of the stack at the source and drain. *DoS(E)* is the graphene density of states, *f(E,E_D)* is the Fermi-Dirac distribution, C_{IL} is the IL capacitance. In the S/D regions, the solution of Eqs. (1) and (2) provides the charge Q_{GR} and the displacement (E_D^S=E_D^D=E_D) of the Fermi levels (E_F^S, E_F^D) with respect to the graphene Dirac Point, that is then used as Dirichlet boundary condition in the Poisson equation at the left and right sides of the dashed box in Fig. 1(b). If we momentarily neglect the effect of the tunneling resistance (we will discuss its role in Sec. III), the displacement between E_F^S and E_F^D corresponds to the extrinsic V_{DS} voltage directly applied between the S/D metal contacts (see Fig. 2).

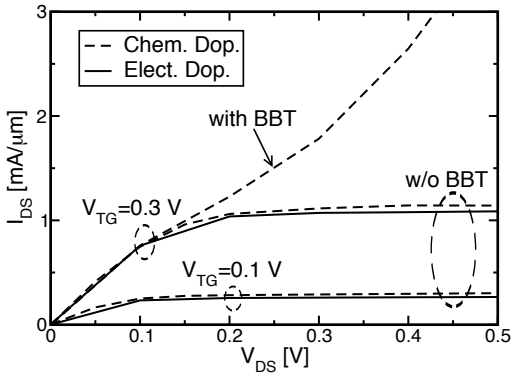

Fig. 5. I_{DS} vs. V_{DS} for GFETs with chemical (dashed) and electrostatic (solid) doping. Results including BBT according to the model in [6] are reported at V_{TG}=0.3 V for the case with CD. BBT model for the ED is under development.

Fig. 3 shows the energy displacement E_D vs. the work–function ϕ_M of the metal contact for a few values of the IL thickness t_{IL} in the metal/IL/graphene stack (solid lines) and in the metal/IL/graphene/insulator/metal structure (dashed lines). As expected, E_D is null when the metal work–function equals the graphene affinity (χ_{GR}=4.6 eV) and, the thinner the IL is, the larger the charge induced in the graphene is, since C_{IL} increases. We see that the presence of the back–oxide (here 20 nm of SiO_2, consistently with what simulated in the following of this work) does not change significantly the amount of the induced charge in the graphene and finally, the value of E_D is almost the same of the previous structure (compare solid and dashed lines).

Concerning the transport simulations of complete GFETs, in both CD and ED cases, carriers are injected at the S/D ends of the MC simulation domain according to a Fermi–Dirac distribution with E_F^S=0 and E_F^D=$-qV_{DS}$, respectively, similarly to what was done for MOSFETs in [11]. For the sake of a fair comparison between the devices in Fig. 1, we set a work–function of the S/D metal (ϕ_M=2.061 eV) that induces in the ED case a Q_{GR}/q=$5{\cdot}10^{13}$ cm^{-2}, that is, exactly the same value of the doping in the CD case. Unless otherwise stated, we simulated report calculations on n-GFETs with channel length L_{CH}=30 nm, 2 nm underlap, 2 nm SiO_2 top–oxide (t_{TG}) and 20 nm SiO_2 back–oxide (t_{BG}).

Fig. 4 compares the average electron density under the top–gate vs. V_{TG} in the case of CD and ED for V_{DS}=0 V. The mutual agreement between curves is good, as expected, since the electrostatics is controlled by the gate, while the S/D regions only set the electron Fermi level. This results proves the correct implementation of the model.

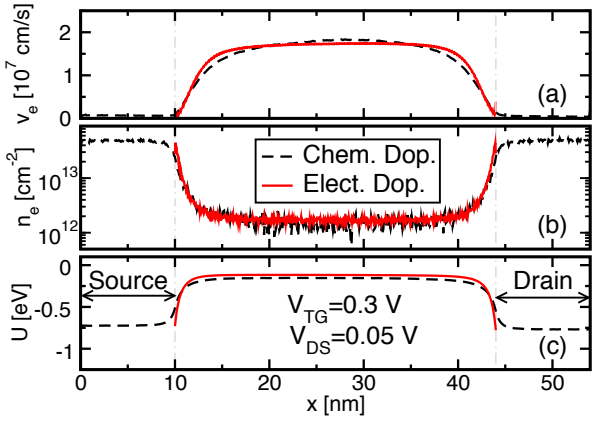

Fig. 6. Electron velocity (a), density (b) and potential energy (c) along the channel for GFETs with chemical (black–dashed) and electrostatic (solid–red) doping for V_{TG}=0.3 V and V_{DS}=0.05 V. Device parameters: L_{CH}=30 nm, 2 nm underlap, t_{TG}=2 nm (SiO_2) and t_{BG}=20 nm (SiO_2).

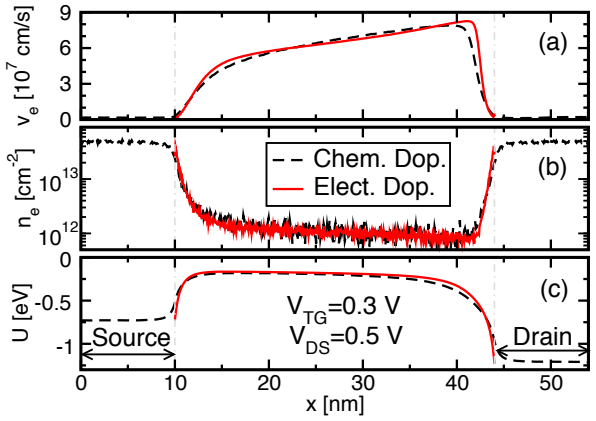

Fig. 7. The same as in Fig. 6 with V_{DS}=0.5 V.

Fig. 5 compares the output characteristics for GFETs with CD or ED in the source and drain. The motivation for the observed differences are investigated with the help of Figs. 6 and 7 showing the electron velocity (a), concentration (b) as well as the potential energy (c) profiles at V_{DS}=0.05 V and V_{DS}=0.5 V, respectively. At high V_{DS} the agreement between these profiles in the CD and ED cases is worse than at low V_{DS}, explaining the small differences in the resulting output characteristics of Fig. 5. For the CD case, simulations including the contribution of BBT are also reported in Fig. 5, showing the typical non–saturated behavior [6]. The BBT model for the ED case is under development, since the determination of the BBT rate requires a careful estimation of the carrier fluxes in the high electric field regions [6] that feature significant differences in the ED and CD cases.

III. MODELING SERIES RESISTANCES

So far we have included the effect of the metal contact on the electrostatics. The non–negligible tunneling resistance of the IL translates into a significant series resistance [12], [13]. In order to have a comprehensive GFET simulation tool,

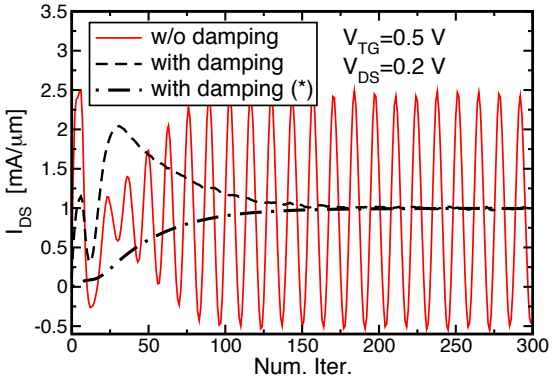

Fig. 8. I_{DS} evolution during the MC simulation of a GFET with series resistance. Without damping procedure, the simulation does not converge (solid line). The damping algorithm solves the problem (dashed line). The dash–dotted line is the current value used in the algorithm to calculate the Fermi-level drop across the series resistances at each iteration.

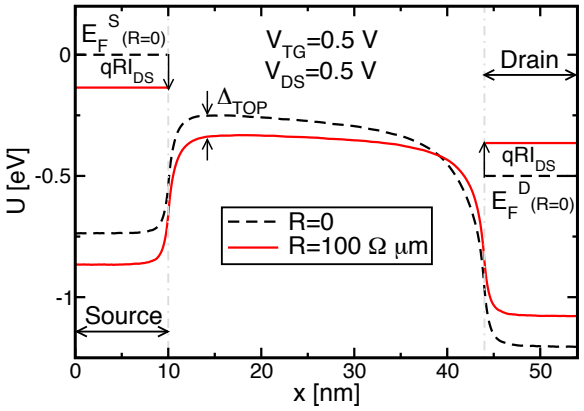

Fig. 9. Potential energy profile along the GFET (CD) without (dashed black) and with (solid red) the series resitances. The Fermi levels in the S/D regions (E_F^S, E_F^D) are reported (dashed black: no R, solid red: with R). The shift of the Fermi levels in the source and in the drain regions reduces the intrisc V_{DS}^i.

we include directly in the self–consistent MC loop the series resistances (R) at each side, inclusive of contributions from tunneling resistance, graphene sheet resistance in S/D, etc. At each iteration, the electrons' Fermi levels of the source and drain are shifted by qRI_{DS}. The instantaneous current (I_{DS}, estimated as an average along the channel of the product between the carrier concentration and the average carrier velocity) requires a proper estimation. In fact, Fig. 8 shows that, without introducing some damping, the simulation does not converge (solid line). To overcome this difficulty, we limit the variations of the RI_{DS} value to less than 1% between two MC iterations. The dash–dotted line in Fig. 8 shows the current value used to calculate RI_{DS}, while the dashed line is the I_{DS} obtained at the given iteration, that converges thanks to the proposed damping scheme.

Fig. 9 shows the potential energy profile for the CD GFET w/o and with R=100 $\Omega\mu$m. For R>0, E_F^S is reduced, while E_F^D is increased, thus reducing the intrinsic voltage drop across the channel (V_{DS}^i=V_{DS}−$2RI_{DS}$). In addition, the

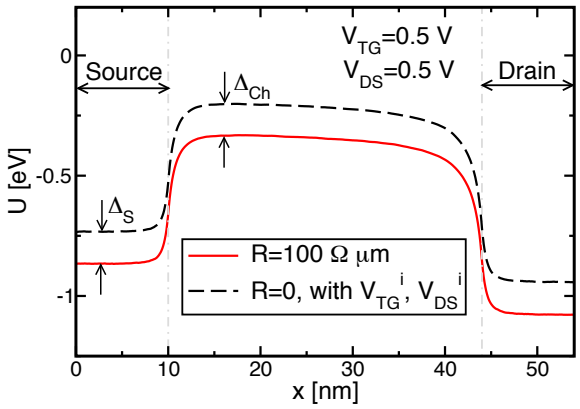

Fig. 10. Potential energy profile along the GFET (CD). Solid red: simulation with V_{DS}, V_{TG} and the series resistance. Dashed black: simulation with the intrinsic biases V^i_{TG}=V_{TG}−RI_{DS}, V^i_{DS}=V_{DS}−$2RI_{DS}$ and without the series resistance. Δ_S=Δ_{Ch} demonstrates that it is present only a pure shift between the two potential energy profiles, since E^S_F and E^D_F are shifted of qRI_{DS} in the two simulations.

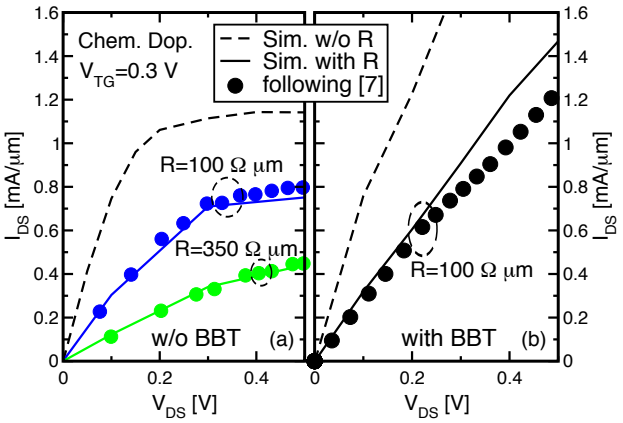

Fig. 11. I_{DS} as a function of V_{DS} for a GFET with chemical doping without (left) and with (right) the contribution of BBT. Results without (dashed lines) and with the series resistance (solid lines) are compared. Symbols are the data without R after the trasformation of the plane (V_{DS}, V_{TG}) to include the series resistance potential drop (as proposed in [7]).

series resistances reduce the intrinsic top-gate bias (V^i_{TG}), as shown in Fig. 10, where the dashed line is the simulation obtained for V^i_{TG}=V_{TG}−RI_{DS}, V^i_{DS} and R=0. The difference between the dashed line and the solid line (again obtained with R=100 $\Omega\mu$m) is almost constant over x and it is exactly Δ_S=Δ_{Ch}=qRI_{DS}. It is interesting to note that Δ_{TOP} in Fig. 9 is smaller than Δ_{Ch}=Δ_S in Fig. 10; this indicates that R not only reduces V^i_{DS}, but also increases the effective potential energy barrier ($\Delta_S - \Delta_{TOP}$) at the injection point, as it should be.

Fig. 11 compares the current with and w/o series resistance to the case where R is introduced as a lumped element by transforming the look–up table of the I_{DS} in the (V_{DS},V_{TG}) plane through interpolation [7]. The agreement between the method of [7] and our implementation where R is introduced in the MC loop confirms the correctness of our technique, that has the advantage of saving the simulation time needed to construct the look–up table (at least a factor of two in time if a coarse table is used).

IV. Conclusion

Efficient implementation of S/D resistance in a MC transport model yields a useful tool to simulate realistic I–V curves of GFETs in reduced times. Physics based models of chemically or electrostatically doped contacts (the main contributor to the series resistance) show that, for the same S/D sheet charge, GFETs with CD or ED drive essentially the same I_{DS} current. Nevertheless, because of technological limitations, such as the difficulty in doping the graphene and the availability of suitable metal contacts, the two solutions may be not equivalent in actual realizations.

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