Simulation of Semiconductor Processes and Devices 2016
Edited by E. Bär, J. Lorenz, and P. Pichler

Impact of BTBT, Stress and Interface Charge on Optimum Ge in SiGe pMOS for Low Power Applications

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***Abstract*— The feasibility of medium-high fraction SiGe based FinFET pMOS devices for a sub-10nm CMOS logic technology from a performance (I_{EFF} @ fixed I_{OFF}) standpoint is evaluated, considering three key device aspects - stress, band-to-band-tunneling (BTBT), and interface charge density (D_{IT}). The analysis reveals that while for high Ge (>90%), performance is limited by BTBT, overall stress reduction beyond Ge 65% further limits performance. Including realistic (D_{IT}) profile further shows that optimum Ge content is between 40%~50% for low power applications.**

Keywords—SiGe pMOS, BTBT, stress, mobility, low-power.

I. Introduction

For continued scaling beyond 10nm node, feasibility analysis of new channel materials such as SiGe for pFET [1] and III-V for nFET [2] employing strain engineering is becoming increasingly important. Although SiGe with high Ge content offers intrinsically higher mobility than strained Si, its lower bandgap results in increased band-to-band (BTB) tunneling leakage. This limits its integration into advanced CMOS technologies, especially for low power. Thus, in this work, we evaluate the feasibility of medium-high fraction SiGe based pMOS FinFET devices for a sub-10nm technology from a performance (I_{EFF} @ fixed I_{OFF}) standpoint. Performance impact due to three key device design aspects – stress, band-to-band-tunneling (BTBT) and interface charge density, has been investigated. The analysis reveals that while for high Ge content (>90%), performance is limited by BTBT, overall stress reduction beyond 65% Ge content further limits performance. Moreover, taking into account conventional surface passivation issues associated with SiGe which result in increased interface charge (D_{IT}), it is further shown that optimum Ge content is between 40%~50% for low power applications.

II. Device description

A schematic of the FinFET cross section considered in this paper, is shown in Fig. 1 for a (110)/[110] surface/channel orientation. A $Si_{1-x}Ge_x$ channel with different composition of Ge in channel is considered along with lattice mismatch induced stress from substrate ($Si_{1-z}Ge_z$) and embedded source-drain ($Si_{1-y}Ge_y$) regions. Aggressive device dimensions are assumed following the sub-10nm ITRS roadmap guidelines [3]. Drift-Diffusion (DD) TCAD simulations using an in-house developed tool [4] were performed considering detailed modeling of (1) BTBT leakage including quantum confinement related band-gap widening for multiple subbands; (2) full strain-induced mobility and saturation velocity changes with Ge and multiple stress sources; and (3) D_{IT} as a function of Ge content. For each Ge concentration, full device optimization, including source-drain doping is done [5] while considering stress induced suppression of Boron diffusion.

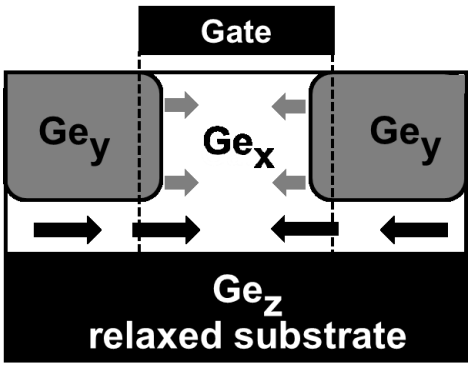

Fig.1: Schematic of device architecture. A SiGe device with different composition of Ge in channel (x), substrate (z) and S/D (y), is considered.

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III. MODELING

A. BTBT

Due to the close proximity (0.14eV) of the Γ and Λ-valleys in Ge, direct BTBT is dominant [6]. In addition, increased S/D doping and channel stress levels also reduce the bandgap thereby increasing leakage. A multi-valley non-local BTBT model has been implemented in an in-house developed semi-classical simulator [7]. The model considers both direct and indirect transitions from valence bands (taking into account anti-crossing effects [7]) to (X, Γ, Λ) conduction band valleys, and uses dynamic search of the tunnel path. Tunneling rate is strongly dependent on the direct-gap separating the top of the valence band and the conduction band at the Γ point. Fig. 2 shows that the direct tunneling component ($\mathbf{E_{\Gamma\Gamma}}$) of the band-to-band generation rate reduces sharply (8 orders of magnitude) with increasing Si content in SiGe alloy, and becomes negligible for Si content > 15%.

In order to capture the effect of geometric confinement in thin fin structures, the width-dependent valley band edges were extracted from an in-house developed 1D Multi-Subband Boltzmann Transport Equation (MSBTE) [7] solver, that is based on the self-consistent solution of multi-subband BTE, and Schroedinger-Poisson equations. A thin layer quantum correction device model including conduction band non-parabolicity effects as well as a valence band correction term was calibrated to match the band-edges, as show in Fig. 3. It can be seen that quantum correction induced bandgap widening starts at fin-widths <10nm. Thus, even for relatively high Ge content devices, the BTB currents can be mitigated by using narrower fin-widths, as it reduces the energy window for tunneling.

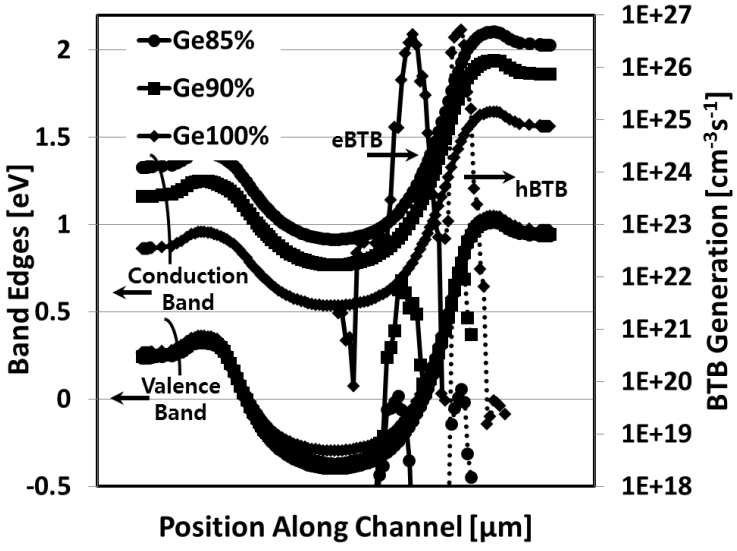

Fig. 2: BTBT modeling: (a) Conduction & Valence band edges (CBE/VBE) and direct BTB generation rate obtained using non-local model for different Ge content. The direct BTB generation rate sharply decreases with reduction of Ge content and is negligible for Ge < 85%.

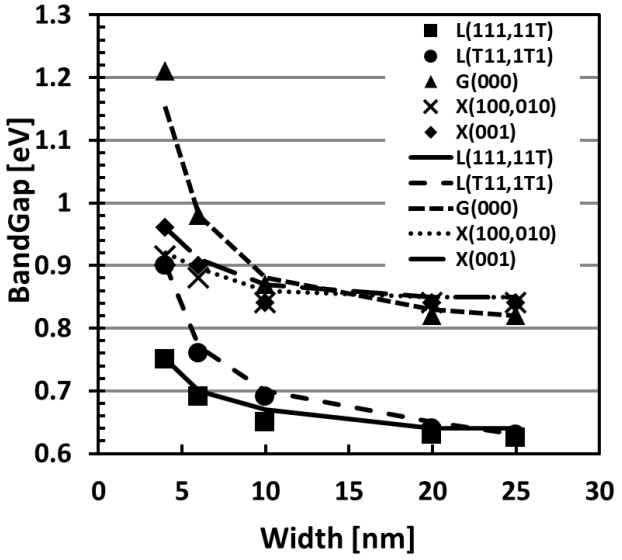

Fig.3: Bandgap vs. Fin width as obtained from MSBTE (symbols). The lines refer to the calibrated Thin Layer quantum correction model for device simulation.

B. Mobility

The key feature for realizing medium-high SiGe channel devices is mobility enhancement. Fig. 4 shows the hole mobility (μ) vs. Ge content for different uniaxial stress levels, as obtained from 1D MSBTE. Scattering due to surface-roughness, coulomb scattering, acoustic and optical phonon

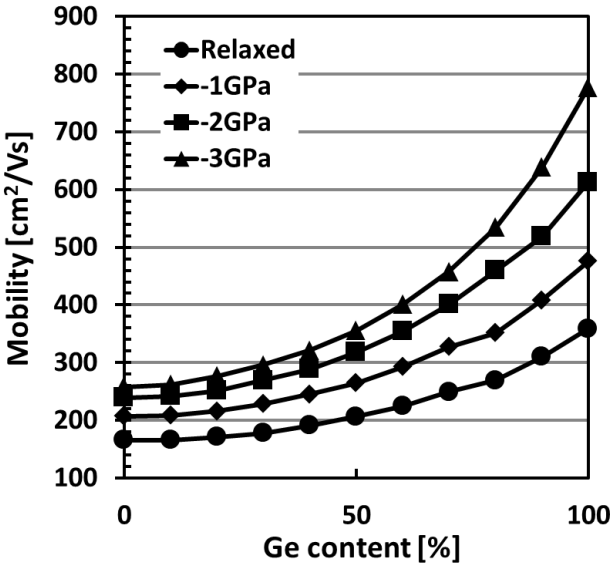

Fig.4: Computed double-gate hole mobility (N_{inv}=1e13/cm^2) for varying Ge content in SiGe alloy for different compressive stress, using MSBTE.

and random alloy, which significantly impacts the transport of carriers are included. It is observed that comparable mobility boost can be expected for medium fraction Ge with ~2GPa and high fraction Ge with ~1GPa stress.

For SiGe alloy device, the alloy disordered scattering is also included. The alloy scattering potential was extracted using MSBTE based on relaxed SiGe20% measured data [8]. A value of U_{ALLOY} = 0.6eV was obtained for planar structure, using which the strained SiGe20% mobility was calculated, which shows good agreement with measured mobility, as seen in Fig. 5a. Using the fixed U_{ALLOY}, MSBTE was used to generate ID-VG curves for different Ge content and density-gradient (DD) parameters were extracted to match the MSBTE sub-threshold behavior.

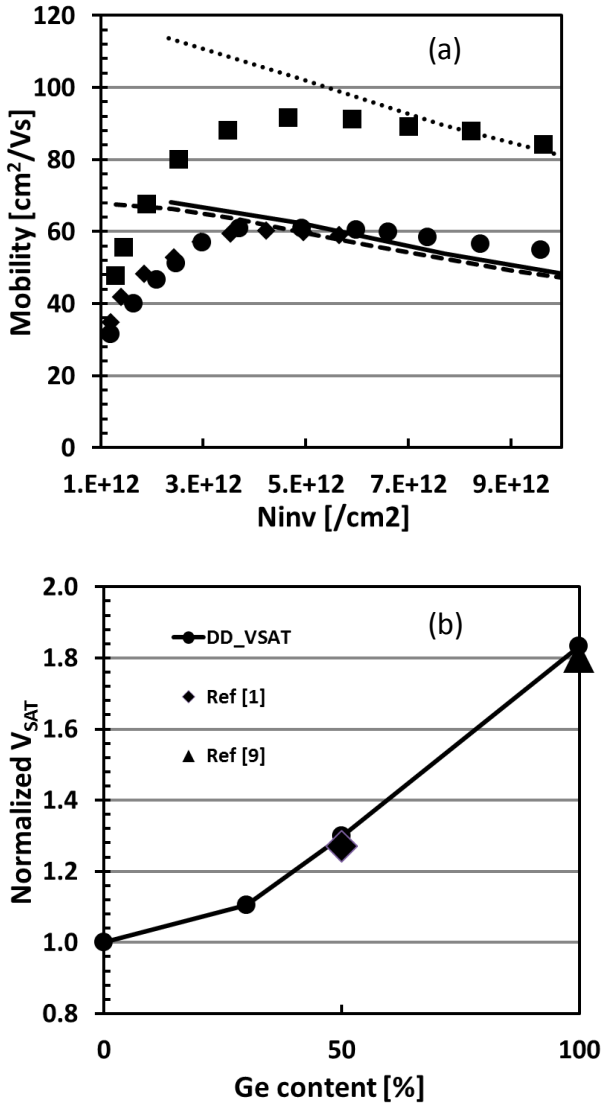

Fig.5: Mobility & v_{SAT} calibration: (a) Mobility versus inversion charge for relaxed Si: diamond symbol (measured), solid line (MSBTE); relaxed SiGe20%: circle symbol (measured), dashed line (MSBTE); strained SiGe20%: square symbol (measured), dotted line (MSBTE). (b) Normalized saturation-velocity, v_{SAT} (DD) versus Ge content.

With the inclusion of scatterings, the MSBTE approach captures the quasi-ballistic transport effects. Therefore, at high-field, the MSBTE can give overshoot of drift velocity which can be larger than the saturation velocity, v_{SAT}, in a bulk system. For DD, in order to mimic this effect, the v_{SAT}, within the high field mobility model is considered as a fitting parameter. The v_{SAT}(DD) relation was extracted to match the experimental data [1,9], with trends obtained by matching to on-current, I_{ON}, from MSBTE, as shown in Fig. 5b.

IV. Performance Evaluation

The impact of three key aspects – BTBT, strain-induced mobility enhancement and interface charge density, on performance (I_{EFF} @ fixed I_{OFF}) are discussed in this section. As stated in section III, BTBT in high-fraction SiGe channel can be significantly modulated by reducing fin-width. Fig. 6 shows that accurate modeling of confinement allows for ~7% increase in Ge content, in the range where mobility increases sharply with Ge content. Thus, proper choice of Si% and fin-width offers a path for low-power (< 1nA/um) application.

Mobility in SiGe channel devices may be boosted by considering a medium fraction strained channel or alternatively with high-fraction channel with intrinsically higher mobility. The composition of channel, S/D and substrate material are chosen such that it generates compressive channel stress. Note that for a fixed S/D Ge content (y) and fixed difference in Ge content between channel (x) & substrate (z), increasing the channel Ge content (x) will reduce the stress from S/D regions, as shown in Fig. 7.

A major concern with SiGe channel devices is the lack of good quality gate oxide stack, resulting in formation of large number of interface states which strongly reduce mobility and

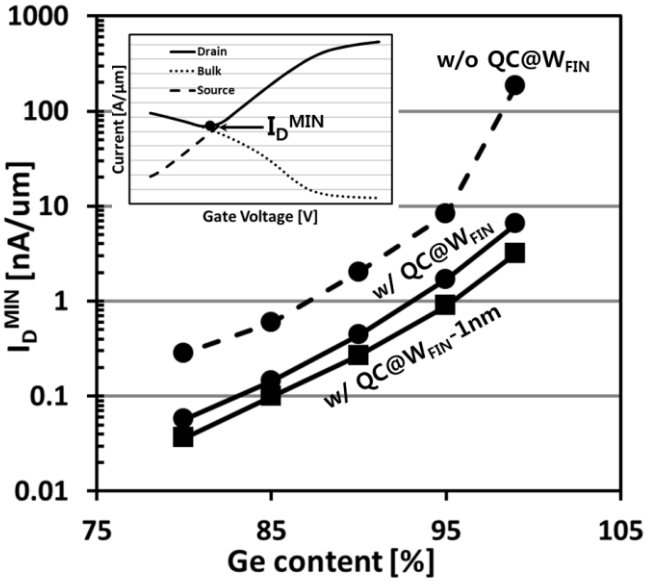

Fig. 6: Impact of quantum correction (QC), with (w/) and without (w/o), on off-current reduction at fixed Ge content, at W_{FIN} and 1nm reduced W_{FIN}. Inset shows I_D^{MIN}, the minimum drain current, considering BTBT.

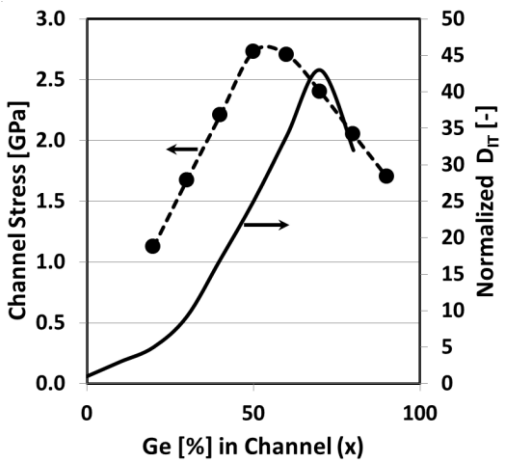

Fig. 7: Stress along channel direction and normalized D_{IT} profile, as a function of Ge content in channel. Mechanical properties of SiGe material are linearly interpolated between the Si and the Ge values. It is assumed that, y - x = 10% ~40% and x - z = 0 ~30%.

increase sub threshold swing. Fig. 7 shows the evolution of D_{IT} profile, using ab-inito simulations, considering up to 2000 different configurations of Si/Ge atoms at the SiGe-SiO_2 interface. With increasing Ge content, the number of dangling bonds increases, resulting in higher D_{IT}. For sufficiently large number of dangling bonds, the probability of bond passivation increases, resulting in a drop in D_{IT} level.

Fig. 8 shows a plot of I_{EFF} @ fixed I_{OFF} for fixed D_{IT} and ab-initio generated D_{IT} profile, uniformly distributed in the bandgap, as a function of Ge content. At fixed D_{IT}, for $Si_{1-x}Ge_x$ x<60%, the channel stress decreases but intrinsic mobility and v_{SAT} increase. The increased Swing due to bandgap reduction is compensated by G_{MMAX} increase, as shown in Fig. 9, resulting in improved on-currents. For x>75%, BTBT significantly increases leakage current while simultaneously the stress benefit of mobility is reduced (G_{MMAX} drop), leading to lower performance. In contrast, for realistic profile, the D_{IT} impact on Swing and mobility degradation (G_{MMAX} drop) becomes much stronger around x=40~50%, and severely limits the performance.

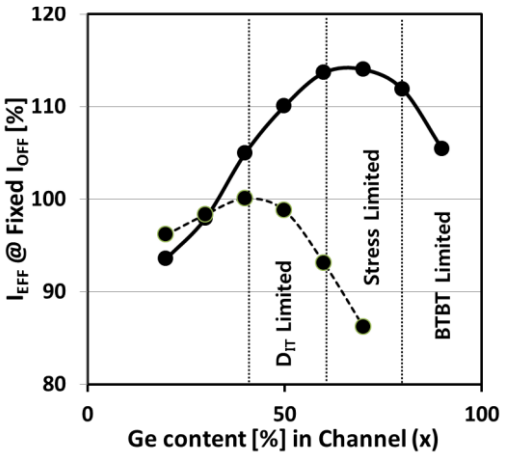

Fig. 8: I_{EFF} @ fixed I_{OFF} versus channel (x) Ge content for fixed (solid line) and realistic (dashed line) D_{IT} profiles. It is assumed that y - x = 10% ~60% and x - z = 0~20%.

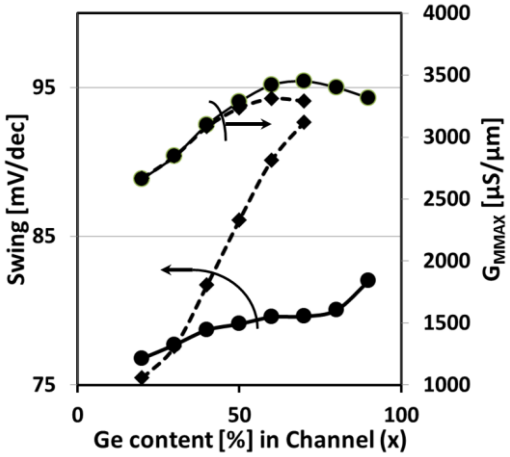

Fig. 9: Sub-threshold Swing & G_{MMAX} versus channel (x) Ge content for fixed (solid circle line) and realistic (dashed diamond line) D_{IT} profile.

V. CONCLUSIONS

Our analysis shows that (1) high-fraction SiGe channel devices can meet low-power requirements with minimum BTBT; (2) both medium and high-fraction SiGe based devices can be realized to deliver high drive currents by proper consideration of interface charge, stress and leakage; (3) the optimum channel Ge content shifts from 65% to 45%, when considering realistic interface charge distribution.

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