Simulation of Semiconductor Processes and Devices 2016
Edited by E. Bär, J. Lorenz, and P. Pichler

Physical Modeling of Ferroelectric Field-Effect Transistors in the Negative Capacitance Regime

P. Lenarczyk and M. Luisier
Integrated Systems Laboratory, ETH Zürich
CH-8092 Zurich, Switzerland
Email: pawel.lenarczyk@iis.ee.ethz.ch

***Abstract*—Field-effect transistors (FETs) with a ferroelectric insulator instead of a conventional gate dielectric have been shown to operate in a negative capacitance (NC) regime when properly engineered, giving rise to a less than 60 mV/decade subthreshold slope (SS) at room temperature. In this paper a comprehensive, physics-based model for the investigation of such ferroelectric FETs (FeFETs) is reported. Contrary to standard semi-analytical and 0-D approaches it relies on a multi-dimensional description of the simulation domain, thus offering the possibility not only to study the characteristics of gate stacks, but also the overall scalability of FeFETs. As key finding it is revealed here that the presence of large electric fields on the drain side of transistors tends to suppress the NC effect, which becomes an issue in short channel devices.**

I. Introduction

For many years, ferroelectricity in ultra-thin films has been investigated as a potential candidate for non-volatile memory cells thanks to the bistability of polarization. Coupling the ferroelectric polarization directly to the channel of a field-effect transistor (FET) provides a uniquely compact memory unit with consequent advantages in terms of size, read-out operation, and costs [1].

In Ref. [2] Salahuddin and Datta proposed a completely new use of ferroelectrics for lowering the sub-threshold slope (SS) of FETs. The underlying idea consists in exploiting the negative capacitance (NC) region of the ferroelectric material, which manifests itself in the negative slope of the P-E (polarization versus electric field) characteristic around the origin. Ordinarily, this negative slope segment is unstable leading to an hysteretic jump in the polarization. However when the ferroelectric is placed in series with a normal capacitor, the negative capacitance segment can be effectively stabilized, making it possible for the surface potential ψ_S to change more than the applied voltage V_g. This provides a step-up voltage transformer that allows for the realization of transistors with steep subthreshold characteristics: SS below 60 mV/dec at room temperature. The concept has already been confirmed by many experimental studies [3], [4], [5].

State-of-the-art, commercially available TCAD tools already offer simulation capabilities for ferroelectric materials through multidimensional electrostatic solvers [6]. The latter are based on the *Preisach hysteresis* model, which assumes an hysteretic behavior of the ferroelectric layer. With this assumption it is not possible to model the NC effect, as shown in Fig. 1. It can be seen there that the Preisach model does not result in a voltage amplification for thin ferroelectric layers, contrary to what is predicted by *Landau theory*. Recent experiments confirmed the NC effect in ferroelectric-dielectric heterostructures [7].

978-1-5090-0818-6/16/$31.00

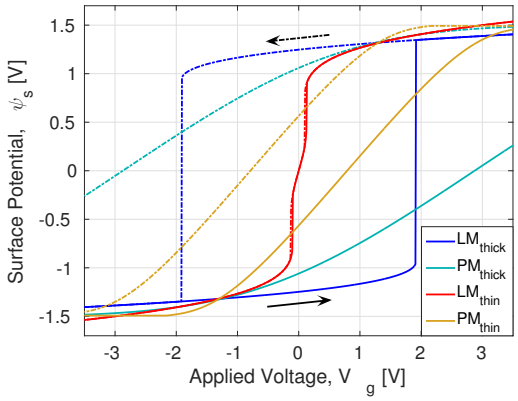

Fig. 1. Salahuddin thought experiment [2] with Landau model (LM) and Preisach model (PM) of ferroelectric. For thick ferroelectric (1000nm) the models qualitatively agree. For thin ferroelectric (275nm) Landau model predicts surface potential amplification and small hysteresis, while Preisach model results in a fully hysteretic characteristics with no voltage gain.

The paper is organized as follows. In Section II a formal description of the newly developed model is presented. It is derived based on a thermodynamic potential of the ferroelectric, which is extended to treat semiconductors and metals. Numerical issues and implementation strategies are also discussed. In Section III the proposed model is applied to Metal-Ferroelectric-Metal-Oxide-Semiconductor (MFeMOS) system. The simulation results are compared with experimental data and the device operation is explained. Then a non-hysteretic FeFET switch based on a properly designed gate stack is examined. Simulations are performed for devices with varying gate lengths and a multi-dimensional drain-coupling effect and its influence on device performance is thoroughly studied. Finally, Section IV summarizes the paper and its main contributions.

II. Method

The starting point of our model is the free-energy density of a ferroelectric crystal proposed in [8]. It takes into account the electrostatic potential-polarization coupling and is therefore very suitable for device simulations. The formalism

is extended to treat non-uniform polariztions through the Landau-Ginzburg approach [9]. To include the influence of the semiconductor material into this thermodynamic description a variational principle of Poisson's equation is employed, where the electronic charge density is incorporated into the energy functional. The latter represents the total potential energy of the system and has the following form:

$$\begin{aligned}\Pi \quad = \quad & \int_\Omega \left(\tfrac{\alpha_i}{2} P_i^2 + \tfrac{\beta_i}{4} P_i^4 + \tfrac{\gamma_i}{6} P_i^6 - \tfrac{g_i}{2} \left|\nabla P_i\right|^2 \right. \\ & \left. + \nabla_i \psi P_i - \tfrac{\epsilon_0}{2} \left|\nabla \psi\right|^2 + \psi \rho \right) \, \mathrm{d}\boldsymbol{x} \ . \end{aligned} \tag{1}$$

In the above equation the three first terms correspond to the *Landau energy density* due to the polarization $\boldsymbol{P}$. The fourth term of *Landau-Ginzburg* theory accounts for an additional energy cost caused by the nonuniform polarization. The fifth term is the electrostatic potential-polarization coupling and the last two terms refer to the electrostatic field energy including the semiconductor charge contribution ρ, where ψ is the electrostatic potential.

Considering the *condition of stationarity* [10] for the functional in Eq. (1) i.e. $\delta\Pi = 0$ a set of partial differential equations (PDEs) can be derived. After performing some differentiations and integrations by parts one obtains:

$$\begin{cases} -\epsilon_0 \Delta \psi = -\nabla \cdot \boldsymbol{P} + \rho \\ \alpha P_i + \beta P_i^3 + \gamma P_i^5 + \Delta P_i = -\nabla_i \psi \ , \ i = x, y \end{cases} \tag{2}$$

The system in Eq. (2) is solved in a device domain with boundary conditions:

$$\begin{aligned} \psi &= V_\mathrm{g} && \text{on} \quad \Gamma_\mathrm{c} \\ (-\epsilon_0 \nabla \psi + \boldsymbol{P}) \cdot \boldsymbol{n}_\mathrm{out} &= 0 && \text{on} \quad \Gamma_\mathrm{ins} \end{aligned} \tag{3}$$

where Γ_c represents the contour of the gate contact(s) and Γ_ins the rest of the domain boundaries. The vector $\boldsymbol{n}_\mathrm{out}$ denotes the unit outward normal to the boundary.

Several of the properly working FeFETs reported so far include a floating metallic gate within their gate stack. This additional layer is modeled by setting its electric field to 0, assuming that the metal is a perfect conductor. The zero electric field condition in metal is enforced by using a Lagrange multiplier λ [10]. This results in an added contribution to the functional in Eq. (1) (with ferroelectric parameters neglected) of the form $\int_{\Omega_\mathrm{m}} \nabla\psi \cdot \boldsymbol{\lambda}$. By requiring the stationarity of the modified functional a set of equations for the electrostatic potential and Lagrange multiplier is obtained:

$$\begin{cases} -\epsilon_0 \Delta \psi = \nabla \cdot \boldsymbol{\lambda} \\ \nabla_i \psi = 0 \end{cases} \tag{4}$$

that is solved in the metal domains.

Due to the mixed formulation of the system in Eq. (2) and the possible discontinuities in the polarization field the space discretization of these equations presents several numerical challenges. Strong oscillations in the polarization variable inside the ferroelectric layer are observed when implementing a finite-difference discretization scheme on a staggered grid.

To avoid those spurious oscillations that cause the divergences of the solver it is necessary to implement a stabilized discretization scheme. In this work a discontinuous Galerkin (DG) finite element method is applied that is known for its stability properties when dealing with problems of a similar form as in Eq. (2) [11]. The application of the method requires rewriting Eq. (2) in a conservative form. This is done by introducing an auxiliary flux corresponding to the displacement vector $\boldsymbol{D} = -\epsilon_0 \nabla\psi + \boldsymbol{P}$. Gauss law of electrostatics is then enforced element-by-element in a conservative way with properly formulated numerical fluxes that ensure the stability of the method. For metal layers governed by Eq. (4) the same procedure applies, except that the ferroelectric parameters are set to 0 and the polarization variable $\boldsymbol{P}$ is replaced by the Lagrange multiplier $\boldsymbol{\lambda}$.

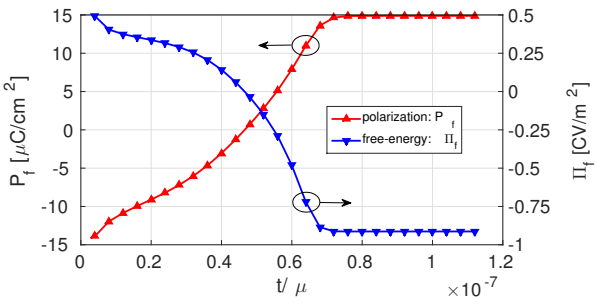

Fig. 2. Polarization switching between bistable states in a ferroelectric capacitor. The evolution of polarization towards equilibrium is driven by the reduction in the total free-energy.

Due to possible multiple solutions for a given bias point and the associated hysteresis phenomena it is critical to verify that the nonlinear system in Eq. (2) converges to the physically relevant solution. This is achieved by following the general framework proposed in [12] and by applying a kinetic equation of the form:

$$-\delta\boldsymbol{\zeta}^\mathrm{T} \frac{1}{\mu} \frac{\mathrm{d}\boldsymbol{\zeta}}{\mathrm{d}t} = \delta\Pi \ , \ \boldsymbol{\zeta} = \begin{bmatrix} \psi \\ \boldsymbol{P} \end{bmatrix} \ , \ \frac{\mathrm{d}\boldsymbol{\zeta}}{\mathrm{d}t} = \frac{\mathrm{d}}{\mathrm{d}t} \begin{bmatrix} 0 \\ \boldsymbol{P} \end{bmatrix} \tag{5}$$

where μ is a kinetic coefficient.

Consecutive iterations on Eq. (5) ensure that the free-energy of the system necessarily decreases along the solution paths, as required by the second law of thermodynamics. This *decrease property* is verified by differentiating the minimized functional Π, giving:

$$\frac{\mathrm{d}\Pi}{\mathrm{d}t} = \left(\frac{\delta\Pi}{\delta\boldsymbol{\zeta}} \right)^\mathrm{T} \frac{\mathrm{d}\boldsymbol{\zeta}}{\mathrm{d}t} = -\mu \left(\frac{\delta\Pi}{\delta\boldsymbol{\zeta}} \right)^2 \leq 0 \tag{6}$$

where the second expression on the right-hand side is obtained by recalling the postulated kinetic equation (5). The equality in Eq. (6) holds for the equilibrium case. The convergence is thus achieved based on physical grounds, as depicted in Fig. (2).

The DG space discretization is combined with a Runge Kutta (RK) scheme to handle the time dependence as in the RKDG method [13]. Note that the rate-dependent terms in Eq. (5) are retained only for the polarization variable, which is treated as the primary order parameter. The Poisson equation constitutes an algebraic constraint in the the space-discretized

system of differential algebraic equations. It is solved with an Implicit-Explicit RK method, where Poisson's equation is treated implicitly and the polarization updates explicitly.

The input of the solver is a set of Landau coefficients α, β, γ as extracted from capacitor measurements. The polarization gradient coefficient g is of the order $10^{-9}\frac{\mathrm{Jm}^3}{\mathrm{C}^2}$. The coupling to the electronic transport comes from the charge density ρ. In this work a drift-diffusion model of electron transport is implemented into a stand-alone simulation tool.

III. Results

The ability of the model to reproduce experimental data is demonstrated in Fig. 3 with the device of Ref. [14]. The investigated p-type silicon FET is based on a Metal-Ferroelectric-Metal-Oxide (MFeMO) gate stack, where a thin metal layer (50 nm of AlSi) is introduced between the gate insulator (10 nm of SiO_2) and ferroelectric (40 nm of P(VDF-TrFE)). The smallest calculated SS for a forward voltage sweep is 34mV/dec, very close to the experimental value of 41mV/dec. A steep switching happens in the strong inversion region in both experiment and simulation. This switching is however hysteretic. The threshold voltage of the backward sweep is shifted towards negative values and the calculated hysteretic window is 0.9V, agreeing very well with the experimental one of 0.8V.

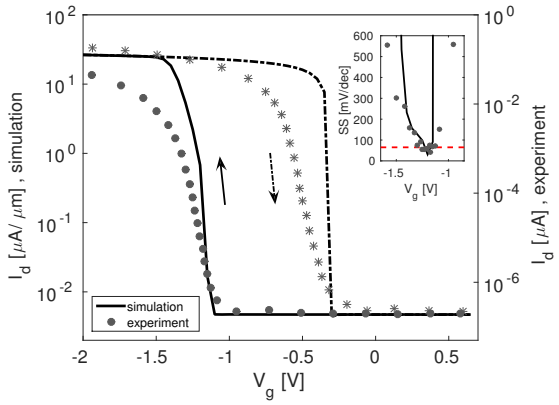

Fig. 3. Transfer characteristics of the FeFET device of [14] ('Fe-FET1'): simulation results (lines, current density) and experimental data (markers, current) [14]. The inset shows the extracted SS values for forward voltage sweep in the subthreshold region. The device exhibits SS<60mV/dec at room temperature. The steep subthreshold slope is due to the negative ferroelectric capacitance in the P(VDF-TrFE)/AlSi/SiO_2 gate stack.

A unique feature of the MFeMO gate stack is the ability to probe the internal metal voltage, which allows to explore the negative capacitance effect [14]. Figure 4 plots the simulated internal metal potential ψ_{int} as a function of the applied gate voltage V_g. As can be concluded by comparing Fig. 3 and Fig. 4 the region of the internal voltage amplification $\mathrm{d}\psi_{int}/\mathrm{d}V_g > 1$ overlaps with the steep switching SS $< 60\mathrm{mV/dec}$ in the drain current of the transistor. The inset in Fig. 4 shows a unique *S-shape* of the polarization with a negative slope with respect to the electric field. This feature

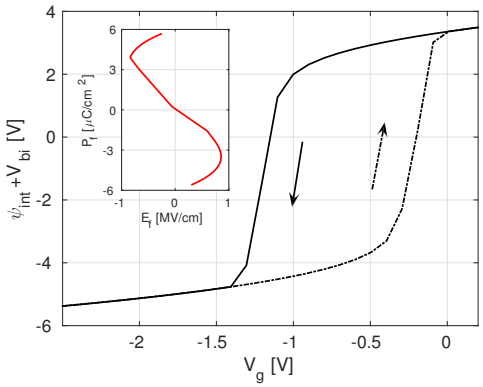

Fig. 4. Internal metal potential ψ_{int} vs. gate voltage V_g in the FeFET device of Fig. 3. The internal voltage amplification $\mathrm{d}\psi_{int}/\mathrm{d}V_g > 1$ overlaps with the sub-60mV/dec switching in the drain current in Fig. 3. The inset shows the polarization vs. electric field $E_f = -(V_g - \psi_{int})/h_f$ in ferroelectric for a forward voltage sweep. An *S-shape* behavior associated with the negative capacitance is found.

is specific to the negative capacitance effect. The negative slope in the polarization appears for electric fields in the range [-8.4, 8.5]MV/cm corresponding to applied gate voltages [-1.4, -0.47]V. They lie in the range where the internal voltage amplification and steep switching take place. This agrees well with the experimental findings in [14].

An optimized FeFET device structure with a ferroelectric insulator thickness exhibiting a non-hysteretic switching is depicted in Fig. 5. The transfer characteristics of the device with a channel length L_c=1μm are reported in Fig. 6. It can be seen that the surface potential ψ_s is up-converted only in a limited range of the applied gate voltage V_g. The surface potential gain $\mathrm{d}\psi_s/\mathrm{d}V_g > 1$ automatically translates into a drain current with SS $< 60\mathrm{mV/dec}$. This is in agreement with the results of a 0-D semi-analytical modeling presented in [15].

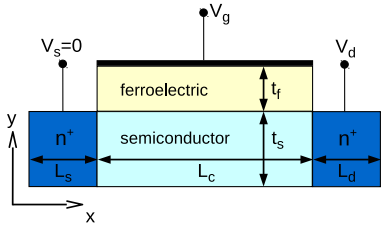

Fig. 5. Cross-sectional view of the studied FeFET. The transistor consists of an intrinsic silicon channel with a body thickness t_s=20nm and a channel length L_c varying between 50nm and 1μm. The source and drain extensions measure L_s=L_d=0.5μm, they are doped with a donor concentration N_D=$10^{20}\mathrm{cm}^{-3}$. The active gate oxide is an SBT ferroelectric characterized by the Landau coefficients: α=$-2.6\cdot10^8\mathrm{m/F}$, β=$5.2\cdot10^{10}\mathrm{m}^5/\mathrm{F/C}^2$ and γ=0, at room temperature. The ferroelectric insulator thickness is set to t_f=15nm.

Interestingly, the step-up conversion capability of the ferroelectric layer is not only a function of the gate voltage, but also of the position along the channel. This is more clearly visible in Fig. 7, which shows the multidimensional

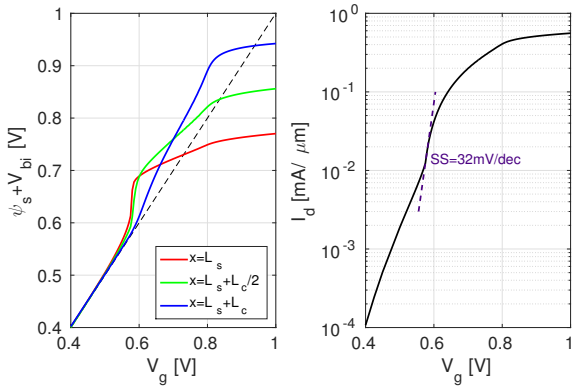

Fig. 6. Transfer characteristics of the FeFET device of Fig. 5. with a channel length L_c=1μm. The voltage applied to the drain is V_d=0.3V, the source is grounded. (left) Semiconductor surface potential extracted at different channel positions vs. gate voltage. (right) Drain current vs. gate voltage. The value of the steepest slope is indicated. The sub-60mV/dec switching happens in the NC region where $\mathrm{d}\psi_s/\mathrm{d}V_g > 1$.

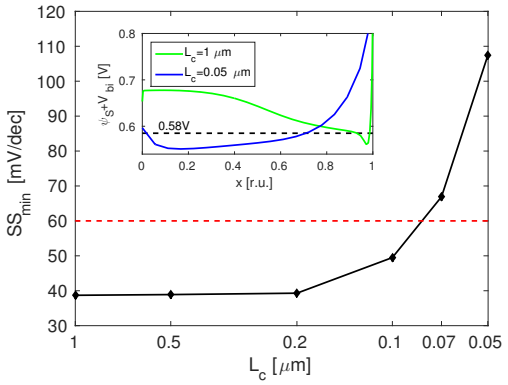

Fig. 8. Channel scalability of the FeFET device of Fig. 5. The main plot shows the smallest value of SS as a function of the channel length L_c. The inset plots the surface potential cross section along the channels of the L_c=1μm and L_c=0.05μm devices. The long-channel device shows surface potential amplification close to the source. For the short-channel device the step-up conversion capability is lost due to drain-gate coupling.

electrostatic potential and polarization profiles of the analyzed device in the NC regime. The electrostatic potential is up-converted only far away from the drain. This is the only region where the semiconductor can develop the necessary inversion charge to screen the ferroelectric polarization. The polarization domain wall (discontinuity in y-polarization component) at the semiconductor-ferroelectric interface acts as an effective positive charge responsible for the potential up-conversion.

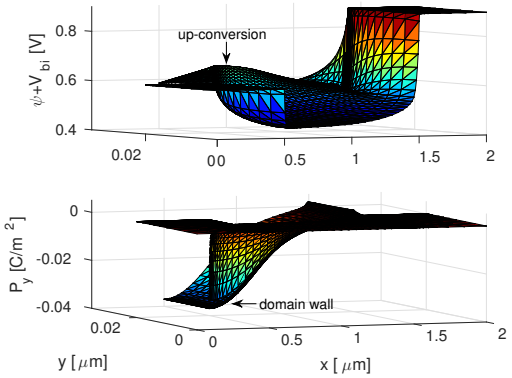

Fig. 7. Multidimensional solution of the electrostatic potential (top) and switchable y-polarization component (bottom), corresponding to V_g=0.58V in Fig. 6. The polarization discontinuity at the ferroelectric-semiconductor interface (y=0.02μm) results into an effective positive surface charge responsible for the electrostatic potential up-conversion.

The position dependence of the NC effect has a serious impact on the FeFET device scalability, as shown in Fig. 8. The smallest value of SS rapidly increases as the channel length goes below L_c=0.2μm. This is explained by the drain-gate coupling effect in the inset of Fig. 8. In long-channel device (L_c=1μm) a 55nm-long region on the drain side is not active, i.e. the surface potential drops as in standard MOSFET. The inactive region covers the entire channel in a L_c=0.05μm device. Consequently, the step-up conversion capability vanishes in the sub-threshold regime and no $SS < 60\mathrm{mV/dec}$ is found anymore.

IV. Conclusion

In summary, a physics-based FeFET model has been rigorously derived and implemented into a simulation tool to allow for accurate device simulations. Results has been compared with experimental data for a MFeMOS transistor, giving a good qualitative and quantitative agreement. A non-hysteretic FeFET switch with optimized gate stack has been considered to examine the multi-dimensional character of the NC effect. The drain-gate coupling has been found to suppress the step-up conversion capability in short channel devices. A consequence is a limited gate length scalability of NC FeFETs. Although the reported results have been mainly discussed in the context of low-power logic switches, the model formulation is general enough to additionally describe the hysteretic behavior of ferroelectric layers. It is therefore applicable to the design of FeFET-based nonvolatile memories.

Acknowledgment

This work was supported by SNF grants PP00P2_159314 and 200021_149495.

References

[1] J. F. Scott, *Ferroelectric memories*, Springer (2000).
[2] S. Salahuddin and S. Datta, Nano Lett. **8**, 405 (2008).
[3] G. Salvatore et al., in Proc. IEDM, pp. 1-4 (2008).
[4] S. Dasgupta et al., IEEE JXCDC **1**, 43 (2015).
[5] M. H. Lee et al., in Proc. IEDM, pp. 22.5.1-22.5.4 (2015).
[6] Synopsys Inc., *Sentaurus Device User Guide*, V-2015.06.
[7] A. Islam Khan et al., Appl. Phys. Lett. **99**, 113501 (2011).
[8] A. Starkov et al., JETP **116**, 987 (2013).
[9] P. Chandra and P. B. Littlewood, Top. Appl. Phys. **105**, 69 (2007).
[10] O. C. Zienkiewicz, *The Finite Element Method: Its Basis and Fundamentals*, Elsevier (2005).
[11] B. Cockburn et al., SIAM J. Numer. Anal. **40**, 319 (2002).
[12] O. Penrose and P. C.Fife, Physica D **43**, 44 (1990).
[13] B. Cockburn and C. Shu, J. Sci. Comp. **16**, 173 (2002).
[14] G. Salvatore, Doctoral dissertation EPFL, pp. 117 (2011).
[15] D. Jimenez, IEEE ED **57**, 2405 (2010).