A Comprehensive Solution for BEOL Variation Characterization and Modeling

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***Abstract*—A comprehensive variation model is critical to achieve both competitive design and manufacturing yield in advanced technologies. Conventionally, as long as FEOL (front end of line) statistical model is appropriate, BEOL (back end of line) variations given by lumping multiple variation sources into few corners is enough to achieve reliable simulation results. However, as BEOL contribution is becoming more important with device scaling, simulation results with conventional corner model may not always produce optimal design margin. We thus propose a more comprehensive solution for BEOL variations characterization and modeling associated with statistical Monte Carlo simulation.**

Keywords—Process variation; Monte Carlo; Statistical model; Global variation; Local variation; Correlation; BEOL.

I. INTRODUCTION

The dramatic scaling occurred alongside technology advancement has made variation modeling a critical factor for achieving both competitive design and manufacturing yield. While variation is most accurately captured by *statistical model*, for most cases, *corner model* is the preferred choice as it provides a computationally-efficient approximation of variations. Conventionally, as FEOL variation dominates BEOL variation in final circuit variation, simplifying BEOL variation into a few representing corners has limited impact on simulation results. However, as BEOL contribution is becoming more important, BEOL *statistical* modeling is becoming ever more beicial for simulation accuracy.

To reap the benefit of technology advancement, this paper proposes a comprehensive solution for BEOL variations characterization and modeling associated with statistical Monte Carlo simulation. Apart from accuracy improvement, the proposed solution has additional advantage of being directly compatible with existing modeling flow. Experimental results justify our claim that the proposed solution is indeed capable of generating BEOL statistical model as reinforcement for conventional BEOL corner model.

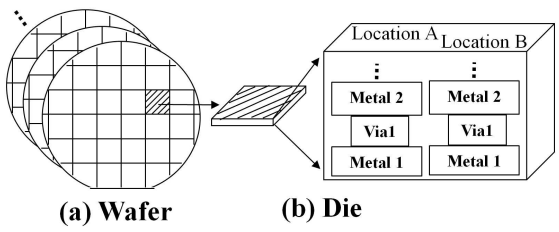

Fig. 1. Test pattern arrangement for BEOL variation characterization. (a) Data is collected from multiple wafers. (b) The same arrangement applies to all dies. Pattern is designed to encompass multiple layers for inter-layer correlation analysis; identical pattern placed at defined Location A and B in the same die enables intra-layer correlation analysis.

II. PROPOSED SOLUTION FLOW

According to BEOL process characteristics, we can consider BEOL structure as composed of the metal layers, and the VIA layers connecting different metal layers. To faithfully model BEOL statistical behavior for simulation, first we need to characterize the variations and correlations *in* (intra-layer) and *between* (inter-layer) every layer.

A. Variation Characterization

The arrangement of the test pattern used for characterization is described in Fig. 1. Data is collected from multiple wafers, every wafer contains multiple dies, and in every die we define *two* locations *A* and *B*. At each location, an identical set of test patterns encompassing multiple metal and VIA layers is placed. Variation characteristics of all layers can then be identified as follows: Firstly, total variation range can be extracted from the complete data set. Secondly, based on correlations between pairs of data from location *A* and *B* of the same die, we can decide whether it is more appropriate to treat variation within a layer as a global or local property. Shown in

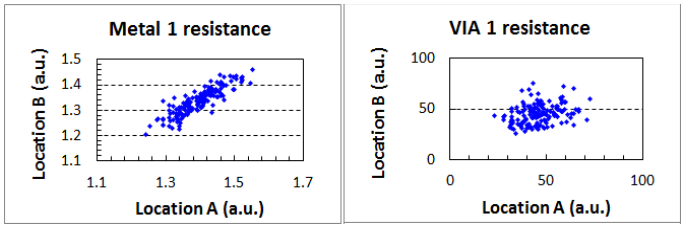

Fig. 2. Example of intra-layer resistance data of location A and B for variation characterization. (a) Strong correlation, (b) weak correlation.

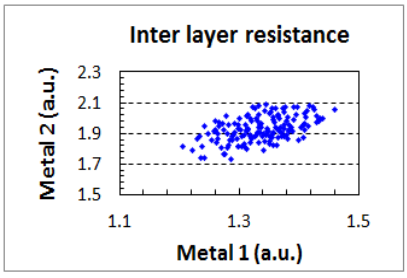

Fig. 3. Resistance data of two layers. The inter-layer correlation is between 0 and 1 (partially correlated).

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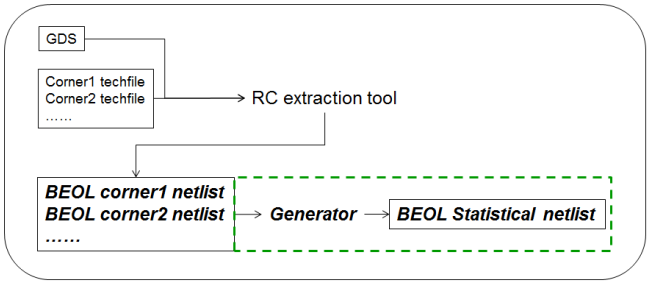

Fig. 4. The position of implemented BEOL statistical netlist generation flow (enclosed in dashed frame) in existing flow; the post-processing strategy requires no change to existing flow.

Fig. 2 are examples featuring two types of variation characteristics, in the metal *(resp. VIA)* layer shown, intra-layer correlation is close to 1 *(resp. 0)* for resistance variation, and can be described as global *(resp. local)* variation. Thirdly, inter-layer correlations between layers are available since patterns are designed to encompass multiple layers: Fig. 3 shows an example with correlation between 0 and 1.

B. Modeling and Simulation

In general circuit design flow, RC (resistance and capacitance) extraction tools provide separate BEOL netlist for every given corner. As described in Fig. 4, our statistical netlist generator takes readily available corner netlists as inputs, and outputs a statistical netlist into which FEOL statistical model can be easily integrated for circuit simulation. The generator works as follows:

Firstly, all resistors and capacitors in the netlist are grouped according to the layer(s) belonged. Secondly, for each group, we assign a set of random variables to calibrate statistically modeled variation according to the corner variation of that layer. Fig. 5 shows that after calibration, the statistical variation of each RC element becomes aligned with its corner variation. Note that if a layer is found to exhibit strong intra-layer correlation (as shown in Fig. 2a), the assigned set of random variables are shared globally in that layer to reflect the fact. However, for layers with weak intra-layer correlation (as shown in Fig. 2b), the set of random numbers should not be shared. Thirdly, *inter-layer* correlations can be specified by assigning the layers' random variables using the following equation [1]:

$$\begin{cases} \Delta Metal1\_ran = par1 \\ \Delta Metal2\_ran = R_{1,2} \cdot par1 + \sqrt{1 - R_{1,2}^{\ 2}} \cdot par2 \end{cases} \quad (1)$$

$\Delta Metal1\_ran$ and $\Delta Metal2\_ran$ are random variables describing variations in layer *metal1* and layer *metal2*. *par1* and *par2* are independent random variables with standard normal distribution; inter-layer correlation extracted from the data is specified as $R_{1,2}$. Finally, a BEOL statistical netlist that considers variations with both intra- and inter-layer correlations can be generated.

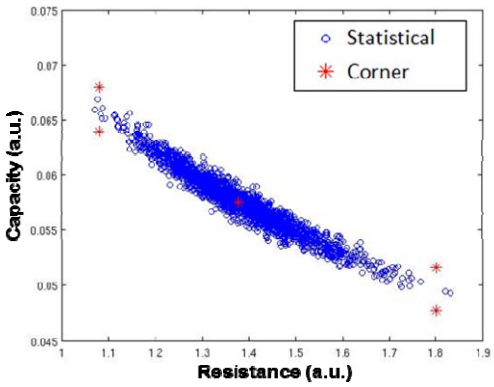

Fig. 5. When a single RC element is considered, the modeled variation range is aligned with corner variation range.

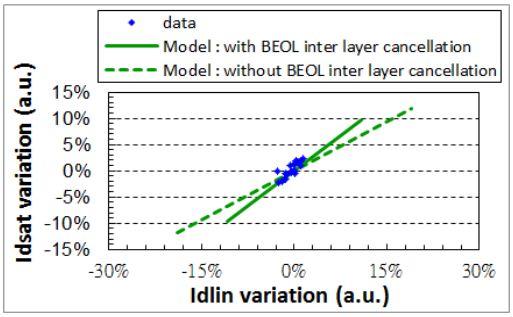

Fig. 6. MOSFET *idsat* vs. *idlin* scatter plot. With BEOL inter-layer cancellation considered, the slope of *idsat* to *idlin* variation matches the data better.

C. Support from FEOL device

For FEOL devices like MOSFET, both *idsat* (saturation current) and *idlin* (linear current) are important performance gauging criteria. However, it is often the case that BEOL resistance has larger impact on *idlin* than on *idsat* in terms of sensitivity. Therefore, as shown in Fig. 6, if the cancellation effect due to smaller-than-one inter-layer correlation is not considered (i.e. directly impose strong correlations between metal layers), BEOL resistance variation predicted by the model becomes too large, resulting in inflated ratio of *idlin* variation to *idsat* variation. Consequently, as BEOL variation grows in importance, neglecting the effect of BEOL inter-layer cancellation during FEOL device modeling can lead to larger deviation.

III. Impact on Circuit Design

In this section, we use three cases to show that both over- and under-estimation of variations are possible when corner simulation is used. This justifies our argument that BEOL statistical model can provide a valuable enhancement to conventional corner model for achieving competitive design without sacrificing yield. Furthermore, to demonstrate the importance of our proposed variation *characterization* step, we also apply sensitivity check to the BEOL statistical model by assigning different correlation conditions. Due to the dependency of variation range on correlation setting, inappropriate variation characterization can lead to deviated simulation results.

The first two cases in this section consider timing paths delay variations, which have critical impact on digital design[2]. Fig. 7 is a schematic of a flop-to-flop structure that is typical of a timing-path unit. The racing between data path and clock path from the common point to their respective pins at the second flop determines whether the input signal can successfully propagate through this path. To ensure this, both *setup* and *hold* timing constraints need to be met. The *setup* timing constraint is to ensure that the data signal arrives at the second flop before the next clock edge (i.e. when the next clock signal arrives), so the *setup* critical paths generally come with their data paths relatively much longer than clock paths. On the other hand, *hold* timing constraint requires data signal to arrive at least a certain time later than the previous clock edge. As a result, the *hold* critical paths usually have data paths relatively shorter than corresponding clock paths.

To be more specific, the *setup* and *hold* criticality of a path can be quantified respectively by the following formulae. In both cases, negative *slacks* imply respective timing violations:

$$\textbf{\textit{Slack}}_{setup} = Clock\ Period + (Delay_{clock\ path} - Delay_{data\ path})$$

$$\textbf{\textit{Slack}}_{hold} = Delay_{data\ path} - Delay_{clock\ path}$$

A. BEOL-contributed Path Delay variation analysis

Since setup timing criticality is determined by how much longer the data path delay is *than* the clock path delay, it is characteristic of a setup critical path (with $Slack_{setup} \cong 0$) to have its setup slack dominated by *data path delay*. As the nets of a data path can actually span multiple layers, variation cancellation caused by inter-layer correlations can have large impact on real data path delay (and $Slack_{setup}$). **In corner-based model**, *all* components are directly set to be *strongly correlated*, when least cancellation occurs, the total delay variation (σ_{delay_corner}) is simply the linear summation of delay variations caused by every composing layer:

$$\sigma_{delay\_corner} = \sigma_{Metal1} + \sigma_{Metal2} + \cdots + (\sigma_{VIA1,A} + \sigma_{VIA1,B} + \cdots) + (\sigma_{VIA2,A} + \sigma_{VIA2,B} + \cdots) + \cdots \quad (2)$$

Where σ_{Metali} denotes the delay variation contributed by all components in metal layer $i \in \{1, 2, \ldots, N\}$, and $\sigma_{VIAj,k}$ is the delay variation contribution of location $k \in \{A, B, \ldots\}$ in VIA layer $j \in \{1, 2, \ldots, N\}$. In statistical simulation, different settings of intra- and inter-layer correlations lead to different levels of variation cancelation. For example, in layers with near-zero intra-layer correlation, such as the one shown in Fig. 2b, variations are largely averaged out due to their local nature. Further variation reduction is possible if *inter-layer* correlations are also taken into account. Here we present one example of delay variation (σ_{delay_stat}) calculation assuming totally independent VIAs :

$$\sigma_{delay\_stat} = \sqrt{corr(m,n) \cdot \sum_{m=1}^{N}\sum_{n=1}^{N} \sigma_{Metal\,m} \cdot \sigma_{Metal\,n} + \sum_{j=1}^{N}\sum_{k} \sigma^2_{VIAj,k}} \quad (3)$$

In Fig. 8, the setup slack ($Slack_{setup}$) of numerous critical paths are plotted for different scenarios. Data of different paths are distributed along the x-axis (path *ID)*. ***TYP*** (resp. ***Corner***) is the simulation result based on the circuit's respective corner

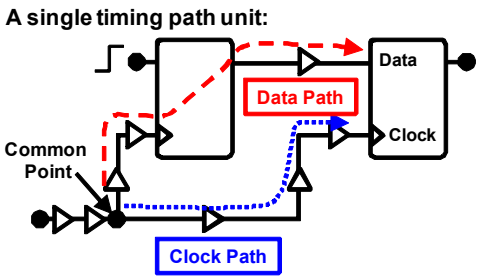

Fig. 7. Schematic for a single unit of flop-to-flop timing path in digital design

model, in which each element is set to its ***typical*** (resp. ***minimum***) corner value. The other two curves plot the lower bound *(median-3*sigma)* of statistical Monte-Carlo simulations under different correlation assumptions. The two assumptions are as follows:

1. **Monte Carlo (All VIA independent)**

	Metal Layer	Via Layer
Intra-layer Correlation	1	0
Inter-layer Correlation	0	0

2. **Monte Carlo (Same VIA layer fully-correlated)**

	Metal Layer	Via Layer
Intra-layer Correlation	1	**1**
Inter-layer Correlation	0	0

The first assumption with all VIAs being totally independent results in strongest cancellation, leading to a *statistical* variation range much smaller than that given by conventional *corner* model. For sensitivity checking purpose, the second assumption increases VIA intra-layer correlation to one, and additional increase in variation from the first assumption demonstrates the impact of correlation change.

Fig. 9 plots the detailed distribution of setup slack statistical simulation results of one selected path from Fig. 8. With relative contributions of different layers to slack variation given in Fig. 9a, simulation results reveal the prohibitively *over-estimated* variation range (approx. 3.5 times that of statistical model based on first assumption) given by conventional corners. Besides, strengthening intra-layer correlations of VIA layers also lead to increase in setup slack variation. These serve as clear evidence that our proposed comprehensive BEOL variation solution does have its benefit.

B. Timing skew variation of two delay paths from BEOL contribution

Timing skew between paths is critical in digital design. Designs based on *underestimated* skew result in circuit failure, such as negative hold slack. Here we would like to point out the potential risk of considering BEOL contribution by conventional, lumped corners only. I*n hold critical paths, data path* delay is usually close to *clock path* delay*, and* the *BEOL variation* values of the two paths *are comparable.* In corner

model approach, data path and clock path delays are assumed to exhibit the same trend, so cases with clock path and data path delay varying in different trends are not covered. As the trend difference can lead to simultaneous decrease in data path delay and increase in clock path delay, possible timing violation can escape timing check based on corner model only.

In Fig. 10, the *hold slack (Slack$_{hold}$)* of numerous critical paths are plotted for different scenarios. The four scenarios are the same as described in Sec. III.A. Fig. 11 then plots the detailed distribution of hold slack statistical simulation results of one selected path from Fig. 10. Here we demonstrate one cause of delay trend difference between clock path and data path. Since different metal layers have different statistical behaviors, and the pair of data path and clock path under competitive racing might be dominated by different layers, as shown in Fig. 11a, corner skew can actually become smaller than statistical variation. This *underestimation* of timing skew variation is especially critical for hold slack analysis, since a hold failure directly results in timing logic error.

C. *FEOL Co-simulation with BEOL statistical model*

For existing FEOL-BEOL co-simulation, corner model remains the only allowed choice for BEOL modeling while both statistical and corner FEOL models are allowed. Our proposed methodology overcomes this limitation. Designers are offered the option to consider BEOL statistical behavior alongside FEOL statistical behavior. As depicted in Fig. 12, possible reduction in total variation range resulted from considering two sources of variations together can now be captured.

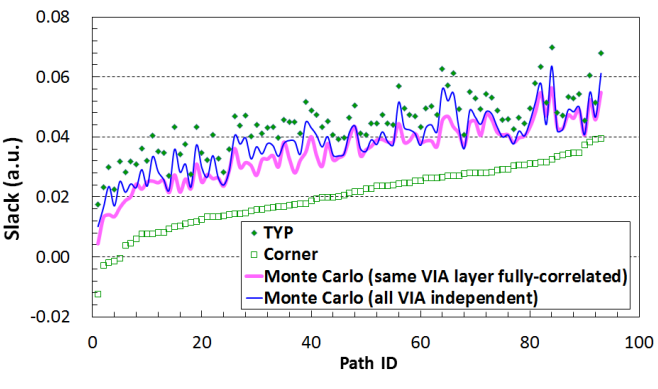

Fig. 8. Setup slacks of numerous critical paths under different scenarios.

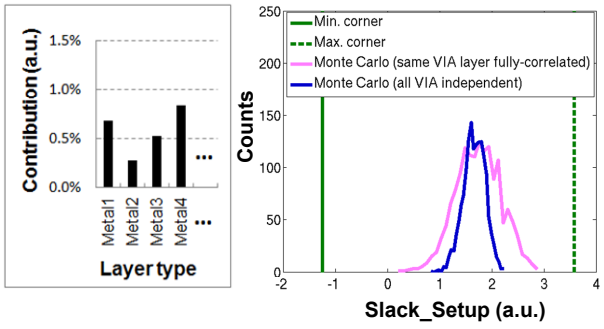

Fig. 9. Setup slack distribution of one selected path. (a) Relative contributions different layers to slack variation. (b) Simulation results.

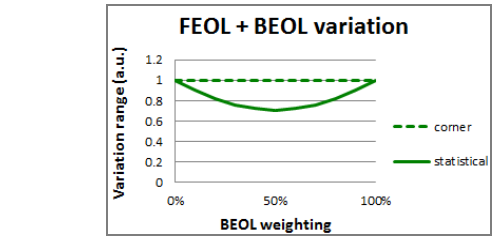

Fig. 12. Total variation ranges given by conventional corner model and statistical model under different BEOL weighting.

IV. Conclusions

This work enables BEOL statistical simulation that is directly compatible with existing simulation flow. A comprehensive characterization and modeling approach associated with statistical simulation is realized with a BEOL statistical netlist generator. Analyses based on three case studies justified the significance of an appropriate variation model to circuit performance/design.

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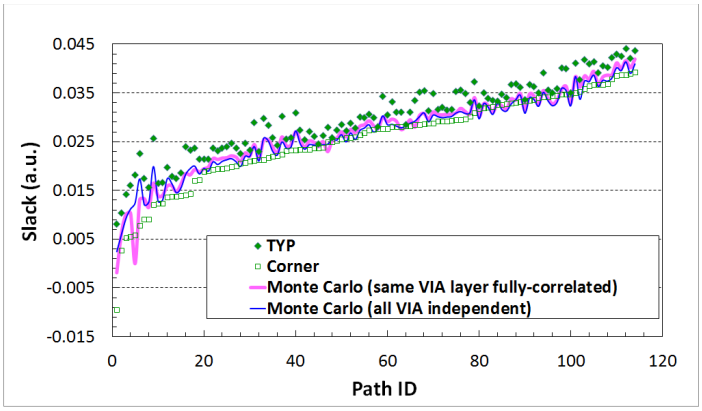

Fig. 10. Hold slacks of numerous critical paths under different scenarios.

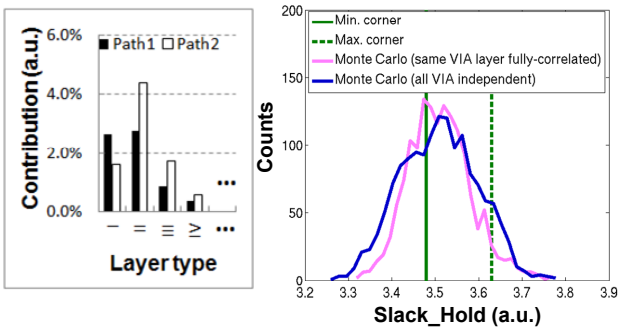

Fig. 11. Hold slack distribution of one selected path. (a) Relative contributions different layers to slack variation. (b) Simulation results.