Simulation of Semiconductor Processes and Devices 2016
Edited by E. Bär, J. Lorenz, and P. Pichler

Simulation of Process Variations in FinFET Transistor Patterning

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***Abstract*—The impact of systematic process variations on the pattering for manufacturing of fin field effect transistors (FinFET) has been studied by means of physical-based lithography and topography simulation. To this end, a typical manufacturing sequence for a static random-access memory (SRAM) cell consisting of six transistors has been simulated. Within this sequence, self-aligned double pattering (SADP) is used to create the fin pattern and litho-etch-litho-etch (LELE) double pattering is applied to structure the gate electrodes. Based on the variations resulting from the manufacturing process, the frequency distributions for the fin width and for the gate length have been extracted. These distributions can be complemented by variations imposed by statistical effects to allow determination of the overall effect of systematic and statistical variations on the circuit behavior of the SRAM cell.**

Keywords—FinFET; SRAM cell; self-aligned double pattering; litho-etch-litho-etch double patterning; process simulation; systematic variations

I. Introduction

In cooperative work reported in this and a further SISPAD 2016 paper [1] we investigate the combined impact of systematic process variations introduced by fin field effect transistor (FinFET) patterning and statistical process variations on a static random-access memory (SRAM) cell fabricated in line with specifications for the 14 nm CMOS (complementary metal-oxide-semiconductor) node. Due to the better channel control, the FinFET architecture is largely favored by industry already for the 22 nm node and has a large potential for further scaling. We selected the silicon-on-insulator (SOI) variant of the FinFET because this facilitates the subsequent work on compact modeling [1].

II. Process Flow

For the fabrication of 14 nm node FinFETs based on optical lithography, double patterning is currently the only industrial solution. As discussed in previous work, for instance by Evanschitzky et al. [2], optical lithography is challenged by variations, in particular by those of the focus distance and the illumination dose. These variations lead to variations of the feature size, quantified by the critical dimension (CD). For 14 nm FinFETs the favored technology [3] is self-aligned double patterning (SADP) for the fins, whereas the gates are patterned by litho-etch-litho-etch (LELE), as this allows higher design flexibility.

In the following, the simulation of these patterning processes is described. For the lithography process, the influence of variations of the focus and the illumination dose is investigated. Furthermore, the dependence of the SADP process on the local layout is studied.

III. Fin Patterning

In Fig. 1 the layout of the SRAM cell under investigation is shown. For the pitch of the lines studied in this work, line patterning is not possible by using a single lithography step (assuming 193 nm illumination wavelength and immersion lithography). Therefore, double pattering techniques have to be used. In the SADP process considered in this work, first the so-called fin cores are patterned in a carbon layer using conventional single-step immersion lithography with an illumination wavelength of 193 nm. In theory, this lithography technique has a minimum pitch of 72 nm. The lithography process has been simulated with the simulator Dr.LiTHO [4] to determine the CD of the carbon lines. Using these CD values, solid modeling was employed to create the fin cores, see Fig. 2 (a).

As illustrated in Fig. 2 (b) and (c), spacers are then generated on these fin cores by oxide deposition followed by anisotropic back etching. Similar to other double patterning processes, this process flow results in a duplication of the number of features and in a reduction of the pitch to about one half. The minimum feature size is now defined by the local thickness of the deposited layer, which can in principle be reduced down to one atomic layer. In the example considered, an oxide layer is deposited using low-temperature chemical vapor deposition. This process is modeled based on the deposited thickness for a planar substrate and a constant sticking coefficient of 0.5 for the reactive molecule redistribution model described elsewhere [5]. The deposition simulation is performed using the tool DEP3D [6]. Back etching has been geometrically emulated as being perfectly anisotropic using the simulator SPROCESS [7], see Fig. 2 (c). Due to the non-conformality of the deposition process the thickness of the spacers is smaller at their bottom than at their top, see Fig. 3. For the resulting width of the spacers, the

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following effect is most important: Due to shadowing effects in the deposition process, the spacers deposited between the carbon lines are narrower than those deposited at the outer sides of the outer carbon lines, see also Fig. 3.

Considering variations of the CD of the carbon lines caused by focus and dose variations in the immersion lithography step, SADP strongly reduces the lithography-induced variations for the inner spacers, see Fig. 4. Changing the CD of the carbon lines has an impact on the width of the inner spacers only. Therefore, the SADP process stabilizes the width of the outer spaces at a fixed value considerably larger than that of the inner spacers, see Table I. The width of the fins patterned by SADP depends on the deposition process and the local layout. The latter refers to the position of the spacers (inside a dense line pattern or at the outside of outer lines).

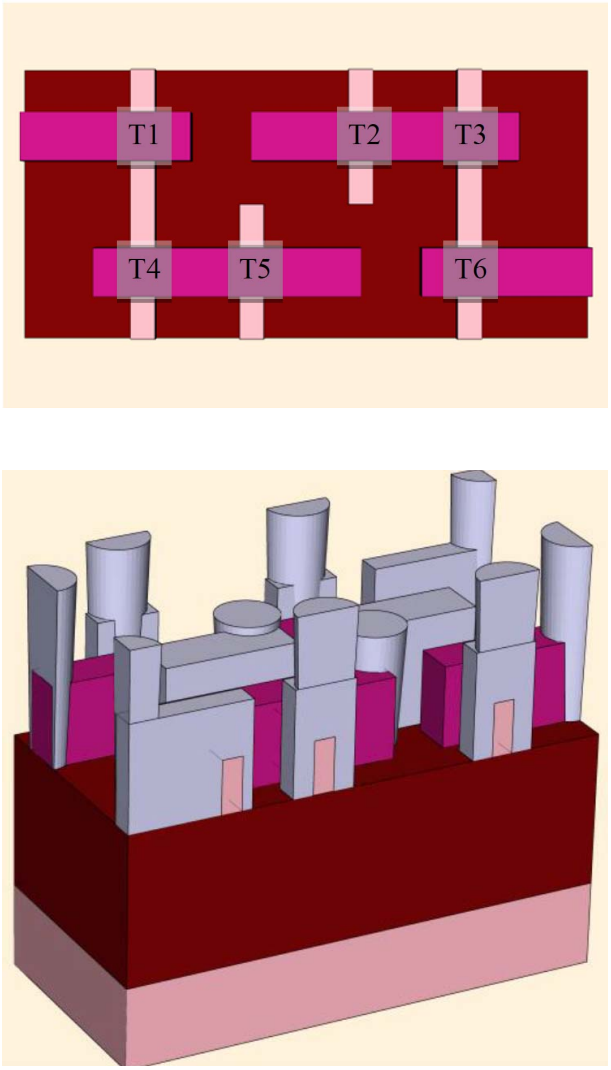
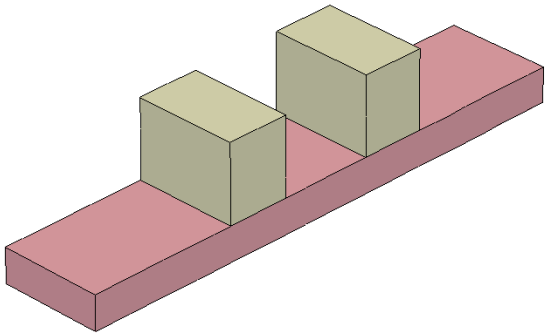
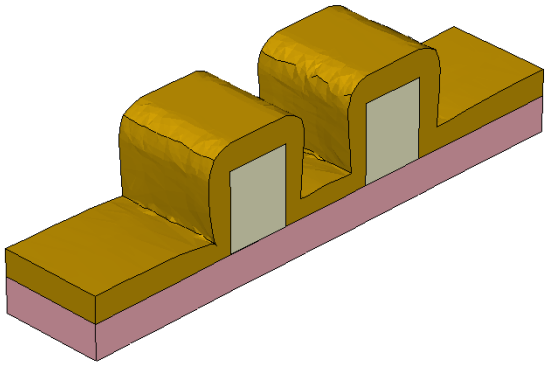


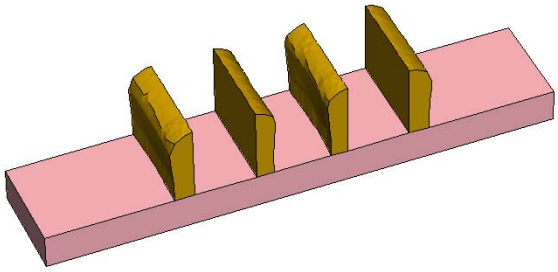
Fig. 1: Layout of a six-transistor SRAM cell with 14 nm SOI silicon FinFETs (top) and a 3D presentation of the cell with metallic contact pads and plugs included (bottom).



(a): Carbon lines patterned by the lithography step



(b): Deposition of an oxide layer



(c): Back etching to create the spacers

Fig. 2 (a – c): Sequence for creating the pattern structure for fin structuring.

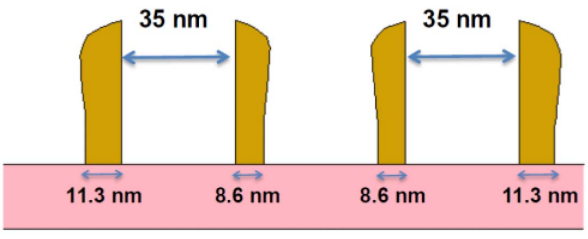


Fig. 3: Analysis of the bottom width of the spacers for carbon lines with a nominal CD of 35 nm.

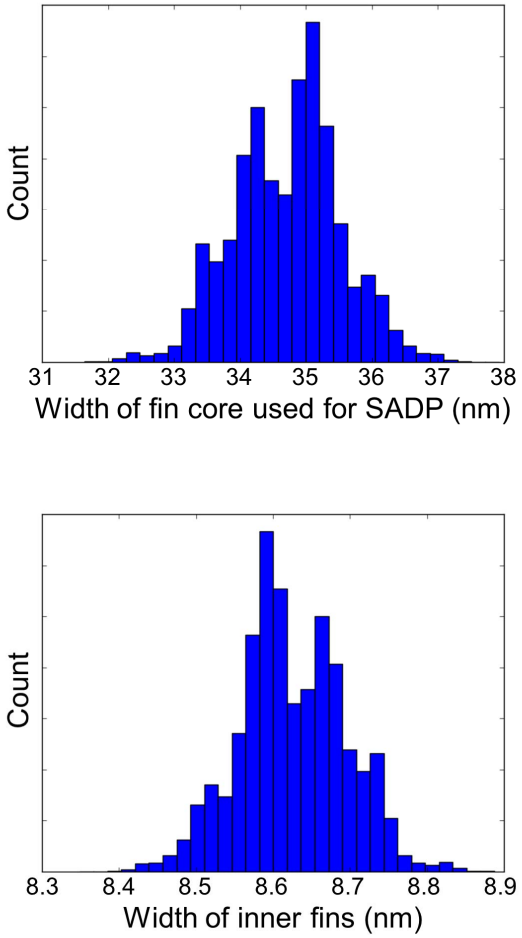


Fig. 4: Widths distribution of the fin core used for SADP (top) and distribution of the resulting inner fin widths (bottom), the outer fins have a constant width of 11.3 nm.

TABLE I
EFFECT OF VARYING THE CARBON LINES CD
ON THE BOTTOM WIDTH OF THE SPACERS

CD (µm)	Bottom width of inner spacers (nm)	Bottom width of outer spacers (nm)
31.5	8.9	11.3
35	8.6	11.3
38.5	8.3	11.3

For the variations caused by the SADP process, the interplay between the deposition and etching processes is most important. For the processes assumed in this work, the inner spacers have a smaller base width which is due to a smaller deposited layer thickness between the carbon lines compared to the thickness at the outer sides of the carbon lines. For other process sequences, this might be different: If the deposition process leads to a perfectly conformal layer, for instance when using atomic layer deposition, and the etching process has a reduced etch rate in the region between the carbon lines, then the inner spacer will have a *larger* width compared to the outer spacers.

As an example demonstrating this effect, we show the spacers resulting from a process sequence consisting of a perfectly conformal deposition process and a dry etching process assuming a spontaneously etching species with a directional angular distribution (modeled by a Gaussian distribution with a FWHM of 0.7 rad), see Fig. 5. The carbon lines are the same as used for the simulation result shown in Fig. 3. It can be seen that now the inner spacers have a larger width than the outer ones. As the deposition process is assumed to be perfectly conformal, the offset between the inner and the outer spacer width depends on the etching process only. The more directional the angular distribution of the etching species, the smaller is the offset between inner and outer spacer width. This is due to the fact that for a more directional angular distribution the shadowing (by the carbon lines) is less important than for a broader angular distribution.

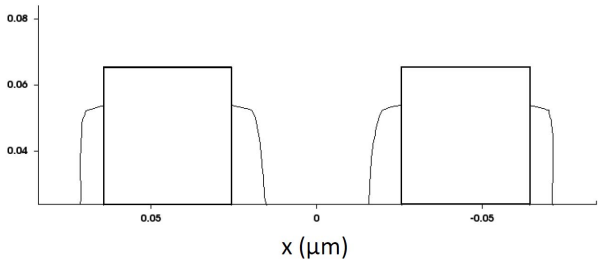


Fig. 5: Spacers resulting from a process sequence of perfectly conformal deposition and dry etching with a directional angular distribution of the etching species. The rectangles represent the carbons lines.

We can conclude that topography simulation allows us to study different deposition and etching process options with respect to the characterization of the process- and layout-dependent variations of the spacer geometry.

It should be noted that the actual fins are generated by subsequent etching processes with the spacers acting as the top mask. These etching processes can introduce additional CD changes which need to be taken into account for the overall analysis of fin CD variability.

IV. GATE PATTERNING

The gate length of the SRAM cell investigated is 20 nm with a pitch of 58 nm, which is again too small for single step lithography. Therefore a litho-etch-litho-etch (LELE) process based on 193 nm immersion lithography is employed. In a LELE process, the structuring is split into two independent lithography steps, for which the gate mask has to be divided into two layers. Although the complex LELE process is usually applied for the generation of multiple gate lengths, in the SRAM example presented here only a single gate length of 20 nm is taken into account.

In each step only each second line out of all lines building the gates is generated: in the first lithography step the first line (horizontal line in Fig. 1 (top) building the transistors T1, T2 and T3), the third line, the fifth line, etc. are structured with a litho-etch process and subsequently the second line (horizontal line in Fig. 1 (top) building the transistors T4, T5 and T6), the fourth line, the sixth line, etc. are generated with a second litho-etch step. Due to this split, the original pitch of 58 nm is doubled and can be realized with a 193 nm immersion system.

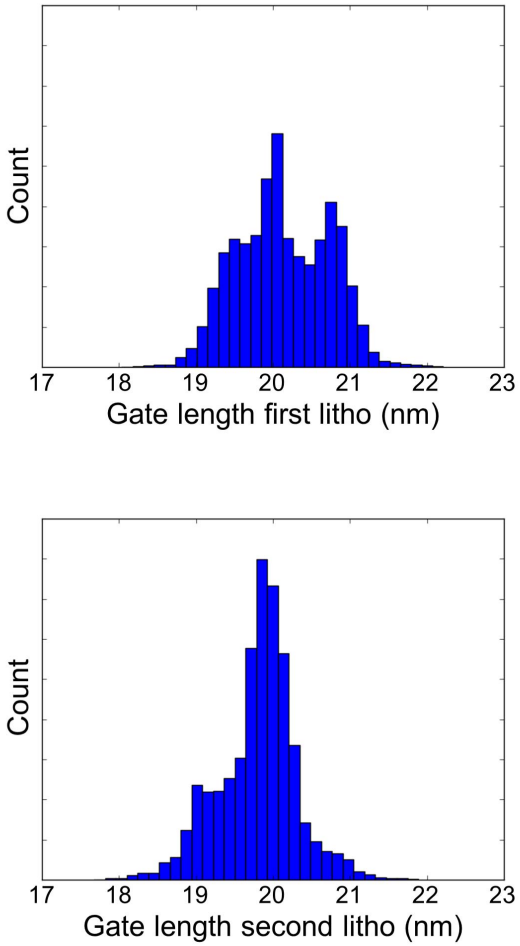


Fig. 6: Distribution of the gate lengths resulting from the first incremental lithography step used for transistors T1, T2 and T3 (top) and from the second lithography step used for transistors T4, T5 and T6 (bottom).

Based on the available technical data and some assumptions for unavailable data, the following system was assumed for the lithography simulations: A dipole source with a sigma inner/outer of 0.52/0.72 and 193 nm transverse electric (TE) illumination, two chrome-on-glass masks for the two lithography steps with 24 nm lines at the corresponding positions (target 20 nm, 4 nm etch bias assumed) and 116 nm pitch (4x reduction), an aberration free water immersion projection system with a numerical aperture of 1.35, and a typical resist with a bottom antireflective coating (BARC). The structures (in the hardmask) resulting from the first lithography step which are covered by the resist for the second lithography step are taken into account by specific rigorous electromagnetic field simulations for the second lithography step. No source mask optimization was performed. All simulations are based on bulk images, where the gate lengths are defined by the bulk image footprint.

Due to peculiarities of the LELE process, the nominal gate length generated in the first and the second incremental lithography process are different, as well as the impact of dose and focus variations on both incremental steps. Fig. 6 shows the gate length variations resulting from the dose and focus variations. The variations are equal within the triples of transistors (T1, T2, T3) and (T4, T5, T6) but different for the two triples. Moreover, the gate lengths variations do not correlate for transistors which belong to different triples.

V. Conclusions and Outlook

The variation-aware circuit simulation of the SRAM cell needs to consider layout effects (inner or outer transistor) on the fin width caused by SADP and the gate length variations caused by focus and dose variations in immersion lithography for the LELE process. The variations due to the LELE process lead to different distributions for the two transistor triples of the cell. There is no correlation between the gate length of the first transistor triple and the gate length of the second transistor triple.

In addition to the process-related effects studied in this paper, stochastic variations caused by the granularity of matter are relevant. The treatment of these stochastic variations and the combination with the process-related effects is discussed in a further SISPAD 2016 paper [1].

Acknowledgment

The research leading to these results has received funding from the European Union Seventh Framework Programme (FP7/2007 – 2013) under grant agreement no. 318458 SUPERTHEME.

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