Carbon nanotube field-effect transistor performance in the scope of the 2026 ITRS requirements

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***Abstract*—Top gate, global back gate and buried gate CNTFET structures with a channel length of 5.9 nm are studied in the scope of the 2026 ITRS requirements. The studies are performed using a numerical device simulator. Figures of merit and performance parameters such as the switching speed, the switching energy, I_{on}/I_{off}-ratio, among others, are obtained for each structure and compared with the 2026 ITRS requirements for different application scenarios. Most of the requirements are met with the buried gate CNTFET. The requirement for the I_{on}/I_{off}-ratio is met at the cost of other performance parameters.**

***Index Terms*—CNTFET, ITRS, switching speed, switching energy, I_{on}/I_{off}-ratio**

I. Introduction

The semiconductor industry has been facing a major challenge since the silicon-based semiconductor technology has come close to reaching its technological and device performance limits, while still trying to push the system performance forward [1]. One potential solution for keeping improving the performance already at the device level is the replacement of the silicon channel by a different semiconducting material, such as carbon nanotubes (CNTs). The corresponding CNT field-effect transistors (CNTFETs) have been predicted to outperform silicon FETs [2]-[4].

The aim of this work is to obtain the figures of merit (FoM) of different CNTFET structures and compare them with the latest requirements of three different application scenarios of the international technology roadmap for semiconductors (ITRS): high-performance (HP), low-operating power (LOP) and low standby power (LSP). The latest ITRS technology node is 5.9 nm anticipated for 2026 [5]. In [6], optimized device parameters have been proposed for high-performance ultra-scaled CNTFETs. However, in [6] the 2026 ITRS requirements for the geometrical dimensions, e.g., channel length, are not met.

In order to predict the behavior of the devices with the recommended gate length of 5.9 nm, the numerical device simulator described in [7] is used. 1D-transport including band-to-band tunneling in the CNT is considered by means of an effective mass Schrödinger-Poisson solver. The simulation boundaries are set directly at the interfaces between the coated and uncoated CNT portions. An additional contact resistance is not included. The reliability of the simulator has been demonstrated in a wide variety of CNTFET studies [8]-[11]. For the study discussed here, the simulator has been calibrated to experimental data (see [12]) of a 9 nm long CNTFET [13].

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II. Simulated Devices

Three different CNTFET structures are studied: a top gate (TG), a global back gate (GBG) and a buried gate (BG). The schematic cross section of each CNTFET structure is shown in Fig. 1. The oxide permittivity is 18 for all structures. The parameters of the simulated devices listed in Table I have been set following the ITRS requirements for the channel length and equivalent oxide thickness.

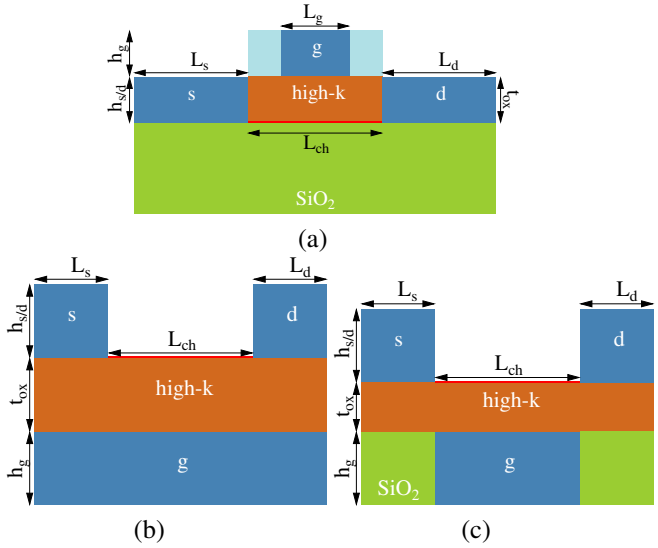

Fig. 1. Schematic cross section of the simulated CNTFET strucutres: (a) top gate, (b) global back gate and (c) buried gate.

For each simulated CNTFET structure, ohmic-like (i.e., ideal) and Schottky (i.e., realistic) contacts are investigated which corresponds to hole Schottky barrier heights ϕ_{SB} of -0.15 eV and 0.15 eV, respectively.

Following the 2026 ITRS requirements given for the HP application scenario, the supply voltage V_{DD} is set to -0.57 V in

TABLE I
DESIGN PARAMETERS OF CNTFETS FOR 2026 ITRS FOMS EXTRACTION

	L_{ch} (nm)	L_g (nm)	d_{CNT} (nm)	$L_{s/d}$ (nm)	$h_{s/d}$ (nm)	h_g (nm)	t_{ox} (nm)
TG	5.9	3	1.4	5	2	2	2
GBG	5.9	11.9	1	3	3	3	3
BG	5.9	5.9	1	3	3	3	2

the simulations. This scenario has the highest supply voltage, which is beneficial for currents and overall performance.

The simulated structures are laid-out for a CNT density of 200 CNTs/µm which is equivalent to a pitch of 5 nm, as suggested in [12]. The simulated devices contain a single CNT and have a width equal to the assumed CNT pitch. By applying periodic boundary conditions it is possible to simulate the electrostatic CNT interactions resulting from such a narrow pitch.

The length parameter defined by the ITRS refers to the gate length L_g. The ITRS parameters are meant for MOSFET-like structures, so L_g is usually equal to the channel length L_{ch}. In the case of CNTFETs, however, L_g and L_{ch} are usually not equal. A TG structure usually has a significant underlap as it can be seen in Fig. 1(a) while a GBG is much longer than the channel as shown in Fig. 1(b). In order to keep the geometrical parameters of the simulated devices comparable to the ones provided by the 2026 ITRS requirements, L_g is still treated as L_{ch} in this work, i.e., as the distance between source and drain, unless it is stated otherwise.

III. PERFORMANCE PARAMETERS

The 2026 ITRS requirements of the three application scenarios for the different FoMs considered in this work are summarized in Table II.

According to the ITRS, both the on-current $I_{on}(= I|_{V_{GS}=V_{DS}=V_{DD}})$ and the off-current $I_{off}(= I|_{V_{GS}=0,V_{DS}=V_{DD}})$ are normalized to the gate width. Correspondingly, in this work both FoMs are normalized with the CNT pitch.

The total gate capacitance $C_{g,tot}$ includes the oxide capacitance and the fringing capacitance and is normalized in the same way as the current.

The intrinsic cutoff frequency $f_{T,i}$ is defined in the ITRS as the frequency at which the small-signal current gain h_{21} drops to one. In the ITRS this parameter is obtained from the extrapolation of h_{21} at 40 GHz with a slope of 20 dB/dec. In this work, an approximation of $f_{T,i}$ is obtained using $f_{T,i} = g_{m,i}/(2\pi C_{g,tot})$, where the transconductance g_m is obtained from the derivative of the drain current with respect to the internal gate-source voltage. Parasitics besides the gate capacitance are ignored. Note that the LOP scenario does not specify a value for $f_{T,i}$.

The intrinsic gate delay CV/I is an estimation of the switching speed of the transistor. The dynamic power indicator CV^2, also known as the switching energy, is an estimation of the consumed energy due to switching between the on-state and off-state of the transistor. The corresponding quantities used to calculate CV/I and CV^2 are $C_{g,tot}$, V_{DD} and I_{on}.

TABLE II
REQUIREMENTS FOR THE PERFORMANCE PARAMETERS GIVEN BY DIFFERENT 2026 ITRS APPLICATION SCENARIOS [5]

	HP	LOP	LSTP
I_{off}(nA/µm)	1×10^2	5	1×10^{-2}
I_{on} (µA/µm)	2.3×10^3	6.6×10^2	2.8×10^2
$C_{g,tot}$ (fF/µm)	4.2×10^{-1}	4×10^{-1}	3.8×10^{-1}
$f_{T,i}$ (GHz)	2.3×10^3	—	2.1×10^3
CV/I (ps)	1×10^{-1}	2.6×10^{-1}	7.3×10^{-1}
CV^2 (fJ/µm)	1.4×10^{-1}	7×10^{-2}	1.1×10^{-1}
I_{on}/I_{off}-ratio	2.3×10^4	1.3×10^5	2.9×10^7
g_m (µS/µm)	6.2×10^3	5.3×10^3	5×10^3

Interesting performance indicators such as the I_{on}/I_{off}-ratio and g_m are not directly specified in the ITRS tables but can be deduced from them. The corresponding values of these performance parameters for each application scenario are shown at the lower part of Table II.

IV. RESULTS AND DISCUSSION

In Figs. 2 and 3, the performance parameters extracted from simulation results of each CNTFET structure with both types of contacts are shown. The recommended values for the 2026 ITRS application scenarios are marked by lines in the plots for each parameter. The shaded areas indicate that the values inside these regions meet the ITRS requirements for both parameters of a specific application scenario.

In Fig. 2 (a), the $f_{T,i}$ versus g_m plot for the three different structures with ohmic-like and Schottky contacts is shown. All CNTFET structures meet at least the LSTP requirement for g_m except for the TG with Schottky contacts. The device with the best channel control, i.e., highest g_m and $f_{T,i}$, is the BG structure, which can be explained by its thinner gate oxide and a reduced parasitic coupling. The BG structure has the lowest $C_{g,tot}$, which translates into an excellent high-frequency behaviour as it can be depicted from the results of $f_{T,i}$. Even though the $f_{T,i}$ value of the TG structure with ohmic-like contacts falls into the LSTP region, only the BG structure meets the LSTP and HP requirements. The BG structure, regardless of the contact type, is the only device which meets the strict 2026 HP and LSTP ITRS requirements for both g_m and $f_{T,i}$.

The switching characteristics of the three CNTFET structures are shown in Fig. 2 (b). All CNTFET structures meet at least the LOP requirement for CV/I, however, only the TG structure with ohmic-like contacts and the BG structure with both type of contacts are fast enough to satisfy the HP requirement. This is directly associated to the improved electrostatics and high I_{on} (see Fig. 3) of the corresponding devices. Regarding the switching energy CV^2, the BG structure is again the device consuming the least energy per switching regardless of the type of contact used. Even though only the 2026 HP and LSTP ITRS requirements for CV^2 are met by the BG structures, the trade-off between switching speed and dynamic power indicator makes these structures suitable for high-performance logic applications.

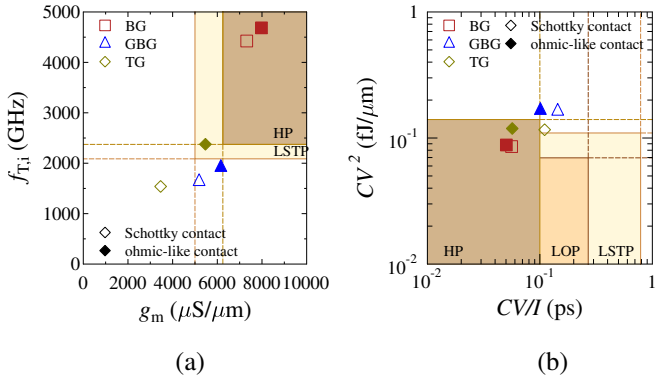

Fig. 2. (a) Intrinsic cutoff frequency versus transconductance and (b) switching energy versus intrinsic gate delay of the simulated CNTFET structures with ohmic-like and Schottky contacts. Values in the shaded regions meet the corresponding 2026 ITRS application scenario requirement.

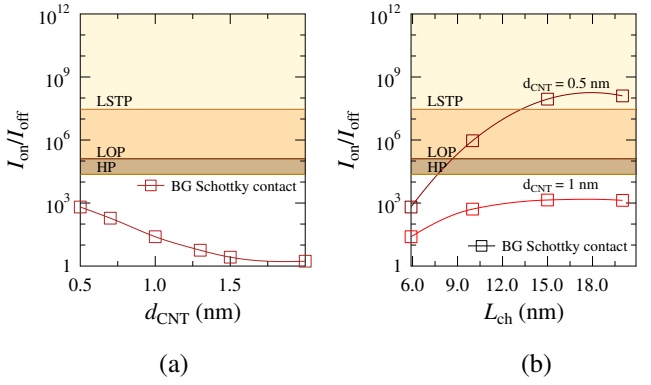

Fig. 4. (a) I_{on}/I_{off}-ratio versus tube diameter and (b) I_{on}/I_{off}-ratio versus channel length of the simulated BG CNTFET structure with tube diameters of 0.5 nm and 1 nm and Schottky contacts.

The plot of I_{on}/I_{off}-ratio versus I_{on} of the simulated CNTFET structures is shown in Fig. 3. Since there is no tunneling barrier for carriers, all CNTFET structures with ohmic-like contacts have larger I_{on} compared to the CNTFET structures with Schottky contacts and meet the ITRS specifications for all scenarios. For Schottky contacts only the BG structure fulfills the 2026 ITRS requirements for all scenarios with an $|I_{on}|$ equal to 2.7×10^3 µA/µm which is much higher than the value reported in [12] for the same pitch and at a similar V_{DD}. It has been seen so far, that the best performance of all the simulated devices is achieved with the BG structure. However, due to the low barrier height (see Fig. 5) leading to high values of I_{off} not even this device can meet the 2026 ITRS requirement for I_{on}/I_{off}-ratio of any application scenario.

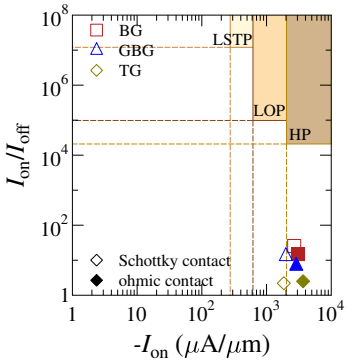

Fig. 3. I_{on}/I_{off}-ratio versus I_{on} of the simulated CNTFET structures with ohmic-like and Schottky contacts. Values in the shaded regions meet the corresponding 2026 ITRS application scenario requirement.

One possible way to improve the I_{on}/I_{off}-ratio is by changing the effective mass which is diameter-dependent [14], [15]. On the left side of Fig. 4, the plot of I_{on}/I_{off}-ratio is shown for CNT diameters d_{CNT}, varying from 0.5 nm to 2 nm using the BG structure with Schottky contacts. The smaller d_{CNT}, the larger is the band gap, i.e., the higher I_{on}/I_{off}-ratio. The highest I_{on}/I_{off}-ratio of 6.5×10^2 is obtained using a CNT diameter of 0.5 nm, however a lower I_{on} and g_m is obtained for this device and the 2026 ITRS goals for I_{on}/I_{off}-ratio are still not achieved of any application scenario.

Another possibility to improve the I_{on}/I_{off}-ratio is to relax L_{ch} while keeping L_g unchanged [16]. The results of the BG structure with Schottky contacts and with CNT diameters of 0.5 nm and 1 nm for different L_{ch} (=5.9 nm, 10 nm, 15 nm and 20 nm) can be seen on Fig. 4 (b). The distance between gate and source/drain contact remains symmetrical for these devices.

It can be seen that, while the BG structure with a CNT diameter of 1 nm can not achieve any of the 2026 ITRS requirements for any of the simulated L_{ch}, a device with a CNT diameter of 0.5 nm meets the HP and LOP requirements with $L_{ch} \geq 9$ nm and all three application scenario requirements with $L_{ch} \geq 15$ nm. The highest I_{on}/I_{off}-ratio of 1.25×10^8 is achieved with $d_{CNT} = 0.5$ nm and $L_{ch} = 20$ nm. This high value is mainly due to a lower I_{off}.

The valence bands along the channel of the BG structure with Schottky contacts and a CNT diameter of 0.5 nm are shown in Fig. 5 for channel lengths of 5.9 nm and 20 nm. A better channel control can be clearly seen in the gated regions. When the devices are in the off-state ($V_{GS} = 0$ V), only thermionic current flows. The value of I_{off} depends on the barrier height, i.e., the difference between the Fermi level in the source and the minimum of the valence band in the gated tube part. The larger the value, the smaller is the current. Furthermore, the longer the channel, the better is the gate coupling since the fringing fields from the source and drain contacts get smaller for longer channels leading to a smaller I_{off}.

While an improved I_{on}/I_{off}-ratio which fulfills the 2026 ITRS requirements for all the application scenarios is obtained with structural changes, the other FoMs for the same devices are degraded and do not meet anymore the 2026 ITRS requirements of any application scenario. Thus, other structural changes such as non-symmetric gate, feedback gate or spacer doping need to be considered in order to find a balance between the I_{on}/I_{off}-ratio and the switching speed and energy in order to meet the ITRS requirements.

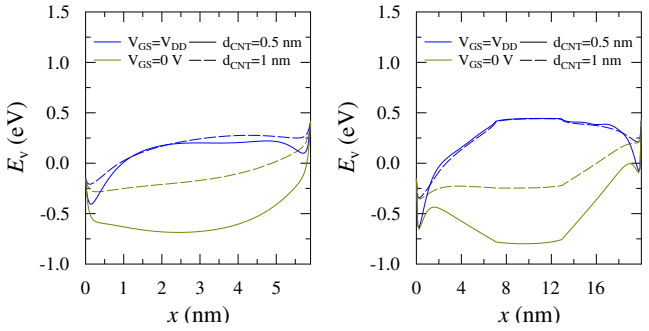

Fig. 5. Valence band diagrams along the channel of the BG CNTFET structure with Schottky contacts for $\mathrm{d_{CNT}} = 0.5\,\mathrm{nm}$ (solid lines) and $\mathrm{d_{CNT}} = 1\,\mathrm{nm}$ (dashed lines) and with (a) $\mathrm{L_{ch}} = 5.9\,\mathrm{nm}$ and (b) $\mathrm{L_{ch}} = 20\,\mathrm{nm}$ while keeping $\mathrm{L_g} = 5.9\,\mathrm{nm}$. Blue (green) lines represent the corresponding valence band at $V_{\mathrm{GS}} = V_{\mathrm{DD}}$ ($V_{\mathrm{GS}} = 0\,\mathrm{V}$).

V. Conclusion

A top gate, a global back gate and a buried gate CNTFET having a channel length of $5.9\,\mathrm{nm}$ and with ohmic-like and Schottky contacts have been simulated using a numerical device simulator enabling 1D-transport including band-to-band tunneling. The simulation results have been compared to the values given by the 2026 ITRS requirements of three different application scenarios.

The BG CNTFET turns out to be the device achieving most of the 2026 ITRS requirements of the different application scenarios for g_{m}, $f_{\mathrm{T,i}}$, CV/I, CV^2 and I_{on}, and even outperforming the on-state current reported in [12] for a demonstrated sub-$10\,\mathrm{nm}$ CNTFET.

However, the simulated $5.9\,\mathrm{nm}$ BG CNTFET is not able to meet the requirements for $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratio of any application scenario. Despite the $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratio, this particular device could be suitable for high-performance logic applications according to discussions previously presented in [6].

In order to achieve the $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratio according to the 2026 ITRS requirements, i.e., to meet the ultra-low power specifications, different structural changes are necessary. $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratio meets the 2026 ITRS requirements for all three scaling scenarios with an BG structure with Schottky contacts, a gate length of $5.9\,\mathrm{nm}$, a channel length larger than $15\,\mathrm{nm}$ and a tube diameter of $0.5\,\mathrm{nm}$. However, this improvement is achieved at the cost of the other performance parameters not meeting anymore the ITRS requirements.

Thus, further structural changes such as non-symmetric gate, feedback gate or spacer doping must be considered in order to find a proper trade-off between $I_{\mathrm{on}}/I_{\mathrm{off}}$-ratio and switching speed and/or energy.

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