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Performance Analysis of p-Type Silicon Nanowire FETs with Silicon-Germanium Cladding

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***Abstract*—The performance of p-type silicon nanowire FETs with three different silicon-germanium cladding options is benchmarked against the silicon reference device. Low-field mobilities and full device characteristics are obtained from the solution of the subband Boltzmann transport equation, including phonon and surface roughness scattering. The subband dispersion is calculated using 6kp band structure model, including the strain induced by the cladding layer. We show that silicon nanowires can be outperformed due to the superior hole mobility of strained silicon-germanium, but the off-state behavior degrades with increasing cladding thickness.**

I. Introduction

The performance of tri-gate FinFET devices can be enhanced by cladding a stress layer onto the channel material. One possible realization of this concept consists of silicon germanium (SiGe) cladded on a silicon fin, having the advantage of being compatible with the typical process flow [1]. For p-type devices, this results in an increased hole mobility and higher drive current [2]. In this paper, we apply the concept of SiGe cladding to gate-all around (GAA) nanowire FETs (NWFET). Due to better gate control compared to FinFETs, GAA-NWFETs represent a possible device architecture enabling further scaling [3].

II. Device Structure and Simulation Approach

We will benchmark the performance of p-type silicon (Si) GAA-NWFETs with a diameter of 7 nm against three different SiGe cladding options, where the germanium mole fraction is 50%. The following geometries are considered: 1 nm SiGe on 5 nm Si core, 1.5 nm SiGe on 4 nm Si core, and 2 nm SiGe on 3 nm Si core. The other design rules are listed in Table I.

The performance analysis is done deploying two different types of simulation. First, we compare the long-channel low-field mobility and the effective transport mass of these devices. This is done on a 2D cross section of the channel, where we solve the self-consistent Schrödinger-Poisson problem using the 6kp band structure model [4]. The stress induced from the SiGe cladding layer is calculated using Sentaurus Process simulator [5] and the corresponding strain is included in the 6kp model Hamiltonian. Averaged compressive stress levels in transport direction within the cladding layer increase from 1.13 GPa for 2 nm SiGe to 1.47 GPa for 1.5 nm SiGe and 1.92 GPa for 1.0 nm SiGe thickness, while tensile stress in transport direction within the Si core decreases from 1.08 GPa to 0.88 GPa and 0.63 GPa respectively. From the resulting confined hole band structure, we extract the effective transport mass and calculate the low-field mobility by solving the linearized Boltzmann equation. Only phonon and surface roughness scattering are considered here. The scattering constants are given in Table II. For phonon scattering, conventional deformation potential models are considered for acoustic and optical phonons, while the surface-roughness model is the same as in Ref. [6]:

$$\langle|M^{SR}_{q_z;nm}|^2\rangle = \sum_{q_s} |\Gamma_{q_s;nm}|^2 \langle|\Delta_{q_s q_z}|^2\rangle \quad (1)$$

$$\langle|\Delta_{q_s q_z}|^2\rangle = \frac{\pi\Delta^2_{so}\Lambda^2_{so}}{LC}\left(1+\frac{\Lambda^2_{so}}{2}(q_s^2+q_z^2)\right)^{\beta_{so}} \quad (2)$$

where n and m denote subband indices, $\Gamma_{q_s;nm}$ is the form-factor containing the derivatives of the wave functions and C is the wire circumference. Note that an exponential function is used for the power spectrum density $\langle|\Delta_{q_s q_z}|^2\rangle$. Linear interpolation in terms of the mole fraction is used to determine the scattering coefficients for the SiGe cladding layers. Coulomb scattering has been neglected since the channel is undoped. Second, we compute the device characteristics of the actual 3D device, as shown in Fig. 1 by solving the subband Boltzmann transport equation [3], [6], [7]:

$$\frac{1}{\hbar}\left(\frac{\partial\epsilon_n(z,k_z)}{\partial k_z}\frac{\partial f_n(z,k_z)}{\partial z} - \frac{\partial\epsilon_n(z,k_z)}{\partial z}\frac{\partial f_n(z,k_z)}{\partial k_z}\right) = C^{in}_n(z,k_z) - C^{out}_n(z,k_z). \quad (3)$$

In Eq. (3) n is the subband index, $\epsilon_n(z,k_z)$ is the subband dispersion, $f_n(z,k_z)$ is the non-equilibrium distribution function and $C^{in}_n(z,k_z)$ and $C^{out}_n(z,k_z)$ denote the in and out-scattering respectively. Since we consider Fermi statistics, Pauli blocking terms are included in the scattering expressions and Eq. (3) becomes a non-linear equation in terms of its solution variable $f_n(z,k_z)$. Therefore, for fixed subband profile, we use a Newton method to solve Eq. (3). During each Newton step, the corresponding linear system is solved using an iterative solver method, since the problem size is typically too large for a direct linear solver. Once we obtain the converged $f_n(z,k_z)$, the subband profile is updated by a Poisson-Schrödinger step. This procedure is repeated until self-consistency is reached. All simulations are performed using Sentaurus Band Structure simulator [4] and Sentaurus Subband Boltzmann simulator [8].

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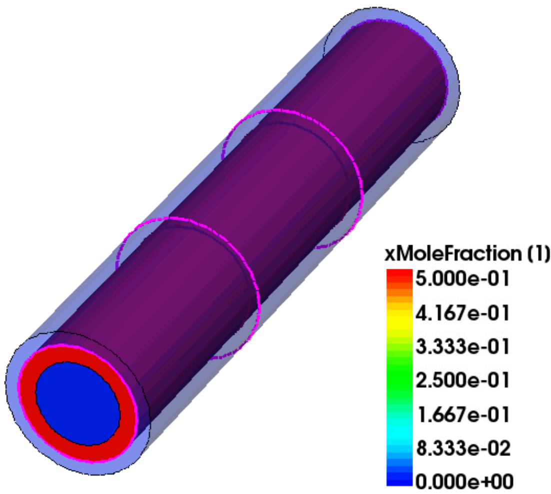

Fig. 1. Device structure of GAA-NWFET with 1 nm SiGe cladding and a 5 nm Si core. Design rules are listed in Table I.

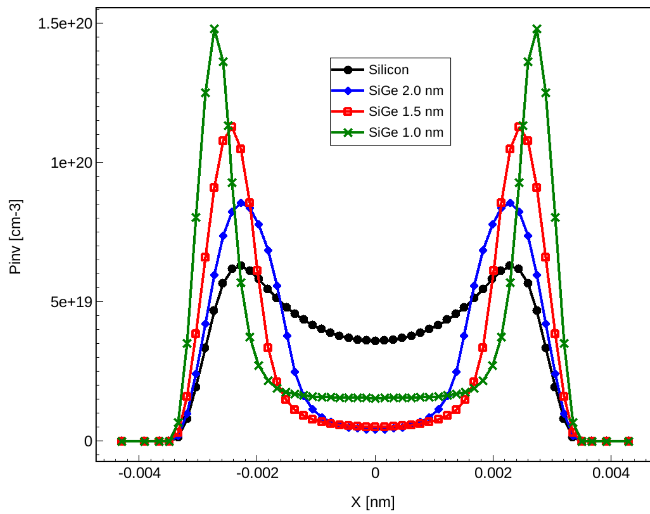

Fig. 2. Hole density profiles on a cutline along [110] direction at total hole inversion charge of $P_{inv} = 5e12\,\mathrm{cm}^{-2}$ after normalizing with the wire circumference. The hole inversion charge is increasingly pushed towards the surface for thinner cladding thicknesses.

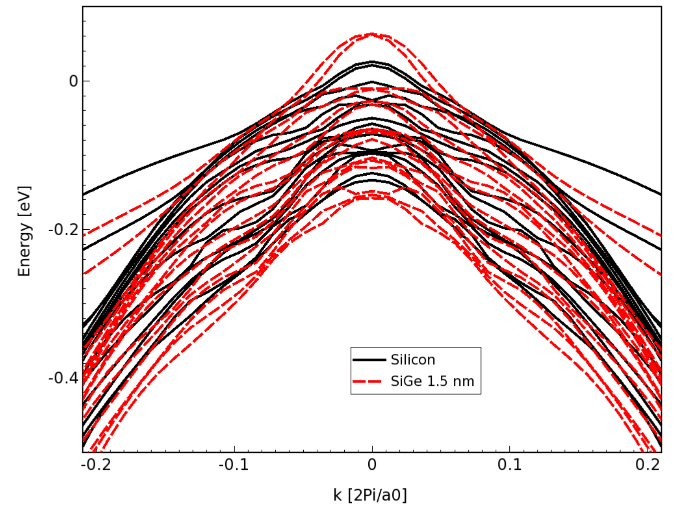

Fig. 3. The subband dispersion of the silicon and strained SiGe 1.5 nm device, calculated at total hole inversion charge of $P_{inv} = 5e12\,\mathrm{cm}^{-2}$ after normalizing with the wire circumference. The difference in the curvature around the Γ-point results in the different effective transport mass reported in Table III.

TABLE I
KEY DESIGN RULES

Parameter	*Value*
Channel Length	13 nm
Gate Dielectric EOT	0.8 nm
Wire diameter	7 nm
Wire pitch	20 nm
Power Supply	0.7 V
Channel & S/D Doping	0, $1e20\,\mathrm{cm}^{-3}$
Channel direction	$\langle 110 \rangle$

TABLE II
SCATTERING PARAMETERS

Parameter	*units*	Si	Ge
Ξ_{ac}	[eV]	13.7	8.1
DtK_{opt}	[eV/cm]	15e8	12e8
$\hbar\omega_{opt}$	[meV]	62	37
Δ_{so}	[nm]	0.25	0.3
Λ_{so}	[nm]	4.0	4.0
β_{so}		-1.5	-2.0

III. RESULTS

In Fig. 2 we show the hole inversion density on a cutline along [110] direction, calculated on a 2D cross-section of the channel at $P_{inv} = 1.1e7\,\mathrm{cm}^{-1}$, which corresponds to $P_{inv} = 5e12\,\mathrm{cm}^{-2}$ after normalizing with the wire circumference. Since the channel is oriented along $\langle 110 \rangle$, the hole distribution in the cross-section does not have circular symmetry: the holes are closer to the [110] surface than the [100] surface. The corresponding subband dispersion is shown in Fig. 3 for the silicon reference devices and the strained 1.5 nm SiGe cladding option. The low-field mobilities are calculated at the same inversion density and are shown in Table III together with the effective transport mass. As can be seen from Fig. 3, the curvature around the Γ point is lower for silicon than for devices with SiGe cladding, resulting in a higher transport mass and a lower mobility. Due to the bulk valence band offset between Si and SiGe, most of the holes are confined to the SiGe cladding layer and increasingly are pushed towards the surface for thinner cladding thicknesses. This reduces the positive effect of SiGe cladding due to increased surface roughness scattering. Due to the lower effective transport mass for holes, SiGe has an intrinsic advantage against pure Si NWFETs. This is enhanced by the stress effect of the cladding on the structure: in Table III, results obtained with the inclusion of stress are compared to

TABLE III
LOW-FIELD MOBILITY AND EFFECTIVE TRANSPORT MASS FOR HOLES

	Mobility [cm^2/Vs]	Mass [m_0]
Silicon	104	0.46
SiGe 2.0 nm	174	0.31
SiGe 2.0 nm w/o Stress	148	0.35
SiGe 1.5 nm	147	0.29
SiGe 1.5 nm w/o Stress	118	0.34
SiGe 1.0 nm	92	0.29
SiGe 1.0 nm w/o Stress	83	0.32

TABLE IV
KEY DEVICE CHARACTERISTICS

	Silicon	SiGe 2.0 nm	SiGe 1.5 nm	SiGe 1.0 nm
Idlin [μA/μm]	104	120	119	111
Idsat [μA/μm]	387	482	525	495
DIBL [mV/V]	41	51	41	37
SS_{lin} at V_{th} [mV/dec]	67	66	66	66
SS_{sat} at V_{th} [mV/dec]	67	82	72	66

those where the stress has been artificially neglected. The stress is increasing the mobility for all three cladding options investigated here. While an analysis of the low-field mobility sheds light on the intrinsic performance of a given channel material composition, the actual device performance including short-channel effects can be evaluated only in a 3D device simulation. Those results are obtained from the solution of the subband Boltzmann transport equation (3). As previously mentioned, only phonon and surface roughness scattering are included. An external resistance of 5 kΩ is added to both the source and drain contacts. The comparison of the saturation currents in Fig. 4 is done for a fixed off-current of 1 nA/μm, i.e. the workfunction has been adjusted respectively. The currents have been normalized by the wire pitch of 20 nm. The comparison of the linear currents is shown in Fig. 5. The ordering of the linear currents is directly correlated to the ordering of the mobilities shown in Table III. The key device characteristics are summarized in Table IV. While all NWFETs with SiGe cladding have a higher on-current than the Si reference device, the subthreshold slope starts to degrade with increasing cladding layer thickness. This is due to the reduced band gap of SiGe compared to Si. Since the band gap is a function of the confinement, the off-current behavior critically depends on the cladding layer thickness. From the data in Table IV, we conclude that there is a narrow window for the cladding thickness: for 2 nm thickness, the subthreshold slope is already degraded and the DIBL increased, while for the 1 nm thickness, the gains in linear and saturation current are lower than for the 1.5 nm case due to the increased surface roughness scattering. Nevertheless, compared to silicon reference device, the device with a 1.0 nm SiGe cladding layer still has better device characteristics. From all the options considered here, the 1.5 nm SiGe cladding layer thickness is the optimal one. In Fig.6, we show its current as a function of drain bias against the silicon reference device for different gate voltages.

For all of the results discussed above, the metal gate of 13 nm is aligned with the junctions. In Fig. 7, we compare

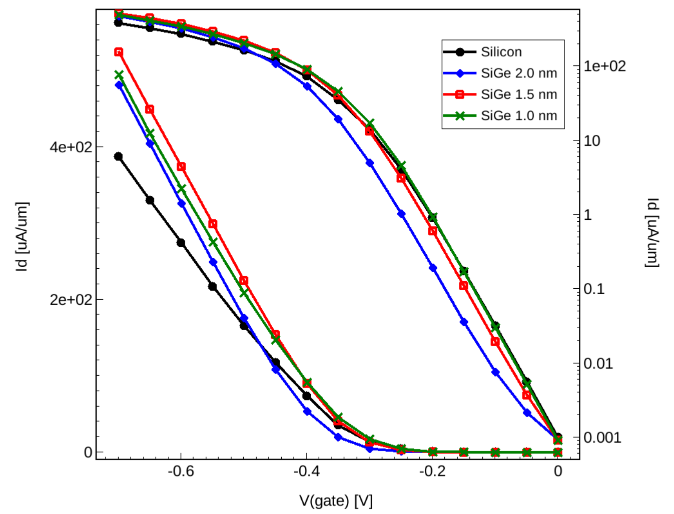

Fig. 4. Saturation current profiles for $V_{DS} = -0.7$ V. Off-current is fixed to 1 nA/μm. Currents have been normalized with a wire pitch of 20 nm. While all three cladding options outperform the silicon reference device in terms of on-current, the off-state behavior degrades with increasing cladding thickness.

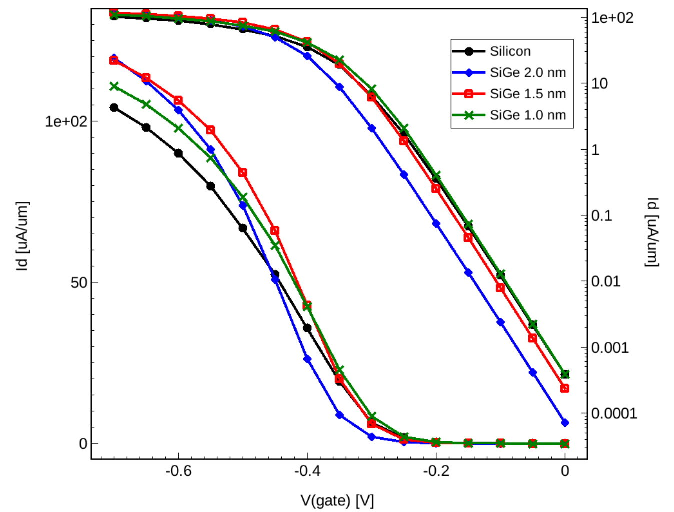

Fig. 5. Linear current profiles for $V_{DS} = -0.05$ V. Currents have been normalized with a wire pitch of 20 nm. With decreasing cladding layer thickness, the current becomes limited by the increasing surface-roughness scattering, which is reducing the effective advantage of the cladding compared to the silicon reference device.

devices with metal gate from 11 nm to 15 nm with aligned junctions (full curves) to devices with 2 nm gate overlap (dotted curves) and 2 nm gate underlap (dashed curves). For a fixed off-current, for example 1 nA/μm, the devices with gate overlap yield the highest on-current for all SiGe cladding options and the silicon reference device. From Fig. 7 it is apparent that the introduction of a thin SiGe cladding layer results in a right-shift of the curves, i.e. an increase of the on-current, up to a cladding thickness of 1.5 nm. A further increase of the cladding thickness from 1.5 to 2.0 nm results left-shift, i.e. a degradation of the on-current. The best per-

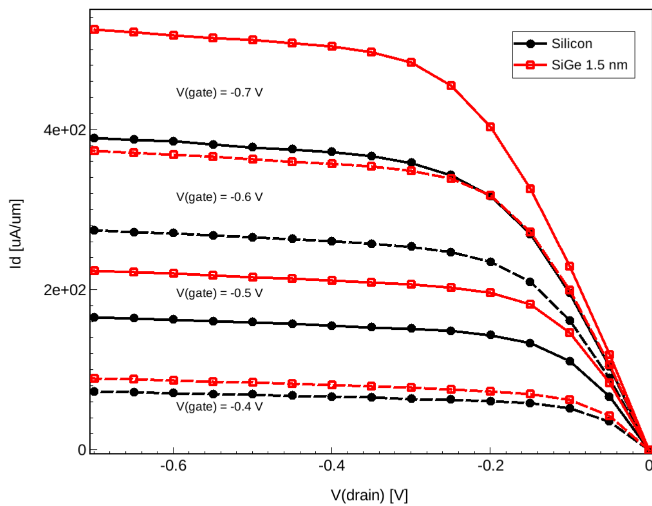

Fig. 6. IdVd current profiles for different gate voltages. The device with SiGe 1.5 nm cladding layer thickness clearly outperforms the silicon reference device in terms of both linear and saturation currents.

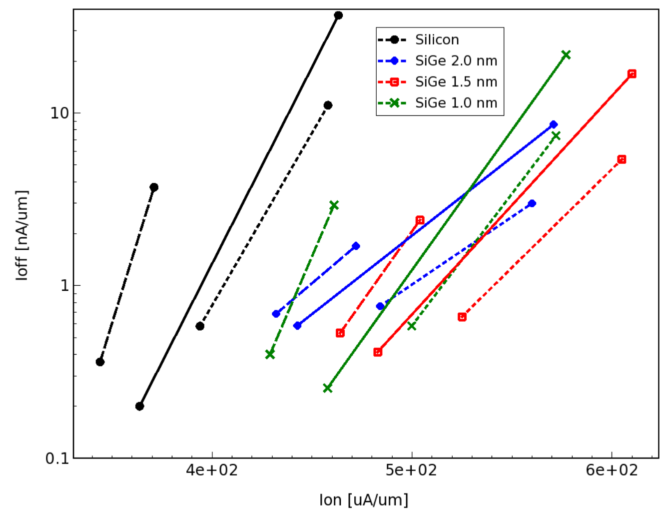

Fig. 7. Comparison of devices with 2 nm gate overlap (dotted curves), 2 nm gate underlap (dashed curves) and devices where the gate is aligned with the junctions (full curves). All three SiGe cladding options and the silicon reference are shown. The gate lengths for the aligned structures varies from 11 nm to 15 nm. For fixed off-current, the devices with 2 nm overlap yield the highest on-current.

formance of all devices considered here is the device with a 1.5 nm SiGe cladding layer and a gate overlap of 2 nm.

IV. Conclusion

We have benchmarked GAA-NWFETs with different SiGe cladding layer thicknesses against the silicon reference device. Low-field mobility is increasing with increasing cladding layer thickness and is outperforming silicon due to the lower transport mass, which is enhanced by the induced strain of the cladding. However, full device simulations indicate that subthreshold slope starts to degrade and the DIBL increases with increasing cladding thickness. We find that the optimal cladding thickness is around 1.5 nm, where the off-state behavior is still comparable to silicon and the on-current is about 35% higher. From the variation of the device structure we conclude that for fixed off-current, a 2 nm gate overlap yields the highest on-current for all cladding options considered here. From this study, we conclude that GAA-NWFETs with SiGe cladding can outperform their Si counterpart, but the dependence of the off-state behavior on the cladding thickness introduces new problems regarding variability.

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