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Comparison of Atomistic Quantum Transport and Numerical Device Simulation for Carbon Nanotube Field-effect Transistors

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***Abstract*—Carbon nanotube field-effect transistors (CNTFETs) are studied using atomistic quantum transport simulation and numerical device simulation. The studied CNTFETs consist of n-doped source- and drain-electrodes with an ideal wrap-around gate. Both the off- as well as the on-currents are described in very good agreement by both methods, which verifies the employed simplified approach in the numerical device simulation. The off-current is strongly dependent on interband tunneling in the studied CNTFETs. Thus, the good agreement between the methods verifies the tunneling model in the numerical device simulator, which can therefore be used to describe other tunneling devices, too. On the basis of the two methods we also discuss the effect of different channel lengths and aggressive gate scaling.**

I. Introduction

Carbon nanotube (CNT) based field-effect transistors (CNTFETs) are promising candidates as building blocks for future nanodevices. Thanks to their linear transfer characteristic, they are especially interesting for analog high-frequency applications [1]–[5].

Various device parameters can be altered in order to improve the performance of CNTFETs. Thus, simulations are essential to guide the device optimization. Numerical device simulation (NDS) and atomistic quantum transport simulation (AQS) are two available methods for such an optimization. The NDS is capable of describing large CNTFETs within an acceptable time for engineering purposes. It also allows to predict the high-frequency performance of CNTFETs as done in Ref. [3]. However, as NDS does not treat the CNTFETs at an electronic level, simple parameterized models are required to describe for example the band structure of the CNT. The physics near the contacts must be modeled very carefully in NDS as well [6], whereas it is basically automatically included in AQS [7].

The free parameters in NDS can be either obtained by fitting experimental reference data [3], [8], [9] or by calculating them directly using a more fundamental method, such as AQS. We use the latter approach. By doing so, we can critically test the core functionality of the NDS, which can be the base of future improvements of the NDS model towards a more physically correct description of CNTFETs.

In this publication we first describe the employed methods and present the simplified CNTFET used for our studies. Afterwards, the device characteristics are discussed. We then extend the study and investigate the impact of gate and channel length scaling.

II. Methods

A. Atomistic Quantum Transport Simulation

The AQS in this work is based on the non-equilibrium Green's functions formalism in combination with the extended Hückel theory as implemented in Atomistix ToolKit [10]–[13]. The typical setup for such a simulation consists of a central region and two semi-infinite leads, which we have applied here, too (see Fig. 1 and for example Ref. [14] for a more detailed description). The gate electrode is modeled by setting the potential to a fixed value. In the extended Hückel theory a set of parameters describes the shape of the orbitals and is used to construct the Hamilton operator. We apply a parameter set previously developed in our group to describe band structures of carbon nanotubes with density functional theory (DFT)-like accuracy [14], [15]. The Brillouin zone is sampled by 25 k-points in the transport direction and we used a density mesh cutoff of 10 Ha.

DFT calculations are performed for extracting the required parameters for the NDS. The density mesh cutoff for DFT calculations is set to 100 Ha, the chosen k-point sampling is $20 \times 1 \times 1$ and the wave functions are expanded in a DZP basis of SIESTA-type numerical atom-centered orbitals [12].

B. Numerical Device Simulation

The NDS is presented in detail in Ref. [9]. It solves the effective-mass Schrödinger equation and the Poisson equation self-consistently. For the band structure the first 4 subbands (2 conduction and 2 valence subbands) are considered in this study. The effective masses as well as the respective band

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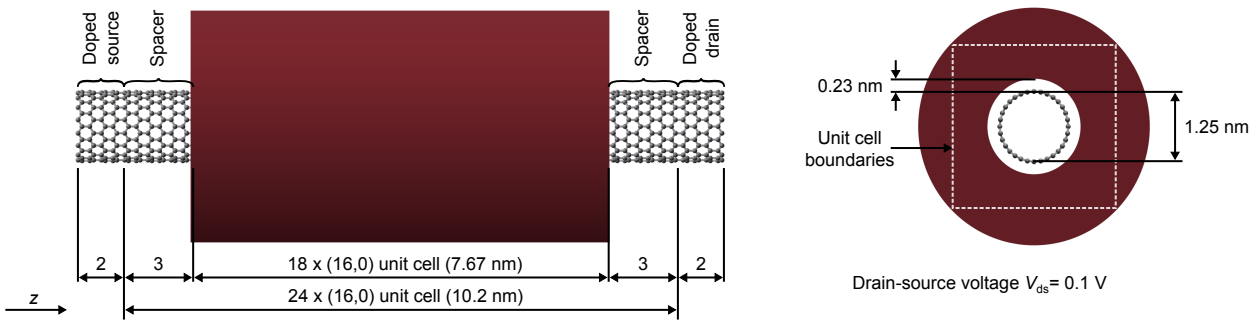

Fig. 1. CNTFET used in this work for the AQS (default setup; different gate lengths and channel lengths are studied). See the text for more details. No atoms are involved in the NDS, but the geometric parameters are identical.

gaps have been extracted from the DFT data. To model the contacts, certain energy ranges are defined where carriers can be injected into the channel. Both the band edges as well as the location of the band edges with respect to the Fermi energy are aligned in such as way that the band edges agree well with the calculated ones from AQS. The effective mass of injected carriers is set to the effective mass of valence or conduction band of the CNT, assuming that the doping does only shift the Fermi energy and does not alter the effective mass. A summary of the parameter used in the NDS can be found in Tab. I.

TABLE I
PARAMETERS EXTRACTED FROM DFT AND AQS TO DESCRIBE THE CNT AND THE CONTACT PHYSICS. m_0 IS THE ELECTRON REST MASS.

Band type	Band gap [eV]	Effective mass [m_0]
1st conduction band	0.30	0.06
2nd conduction band	0.62	0.26
1st valence band	0.30	0.06
2nd valence band	0.56	0.23
Band edge (n)	0.02 eV	
Band edge (p)	-0.58 eV	
Effective mass (n)	0.06 m_0	
Effective mass (p)	0.06 m_0	

III. Studied System

The studied CNTFETs consist of n-doped source- and drain-electrodes and a channel with a cylindrical wrap-around gate (see Fig. 1). This system is an idealized one, which is motivated by the fact that we are mainly interested in a comparison of the two computational methods. In the AQS, the artificial doping increases the number of electrons in each contact, which shifts the Fermi energy close to the conduction band edge. We have chosen a doping level of 0.05 electron per contact cell, which corresponds to an overall doping concentration of 5.86×10^{-9} electrons/cm. Both studied methods do not model any current flow between gate and CNT. Hence, there is no leakage current between gate and channel and it is sufficient to use only a vacuum padding between CNT and gate. This reduces the computational burden in the AQS, since fewer grid points are required when solving the Poisson equation (in contrast to NDS, no adaptive method was available for AQS). Of course, a thick dielectric should be considered for quantitative device studies, but we are mainly interested in a comparison of the employed models. The thickness of the vacuum is 0.23 nm, which corresponds to an equivalent oxide thickness of 0.9 nm. We use the (16,0) CNT as channel material, which has a diameter of 1.25 nm. Such CNTs are often used in experiments [16]. The dimensions along the transistor will be systematically changed later. As default values we have chosen a channel length of 10.2 nm and a gate length of 7.7 nm, which results in spacer regions of 1.3 nm length. The voltage between source and drain contact is set to 0.1 V.

IV. Results and Discussion

A. Transport Regimes

Before discussing the influence of different scaling schemes, the characteristics of the CNTFET with the default parameters are discussed. Fig. 2 shows the transfer characteristic calculated with NDS and AQS. The corresponding local density of states (from AQS) and transmission spectra (both methods) for three selected gate-source voltages is given in Fig. 3. The transistor shows clearly ambipolar behavior. Different regimes of operation can be classified in Fig. 2 and explained by looking at Fig. 3. For gate-source voltages $V_{\mathrm{gs}} > -0.1$ V, the transistor is in the on-state. States are available near the Fermi level, leading to a thermionic current. Applying a negative V_{gs}, the valence states are pushed to higher energies and the transistor is switched off. However, for $V_{\mathrm{gs}} < -1.2$ V, the current increases again due to interband tunneling, which is

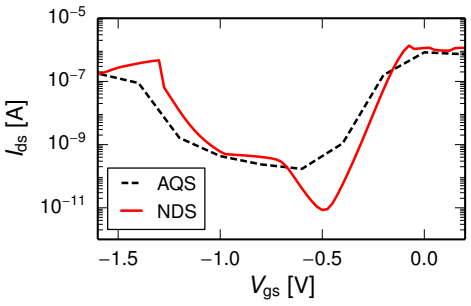

Fig. 2. Transfer characteristic of the studied CNTFET with default parameters.

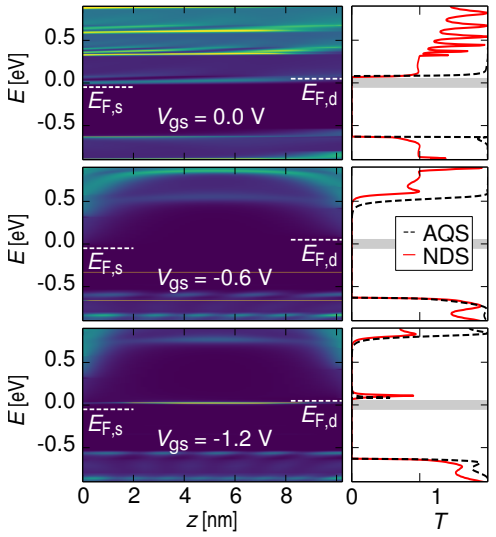

Fig. 3. Local density of states (dark: no states, bright: many states) calculated with AQS (left) and transmission calculated with both methods for different gate-source voltages V_{gs} (right). The Fermi energies of source and drain contact, $E_{\mathrm{F,s}}$ and $E_{\mathrm{F,d}}$, are marked as horizontal dashed lines (left) and are at the lower and upper bound of the grey area (right).

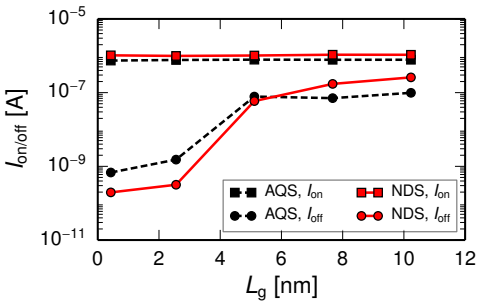

Fig. 4. On- and off-currents for a (16,0) CNTFET for different gate lengths L_{g}, calculated with AQS and NDS.

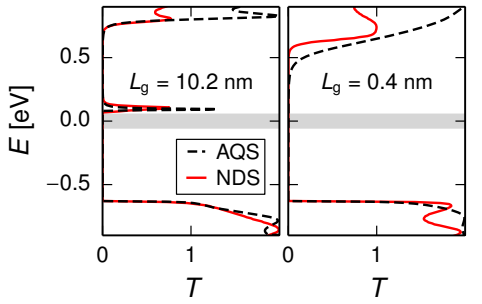

Fig. 5. Transmission spectra for two different gate lengths L_{g} at $V_{\mathrm{gs}} = -1.4$ V. The Fermi energies of source and drain contact, $E_{\mathrm{F,s}}$ and $E_{\mathrm{F,d}}$, are at the lower and upper bound of the grey area.

referred to as band-to-band tunneling (BTBT). This is also obvious from the transmission, where a peak above the Fermi energy of the drain contact is observed. In the local density of states, calculated with AQS, we see a localized state in the channel at the same energy. This state is available due to the high gate-source voltage, which shifts valence states to higher energies. But since the gate creates a potential well in the channel, only discrete states instead of a continuum are allowed.

Comparing NDS and AQS, a good agreement with respect to on- and off-current can be observed. This is an useful finding, since it shows that the NDS can be used to describe quantum mechanical tunneling effects in a reasonable way. Thus, the model is also suitable for transistors, where tunneling plays a crucial role, such as tunneling field effect transistors.

The CNTFET and especially our contact modeling is comparable with the AQS study in Ref. [17]. Very similar ambipolarity is observed there, which supports the validity of the employed models in the present work (quantitative deviations can be attributed to different device parameters in Ref. [17]).

Finally, we note that in the region between on- and off-current, a dip is present in the transfer characteristic from NDS, which is absent in AQS. We have found in our simulations that this dip depends on the electrostatics and thus depends on device geometry and contact modeling. As the contact modeling is the main difference between the two methods, future studies will concentrate on this aspect to explain it and to reach an even better agreement.

B. Aggressive Gate Scaling

NDS is often employed to describe the scaling of devices. Thus, we now vary the gate length L_{g} in a range between 0.4 nm and 10.2 nm and compare the results obtained by AQS and NDS. The channel length is fixed at 10.2 nm and so the spacer regions change accordingly between 4.9 nm and 0 nm.

To compare different gate lengths quantitatively, we define the on-current as the mean of all current values between $V_{\mathrm{gs}} = 0.0$ and $V_{\mathrm{gs}} = 0.5\ V$ (thermionic current). The mean of the current for gate-source voltages in the range between -2 and -1 V gives us the off-current (BTBT current), see also Fig. 2.

In Fig. 4 on- and off-currents for different gate lengths calculated with AQS and NDS are given. While the on-current is independent of the gate length, the off-current is reduced for gate lengths below 4 nm. Here, the ambipolarity (and hence the BTBT) is absent. This originates from the different spacer lengths between the gate and the contacts. For short spacers ($L_{\mathrm{g}} > 4$ nm), the band bending is much steeper between gate and contacts compared to large spacers. Only for short spacers the barriers are thus thin enough to allow interband tunneling. Therefore, by using large spacer, the ambipolarity can be suppressed and high on/off-ratios can be obtained. This technique is very promising to fulfill the ITRS 2026 specification, which is studied more extensively in Ref. [18], employing the same NDS model.

By comparing AQS and NDS, we find good agreement with respect to the calculated on- and off-currents for all gate lengths (see Fig. 4). The very good agreement in the off-currents shows that the BTBT is correctly described by the NDS model. This becomes even more clear from Fig. 5, where the transmission for the shortest and the longest gate at $V_{\mathrm{gs}} = -1.4\ V$ is presented. Above the Fermi energy of

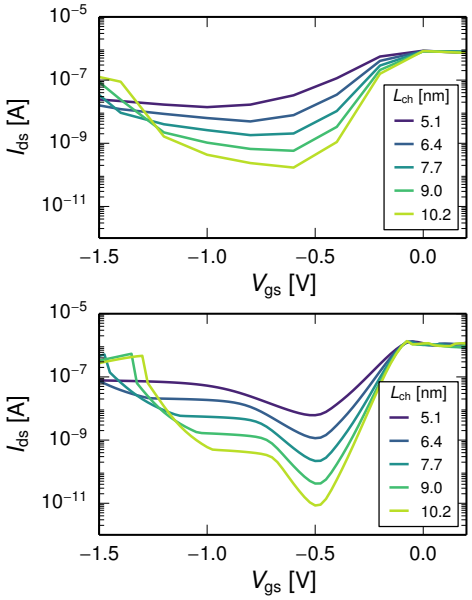

Fig. 6. Transfer characteristics for different channel lengths L_{ch}, calculated with AQS (top) and NDS (bottom).

the drain contact, a peak in the transmission is visible for $L_{\mathrm{g}} = 10.2$ nm. This is a result of BTBT. The shape and the location in energy of this peak is in good agreement between NDS and AQS.

C. Scaling of the Channel Length

In this section we show the impact of channel length variation with spacer lengths fixed at 1.28 nm to study its effect on BTBT. The length of the gate is changed accordingly.

In Fig. 6, the transfer characteristics for channel lengths ranging between 5 and 10 nm are shown. Very similar trends can be observed between both methods. The on-currents do not change with channel length, because both models are working in the ballistic regime. An increase in the current below -0.5 V is observed, which can be attributed to BTBT. For ultra-small channel lengths below 7 nm, no ambipolarity is observed and the intraband tunneling dominates the off-current. Besides the dip coming from the NDS calculation, which we have discussed earlier, the agreement between both models is apparent and again supports the validity of the tunneling model in the NDS.

V. Conclusions

Our comparison between the used AQS and the NDS models allows various conclusion. Both models show good agreement with respect to the calculated on-currents. Regarding the off-currents, caused by BTBT, a reasonable agreement can be found as well. Thus, we have verified the tunneling model in the NDS and have demonstrated that the studied NDS can be employed to describe transistors operating based on tunneling. Significant differences between both models were observed when the transistor is between on- and off-state. Future studies will focus on the deviations. Finally we have shown that the design of the spacer regions strongly influences the magnitude of the BTBT current, i.e. the BTBT can be suppressed by using larger spacers. This should be considered for future device optimizations of CNTFETs.

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