Optimization of Reconfigurable Si NW FETs for Analog High-Frequency Applications

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***Abstract*—Reconfigurable field effect transistors (RFETs) are attractive for analog applications exploiting their inherent switchability from n-type to p-type behavior. Simulation studies by means of an experimentally calibrated 3D numerical device simulator reveal that the recently proposed simplified single gate (SG) RFET architecture leads to a two times larger intrinsic transit frequency while providing the same DC device functionality and a significantly reduced wiring effort. The inferior high-frequency performance of DG RFETs can only be partially compensated by means of a significantly increased program gate voltage.**

***Index Terms*—RFET, Schottky Barrier FETs, Si Nanowire, Transit Frequency.**

I. Introduction

Reconfigurable Schottky barrier (SB) nanowire (NW) FETs are novel multifunctional devices for dynamically switching between n- and p-type behavior [1], [2], [3]. Reconfigurable FETs with a double gate (DG) [4] and triple gate (TG) [5] have been investigated by several authors [6]. Very recently a single gate (SG) device architecture has been proposed in [7] providing the same device functionality as DG RFETs while allowing less wiring and biasing overhead. RFETs have been studied intensively for digital applications while being also interesting for analog applications due to their inherent switchability.

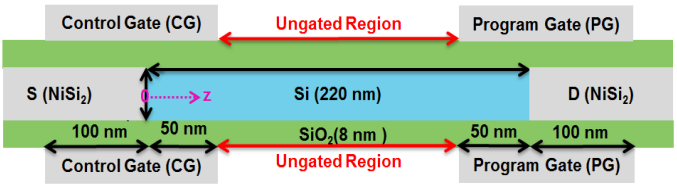
In this work we use experimental data for calibrating TCAD simulations. We address AC and DC performance of DG and SG RFETs and study the impact of the program gate voltage on the behavior of DG RFETs.

II. Structure and Device Simulations

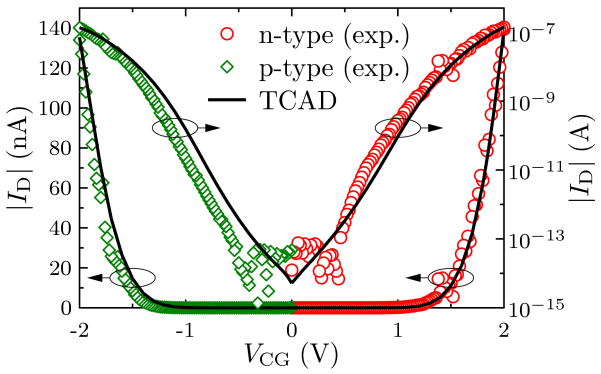
TCAD simulations based on the thermionic emission and tunneling currents at the source/channel/drain contacts and drift-diffusion transport along the channel have been used to study and analyze the high-frequency performance of DG RFETs and SG RFETs (see Fig. 1(a) and Fig. 2(a) for a schematic representation).

The simulation framework was calibrated to the experimental data [2] of DG RFETs (cf. Fig. 1(b)). Symmetric I-V characteristics for n- and p-type configuration have been achieved which is vital from an application point of view.

Fig. 2(b) shows a comparison between the same experimental data of the fabricated DG RFETs and the corresponding simulation results for a SG RFET considering identical dimensions, materials, parameters and physical models. Apparently, the device functionality in terms of reconfigurability and DC characteristics are not deteriorated by the simplification and structural change while allowing less wiring and biasing effort.



(a)



(b)

Fig. 1. (a) Schematic cross-section of the fabricated and simulated DG-RFET (b) transfer characteristics of the DG RFET. Data for p-type and n-type configuration is shown (experimental data (symbols) [2] and TCAD simulations (solid lines). Bias conditions for n-type: V_{DS} = V_{PG} = 2V and $V_{CG} > 0$V, for p-type: V_{DS} = V_{PG} = -2V and $V_{CG} < 0$V.

III. Results and Discusions

Fig. 3 shows the INTRINSIC transit frequency f_T (solid lines) of the DG RFET versus drain current at V_{DS} = 2V and two different program gate voltages V_{PG} of 2V and 4V. Obviously, the intrinsic transit frequency f_T increases with V_{PG} due to an increase of the electric field along the channel in the direction of drain current. In addition, the intrinsic transit frequency (dashed lines) of SG RFETs are shown. For

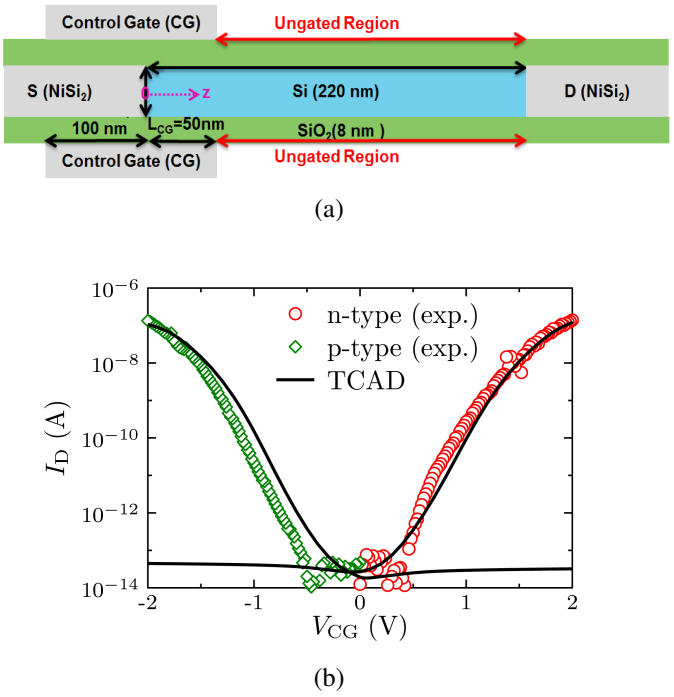


Fig. 2. (a) Schematic cross-section of the simulated SG-RFET (b) transfer characteristics of; data for p-type and n-type configuration is shown (experimental DG RFET data (symbols) [2] and TCAD simulations of SG RFET (solid lines). Bias conditions for ntype: V_{DS} = V_{PG} = 2V and $V_{CG} > 0$V, for p-type: V_{DS} = V_{PG} = -2V and $V_{CG} < 0$V.

the same channel length the studied SG RFET has a slightly smaller intrinsic f_T compared to the DG RFET.

A scaling of the channel length down to 170nm to match the length of the ungated region of the DG RFET allows to exploit the structural benefit of SG RFET in terms of speed (cf. Fig. 3 and Fig. 4) and smaller footprint. Reducing the channel length to 170nm causes an increase of the electric field particularly at the source contact. This leads to a thinner injection barrier there and thus to a higher tunneling probability, higher carrier injection and finally to an improved AC and DC performance (Fig. 4 and Fig. 5).

In terms of extrinsic f_T, the structural advantage of the SG RFET would be even more pronounced since the additional parasitic capacitances due to the program gate are avoided. The additional program gate in DG RFETs increases the parasitic capacitances and deteriorates the extrinsic f_T.

Fig. 4 shows the program gate voltage V_{PG} dependence of the intrinsic f_T of the DG RFET. While a large $V_{PG} \geq V_{DS}$ can partially compensate the structural induced deficiencies of the DG RFET, smaller program gate voltages further deteriote not only the high-frequency performance of the DG RFET but also DC performance (see Fig. 5).

Fig. 5 shows the influence and importance of V_{PG} on the I_{on}/I_{off} ratio of the DG RFET. For comparison, the I_{on}/I_{off} ratio of the SG RFET is also shown.

Decreasing V_{PG} ($V_{PG} < V_D$) deteriorates the device performance and demonstrates not only a worse AC behavior at ($V_{PG} < 2V$ (cf. Fig. 4) but also shows very poor DC characteristics

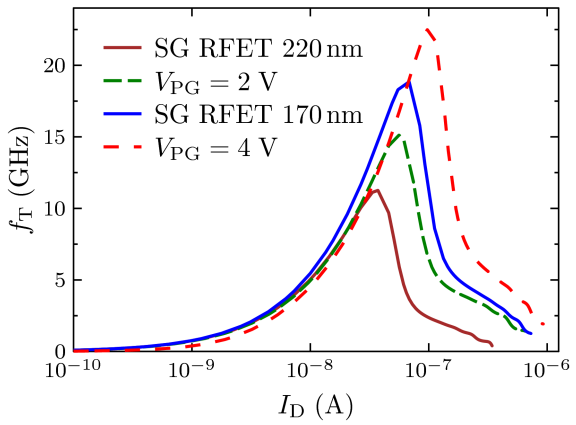


Fig. 3. Intrinsic transit frequency of DG RFETs (dashed lines) and SG RFETs (solid lines). Bias conditions: V_{DS} = 2V.

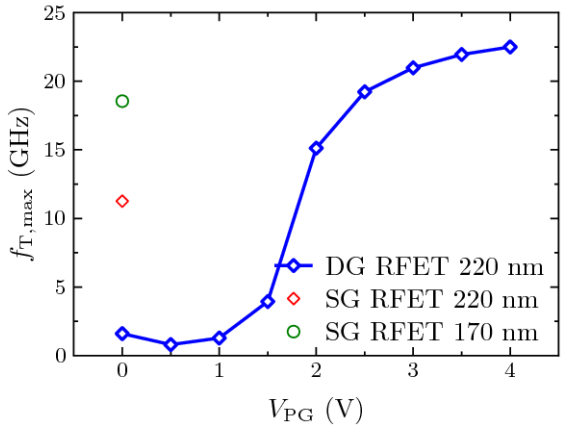


Fig. 4. Peak f_T versus V_{PG} of DG and SG RFETs at V_{DS} = 2V for different channel lengths (see legend).

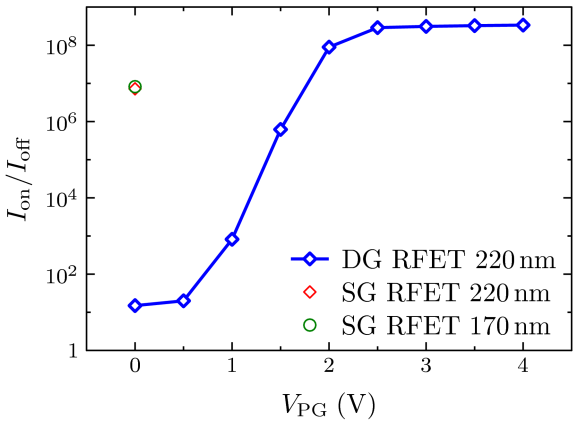
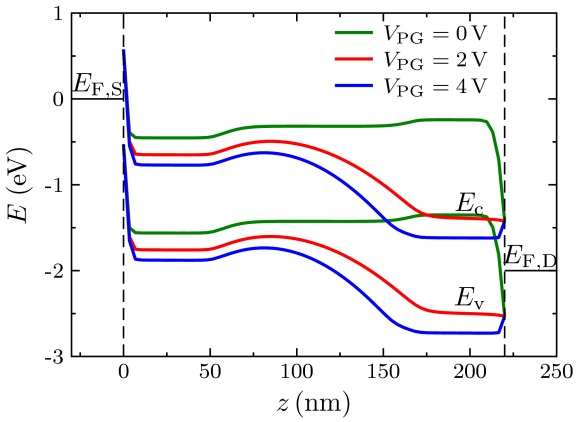


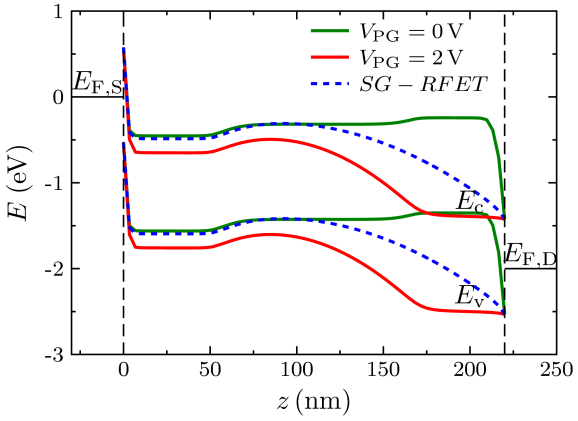
Fig. 5. I_{on}/I_{off} ratio of the DG RFET compared to a SG RFET with L_{ch} = 220 nm and L_{ch} = 170 nm (same length of ungated region compared to DG RFET). Bias conditions: V_S = 0V, V_D = 2V and V_{CG} = [0 4]V.

with I_{on}/I_{off} ratio (cf. Fig. 5) about 50 at $V_{PG} = 0V$.

A program gate voltage V_{PG} of 2V and 4V leads to a wide injection barrier for the holes at the drain contact, which



(a) DG RFET



(b) DG and SG RFETs

Fig. 6. The band diagram of (a) DG RFET with different program gate bias V_{PG} and (b) DG RFET with V_{PG} = 0V and 2V compared to SG RFET.

blocks hole injection from the drain side. This is not only the reason for a high I_{on}/I_{off} ratio in Fig. 5 but also for a better AC performance (cf. Fig. 4). However, a lower program gate voltage V_{PG} of 0V leads to a thinner injection barrier at the drain contact (cf Fig. 6(a)) and increases the carrier injection from drain side and decreases significantly the I_{on}/I_{off} ratio.

Fig. 6(b) visualizes the band diagram of a DG RFET at $V_{PG} = 0V$ and $V_{PG} = 2V$ together with the band diagram of the SG RFET. If one compares the DG RFET characteristics at $V_{PG} = 2V$ with the characteristics of the SG RFET, a slightly wider barrier (cf. Fig. 6(b)) of the DG RFET at the drain side leads for a slightly better f_T (see Fig. 4) and I_{on}/I_{off} ratio (see Fig. 5) which it is mainly the influence of an additional V_{PG}. Considering the SG RFET with $L_{ch} = 170\,nm$, a larger electric field at the source side of the channel due to a shorter channel length improves (see Fig. 4) the SG RFET compared to the DG RFET at $V_{PG} = 2V$.

In Fig. 7, the dependence of the output characteristics of the DG RFET on V_{PG} is shown and compared to those of the SG RFET with $L_{ch} = 220\,nm$ and $L_{ch} = 170\,nm$. Obviously, the lower the program gate voltage, the smaller is the saturation current and the smaller is the onset voltage for the sharp current increase due to the intrinsic ambipolarity of the channel material.

The saturation of the current for large V_{DS} is limited by the source Schottky barrier rather than a channel pinch-off, as known for conventional MOSFETs. The saturation current in SB FETs is associated to the source Schottky barrier height and width.

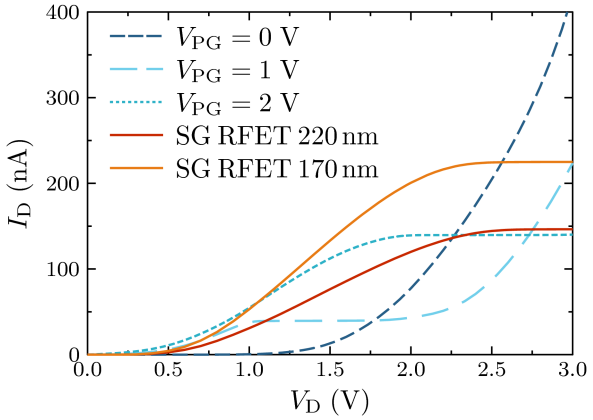


Fig. 7. Output characteristics of the DG RFET (dashed lines) for different V_{PG} and of the SG RFET at $V_{CG} = 2V$.

IV. Conclusions

A small-signal analysis of DG and SG RFETs has been carried out to evaluate the performance of these devices based on calibrated TCAD simulation.

The influence of V_{PG} on f_T and I_{on}/I_{off} of DG RFETs has been illustrated and compared with those obtained from SG RFETs without a program gate. It has been shown that the f_T and I_{on}/I_{off} ratio of DG RFETs increases with V_{PG} due to an increase of the electric field in the entire channel in particular at the drain contact.

The simplified SG RFET with $L_{ch} = 170\,nm$ without a program gate shows higher f_T and I_{on}/I_{off} ratio (better DC and AC performance) compared to the counterpart DG RFETs.

The V_{PG} in DG RFETs should be higher or at least equal to V_D ($V_{PG} \geq V_D$) in order to have a high f_T and I_{on}/I_{off} ratio, otherwise DC and AC performance would be extremely deteriorated. The inferior behavior can only partially be compensated by a significantly increased program gate voltage but at the cost of increased wiring and bias complexity.

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REFERENCES

[1] W. Weber, A. Heinzig, J. Trommer, D. Martin, M. Grube and T. Mikolajick, "Reconfigurable nanowire electronics–A review", Solid-State Electronics, Elsevier, Vol. 102, pp. 12-24, 2014.

[2] A. Heinzig, S. Slesazeck, F. Kreupl, T. Mikolajick and W. M. Weber, "Reconfigurable silicon nanowire transistors", Nano letters, ACS Publications, Vol. 12, No. 1, pp. 119-124, 2011.

[3] M. De Marchi, D. Sacchetto, S. Frache, J. Zhang, P.-E. Gaillardon, Y. Leblebici and G. De Micheli, "Polarity control in double-gate, gate-all-around vertically stacked silicon nanowire FETs", Electron Devices Meeting (IEDM), 2012 IEEE International, pp. 8.4.1-8.4.4, 2012.

[4] A. Heinzig, T. Mikolajick, J. Trommer, D. Grimm and W. M. Weber, "Dually Active Silicon Nanowire Transistors and Circuits with Equal Electron and Hole Transport", Nano letters, ACS Publications, Vol. 13, No. 9, pp. 4176-4181, 2013.

[5] M. De Marchi, J. Zhang, S. Frache, D. Sacchetto, P.-E. Gaillardon, Y. Leblebici and G. De Micheli, "Configurable logic gates using polarity-controlled silicon nanowire gate-all-around FETs", Electron Device Letters, IEEE, IEEE, Vol. 35, No. 8, pp. 880-882, 2014.

[6] J. Trommer, A. Heinzig, T. Baldauf, S. Slesazeck, T. Mikolajick and W. M. Weber, "Functionality-enhanced logic gate design enabled by symmetrical reconfigurable silicon nanowire transistors", Nanotechnology, IEEE Transactions on, IEEE, Vol. 14, No. 4, pp. 689-698, 2015.

[7] G. Darbandy, M. Claus and M. Schroter, "High-Performance Reconfigurable Si Nanowire Field-Effect Transistor based on Simplified Device Design", IEEE Transactions on Nanotechnology, IEEE, Vol. 15, pp. 289 - 294, 2016.