Impact of cross–section of 10.4 nm gate length $In_{0.53}Ga_{0.47}As$ FinFETs on metal grain variability

N. Seoane*, G. Indalecio* and A.J. García-Loureiro*†
*Centro Singular de Investigación en Tecnoloxías da Información
† Departamento de Electrónica e Computación
University of Santiago de Compostela
15782 Santiago de Compostela, Spain
Email: natalia.seoane@usc.es

K. Kalna
Electronic Systems Design Centre
College of Engineering, Swansea University
Swansea SA2 8PP, United Kingdom

***Abstract*—The sub–threshold region variability due to TiN metal grain work–function induced fluctuations in a 10.4 nm gate length $In_{0.53}Ga_{0.47}As$ FinFET is analysed for three different cross–section shapes (rectangular, triangular and bullet–like), using an in–house 3D Finite–Element Density–Gradient Quantum–Corrected Drift–Diffusion device simulation tool.**

The I_D–V_G characteristics in the sub–threshold region have been compared for the three cross–section shapes. The device with more triangular cross–section results in lower off–current, drain–induced–barrier–lowering (DIBL) and sub–threshold slope values. However, the cross–section shape has a very small influence on a metal grain work–function induced variability in the threshold voltage with differences of only 4% between the different device shapes. We also present a new approach, based on the creation of Gate Sensitivity Region Maps, to evaluate the sensitivity of the different regions of a semiconductor device to the metal grain work–function induced variability.

I. Introduction

High–mobility III–V semiconductors are being intensively researched for some time as a Si replacement in the n–channel multi–gate CMOS of future 10 nm or 7 nm technology [1], [2], due to their higher electron mobility and saturation velocity. If the high–mobility semiconductors are going to be used in the channel of future nanoscale transistors, the effect that random intrinsic parameter fluctuations on the device can become more pronounced when the spatial scales of these fluctuations begin to be comparable to the device dimensions. Metal gate work–function (MGW) variations, line–edge roughness (LER) and random dopant (RD) fluctuations are examples of major contributors to the device variability [2], [3] affecting their performance in circuits.

In this paper, we study the impact of the cross–section shape of a 10.4 nm gate length $In_{0.53}Ga_{0.47}As$ FinFET on the TiN metal gate work–function (MGW) induced variability using a 3D finite–element (FE) density–gradient quantum–corrected drift–diffusion simulator. This simulation technique is based on a tetrahedral discretisation of the simulation domain via the FE method which provides an accurate description of the three–dimensional geometry of state–of–the–art multi-gate nano–devices affected by fabrication process. The study of the MGW induced variability only is carried out despite of the existence of other sources of device variability like the LER and the RD because the MGW variability is considered to be a major source affecting device performance of nanoscale high–mobility n-type multi-gate transistors [2], [3].

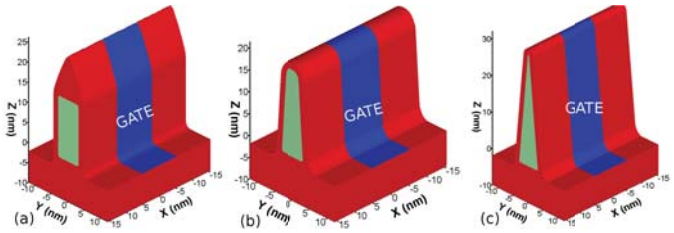

Fig. 1. Schematics of the 10.4 nm gate length (a) rectangular-, (b) bullet- and (c) triangular-shaped channel $In_{0.53}Ga_{0.47}As$ FinFETs. Dimensions and parameters are summarised in Tables I and II.

TABLE I
Device dimensions and parameters that remain fixed for the three shapes of the $In_{0.53}Ga_{0.47}As$ FinFET.

L_G (nm)	10.4	Physical gate length
EOT (nm)	0.59	Equivalent oxide thickness
W_{fin} (nm)	6.1	Fin width
L_{SD} (nm)	10.4	Length of n-doped S/D regions
N_c (cm^{-3})	10^{17}	p-type channel doping
N_{SD} (cm^{-3})	5x10^{19}	Peak value S/D doping
WF (eV)	4.72	Work-function
Area (nm^2)	92-93	Cross-sectional area of the channel

The structure of the paper is as follows. Section II describes the structure of the FinFET device and the main features of the simulation technique employed in the study. Section III presents the implementation of the metal grains and discusses the sub–threshold region MGW variability results, and Section IV summarises the main conclusions of this work.

II. Simulation Methodology

We have simulated three shapes of the FinFETs to investigate the impact that the cross–section shape has on the MGW variability . Initially, we have considered two accurately described (by FEs) cross–sections, a rectangular–like shape

978-1-5090-0818-6/16/$31.00 ©2016 IEEE

TABLE II
FIN HEIGHT, OFF–CURRENT, THRESHOLD VOLTAGE, SUB–THRESHOLD SLOPE AND DRAIN–INDUCED–BARRIER–LOWERING FOR THE THREE SIMULATED $In_{0.53}Ga_{0.47}As$ FINFETS.

	Rectangular	Bullet	Triangular
H_{fin} (nm)	15.2	19.9	30.3
I_{OFF} (nA)	5.19	3.38	1.87
V_{Tsat} (V)	0.186	0.199	0.216
SS (mV/dec)	79.1	78.1	61.3
DIBL (mV/V)	75.5	67.2	67.3

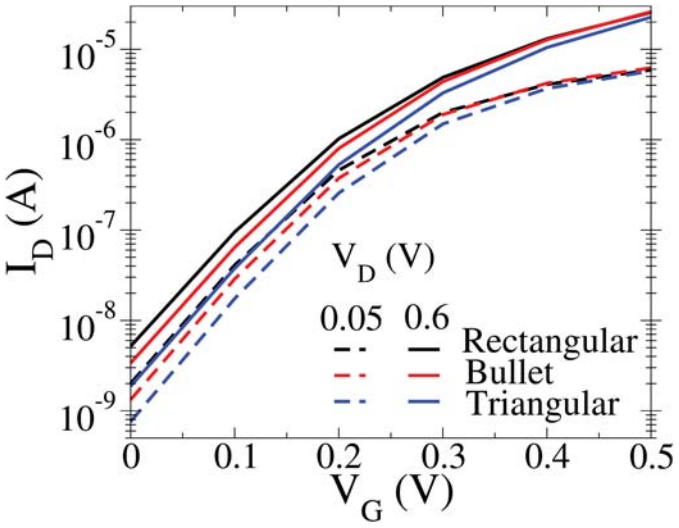

Fig. 2. Sub–threshold region I_D–V_G curves at both low and high drain biases for three cross–section shapes (rectangular, bullet and triangular) of the 10.4 nm gate length InGaAs FinFET.

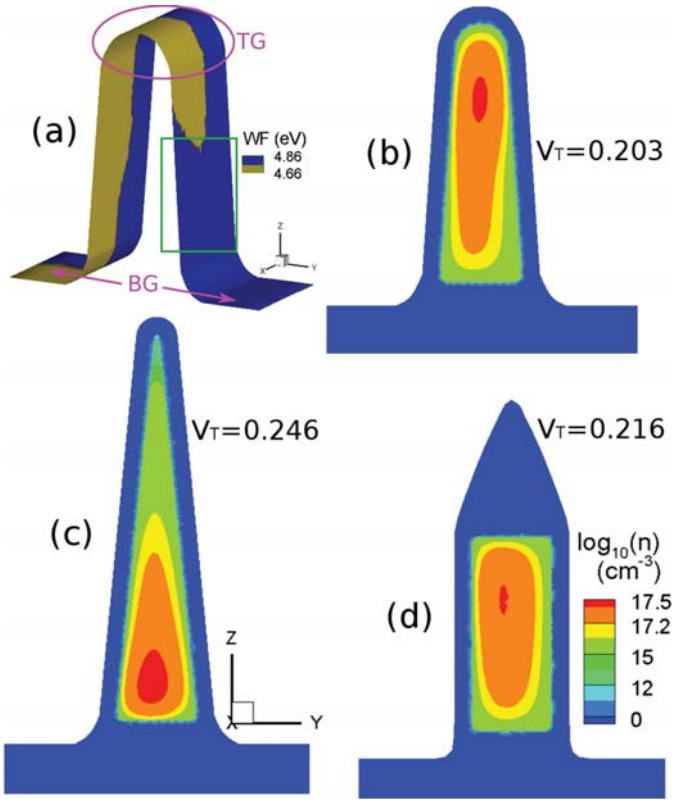

Fig. 3. (a) Example of a MGW profile (with GS=7 nm) applied to the TiN metal gate. Electron density cross–section in the middle of the gate of the FinFET for the same profile with (b) bullet, (c) triangular or (d) rectangular shape at V_G=V_T and V_D=0.6 V. V_T values for each shape are also shown.

(see Fig. 1a) [4] and a bullet–like shape (see Fig. 1b) [5], that have been modelled following the appropriate scaling of experimental devices [6]. We have also considered a third extreme cross–section shape: triangular–like (see Fig. 1c). The design of the 10.4 nm gate length InGaAs FinFET follows the 2013 ITRS [7] predictions for HP logic III–V multi–gate devices. The main device dimensions and doping parameters are shown in Table I. These devices have Gaussian n–type doping in the source/drain regions and an uniform p–type doping in the channel. The three device structures have the same: i) gate length, ii) fin width and iii) cross–sectional area but a different fin height (as seen in Table II).

The devices are modelled using an in–house built 3D finite element (FE) quantum–corrected drift–diffusion (DD) device simulator [3] capable of accurately reproduce the shape of the transistor. The quantum corrections have been included in the simulation via the FE density gradient approach (DG) described in [8].

Fig. 2 shows the I_D–V_G characteristics of the 10.4 nm gate length InGaAs FinFET in the sub–threshold region for the three cross–section shapes. I–V characteristics of the FinFET with a rectangular cross–section were calibrated at both low (0.05 V) and high drain biases (0.6 V) against 3D ballistic NEGF simulations coming from Silvaco [9] with an excellent agreement [3]. The device with a triangular cross–section shows a reduced off–current and DIBL and a nearly ideal sub–threshold slope (SS) (as shown in Table II) indicating a better gate control which makes it more suitable for digital applications. Note that the larger fin height in the triangular cross–section device will be more challenging for process fabrication.

III. SIMULATION RESULTS

To simulate the TiN metal grains, we have followed the methodology described in Ref. [10], which is based on the creation of Poisson Voronoi Diagrams (PVD). The PVD is an accurate method to generate the gate metal grains since it is able to capture the shape of the domains that grow from randomly located nucleation points as seen in real fabrication process [11]. We have generated an ensemble of 300 devices, each with a different MGW distribution and an average grain size (GS) of 7 nm.

Fig. 3a shows an example of a TiN MGW distribution due to its variability. TiN has two possible grain orientations with work–functions (WFs) spanning 0.2 eV [12]. For the same distribution of grains, Figs. 3(b)-(d) show the electron density

in the middle of the gate ($X = 0$) for the three cross–sections. In the triangular (TRI) device, the density is distributed toward the bottom of the cross–section and is low at the narrow top due to stronger quantum mechanical confinement. However, in the rectangular (REC) and bullet (BUL) shaped devices, although the density is distributed along the entire channel, the larger values are found at the top of the cross–section. Grains with a larger WF value are occupying a significant part of the gate profile's right–hand side (see the green rectangle in Fig. 3(a)), which is pushing the electron density to the opposite side of the device (see Figs. 3(b)-(d)). Moreover, V_T is lower for the BUL cross–section, which is due to a larger control at the top of the gate (TG) in this configuration.

To illustrate this, Fig. 4 shows 2D gate sensitivity region (GSR) profiles for the three cross–section shapes allowing to determine how sensible the V_T of a device is to the work–function value that appears on the different parts of the gate. The top of the gate (TG) and the bottom of the gate (BG) are indicated in the figure. In the TRI and REC cross–section devices, the grains present in the sidewall region of the gate are the most influential. Note that, in the REC device there is a thick layer of oxide (of 11 nm) over the channel (see Fig. 1a), whereas for the other two cross–sections this layer is reduced to less than 2 nm. However, in the BUL device, the TG and its vicinity are the most sensitive regions to the WF variations. Independently of the cross–section shape, the sensitivity is larger at the source end of the gate than at the drain end, as seen in the bottom figures of Fig. 4, where the 1D aggregated gate sensitivity along the transport direction is shown.

Fig. 5 shows a scatter plot of V_T from the rectangular (top figure) and triangular (bottom figure) cross–section shapes against V_T from the bullet shape due to MGW variability. The standard deviations of distributions (σV_T) and the Pearson correlation coefficient between the magnitudes (PCC) are also presented. The three cross–section devices show a very similar V_T spread (of around 32 mV) with differences of only 4%, even when the correlation between them is relatively small, which indicate a good immunity of the MGW variability to the cross–section shape.

Fig. 6 represents the normal Quantile–Quantile (Q–Q) plot of the DIBL distribution due to MGW for the three cross–section shapes. Clearly, unlike the V_T fluctuations, there is an impact of the cross–section shape on the DIBL variability. The REC device is more resilient with a σ_{DIBL} to be 40% lower than those of the BUL and TRI cross–sections, although its mean DIBL value is larger that those of the BUL and TRI channel shapes.

IV. Conclusion

In this paper, we have presented a simulation study of the impact that the cross–section shape has on the TiN metal gate workfunction variability in a 10.4 nm gate length $In_{0.53}Ga_0.47As$ FinFET [2] in the sub-threshold region using in-house 3D FE density–gradient quantum–corrected drift–diffusion [8]. Three cross–section shapes (rectangular, triangular and bullet–like), which might result from a fabrication process at nanoscale, were precisely modelled by the FE method following the appropriate scaling of experimental devices, when available.

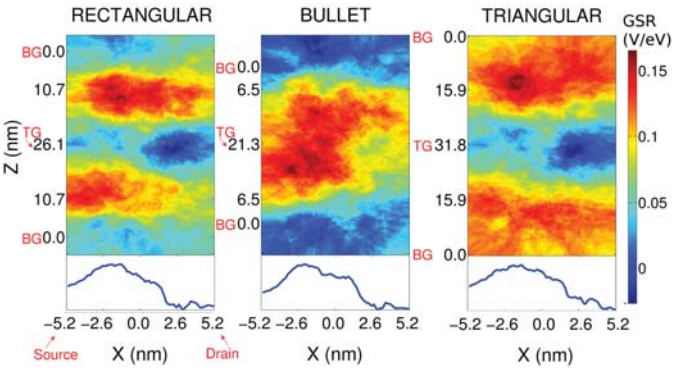

Fig. 4. 2D gate sensitivity profiles for V_T for the three cross–section shapes (top) and 1D aggregated gate sensitivity along the transport direction (bottom). The top of the gate (TG) and the bottom of the gate (BG) regions are indicated in the figure. The results have been obtained at a low drain bias of 0.05 mV.

We have shown that non–rectangular devices have a better gate control, presenting reduced off-current, DIBL and SS values. However, the cross–section shape has not much impact on the V_T MGW variability, with differences of only 4% between the different cross–sections. In order to understand this immunity of the MGW variability to the shape of the channel, we have also introduced a new approach to assess the sensitivity of the different regions of the gate of a semiconductor device to the metal grain variability. This technique, which is based on the creation of a Gate Sensitivity Region Map, demonstrated that there is a very little correlation in the variability results coming from the different cross–section devices. This is quite positive message for the development of future sub-10 nm technology nodes which will allow for larger variations to be accommodated in the cross-section shapes which are affected by the LER during the fabrication process.

Acknowledgment

This work was supported by the Spanish Government and FEDER funds under Grant TEC2014–59402–JIN and Grant TIN2013–41129–P, and in part by the Engineering and Physical Sciences Research Council under Grant EP/I010084/1. Authors would like to thank CESGA for the access granted to their computing facilities.

References

[1] N. Waldron, C. Merckling, W. Guo et al., "An InGaAs/InP quantum well finfet using the replacement fin process integrated in an RMG flow on 300mm Si substrates", *Symp. VLSI Technol. Dig. Tech. Pap.*, pp. 32–33, 2014.

[2] N. Seoane, G. Indalecio, E. Comesana, M. Aldegunde, A. J. Garcia–Loureiro, and K. Kalna, "Random Dopant, Line–Edge Roughness, and Gate Workfunction Variability in a Nano InGaAs FinFET", *IEEE Trans. Electron Devices*, vol. 61, no. 2, pp. 466–472, 2014.

[3] N. Seoane, G. Indalecio, M. Aldegunde, D. Nagy, M. A. Elmessary, A. Garcia–Loureiro and K. Kalna, "Comparison of Fin–Edge Roughness and Metal Grain Work Function Variability in InGaAs and Si FinFETs", *IEEE Trans. Electron Devices*, vol. 63, no. 3, pp. 1209–1216, 2016.

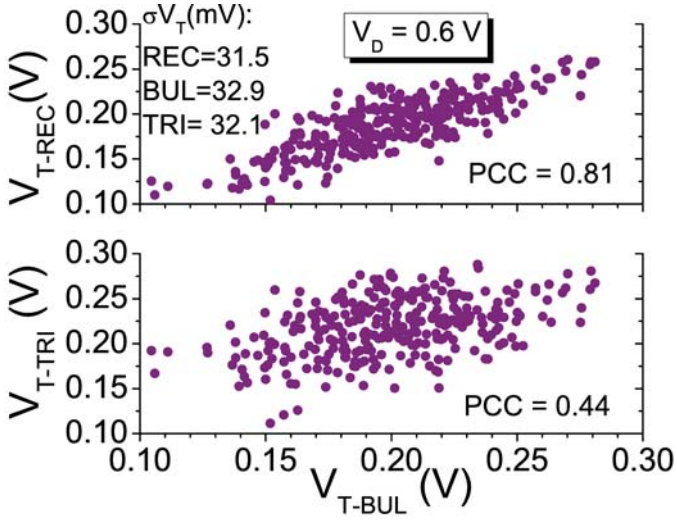

Fig. 5. Scatter plots of V_T from the rectangular (REC) and triangular (TRI) shapes vs. V_T from the bullet (BUL) shape due to MGW variations. σV_T and Pearson correlation coefficient (PCC) are shown for comparison.

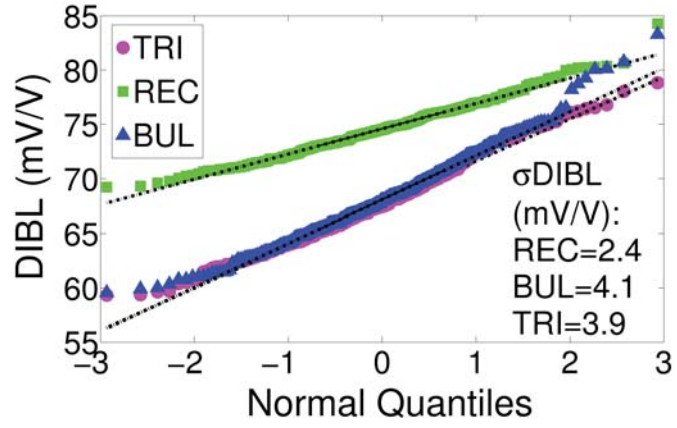

Fig. 6. Q–Q plot for DIBL due to MGW variability for the three cross–sections (REC, BUL, TRI). σDIBL for the three device shapes is also shown for comparison.

[4] V. S. Basker, T. Standaert, H. Kawasaki et al., "A 0.063 μm^2 FinFET SRAM cell demonstration with conventional lithography using a novel integration scheme with aggressively scaled fin and gate pitch", *Symp. VLSI Technol. Dig. Tech. Pap.*, pp. 19–20, 2010.

[5] G. Patton, "Evolution and expansion of SOI in VLSI technologies: Planar to 3D, *IEEE International SOI Conference*, pp. 1–40, 2012.

[6] M. Aldegunde, A. J. García–Loureiro, and K. Kalna, "3D Finite Element Monte Carlo Simulations of Multigate Nanoscale Transistors", *IEEE Trans. Electron Devices*, vol. 60, no. 5, pp. 1561–1567, May 2013.

[7] Int. Technology Roadmap for Semiconductors, 2013. Available at: http://www.itrs2.net/

[8] A. J. Garcia–Loureiro, N. Seoane, M. Aldegunde, R. Valin, A. Asenov, A. Martinez and K. Kalna, "Implementation of the density gradient quantum corrections for 3D simulations of multigate nanoscaled transistors", *IEEE Trans. Comput–Aided Des. Integr. Circuits Syst.*, vol. 30, no. 6, pp. 841–851, 2011.

[9] ATLAS Users Manual, Silvaco Inc., pp.13–4, 2012

[10] G. Indalecio, M. Aldegunde, N. Seoane, K. Kalna and A. J. Garcia–Loureiro, "Statistical study of the influence of LER and MGG in SOI MOSFET", *Semicond. Sci. Technol.*, vol. 29, p. 045005 (7pp), 2014.

[11] G. Indalecio, A. Garcia–Loureiro, N. Seoane and K. Kalna, "Study of Metal–Gate Work–Function Variation Using Voronoi Cells: Comparison of Rayleigh and Gamma Distributions", *IEEE Trans. Electron Devices*, vol. 63, no. 6, pp. 2625–2628, 2016.

[12] H. F. Dadgour, K. Endo, V. K. De, and K. Banerjee, "Grain– orientation induced work function variation in nanoscale metal–gate transistorsPart I: Modeling, analysis, and experimental validation", *IEEE Trans. Electron Devices*, vol. 57, no. 10, pp. 2504–2514, Oct. 2010.