Simulation of Silicon-Dot-Based Single-Electron Memory Devices

F. J. Klüpfel, A. Burenkov, J. Lorenz
Fraunhofer Institute for Integrated Systems and Device Technology IISB
Erlangen, Germany
fabian.kluepfel@iisb.fraunhofer.de

***Abstract*—Electrical properties of silicon-dot-based single-electron memory devices were investigated using numerical simulation. For an accurate calculation of tridimensional electron wave functions in the dots and in the dot-isolation surrounding the nextnano++ simulator was employed. Tunneling rates between the dot and other electrodes were calculated using a post-processing of the electron-state-specific wave functions on the dots and in the electrical contacts. The charge state of the dots was evaluated using the master equation approach. The simulation model was verified by a comparison of simulated and measured charge state life times in a prototype of a single-electron memory device.**

Keywords—quantum dot; single electron memory; numerical simulation; tunneling rate; charge state

I. Introduction

Silicon dots in a silicon dioxide matrix behave in respect to electrons like artificial atoms and the discrete states of these atoms can be used for information storage. A dot can bind some electrons or holes and because the charge carriers are localized on the dot, due to their wave-nature, the energy of such electrons or holes is quantized in certain energy levels. These electronic states can be filled or emptied by means of tunneling between the dot and other electrodes which are isolated from the dot by the silicon dioxide, but are located close enough to allow tunneling from or to the dot, if an appropriate voltage is applied. If the size of the silicon dots is of a few nanometers, the capacitance of such a dot is so small that if one electron comes to the dot or leaves the dot the electrostatic potential on the dot changes significantly and can easily be registered in an electrical measurement. This way, the one-electron charge can be used as the counting unit in the memory device.

The fabrication of silicon quantum dots (QD) in a silica matrix has been demonstrated using plasma enhanced chemical vapor deposition of Si dots with subsequent oxide deposition [1] or ion implantation of silicon into an oxide layer [2,3]. The formation of such dots is assisted by phase separation during thermal treatment [4]. QD based memory cells have been realized by the introduction of single dots in the gate insulator of MOSFETs. For a change of the QD charge by one electron, threshold voltage shifts in the order of 0.1 V have been reported [5,6]. Besides the possibility to detect the dot charge, the lifetime of the dot charge in comparison to writing and erase times is of importance for the memory cell operation. Charge lifetimes between few seconds [5] and and years [6] have been reported for tunneling oxides t_{tunnel} between 2 nm and 7 nm, respectively.

Hinds et al. [5] describe the observed electron life times theoretically with an one-dimensional model. However, they do not discuss the amount of charge actually present on the dot after charging. Due to Coulomb interaction the number of electrons on the dot N_e must have a significant impact on the tunneling rates. Furthermore, the description in [5] only focusses on discharging of electrons already on the dot. We argue, that both charging and discharging rates must be considered for the description of a memory device. We employ tridimensional quantum mechanical simulations with nextnano++ [7] for a correct description of the energetic structure of the QD, supported by device simulations using Sentaurus TCAD software [8]. Tunneling rates were calculated from nextnano wave functions following the formalism presented by Sée *et al.* [9].

II. Device Layout and Electrostatics

A prototype of a QD memory cell is schematically presented in Fig. 1. The device is an NMOS transistor based on a p-Silicon substrate with an acceptor concentration of 4×10^{17} cm^{-3}. The QD with diameter d_{dot} is separated from the substrate by an oxide layer with thickness t_{tunnel}, which was 3 nm for our simulations when not mentioned otherwise. The total thickness of the gate insulator was t_{ox} = 50 nm + t_{tunnel}, following the

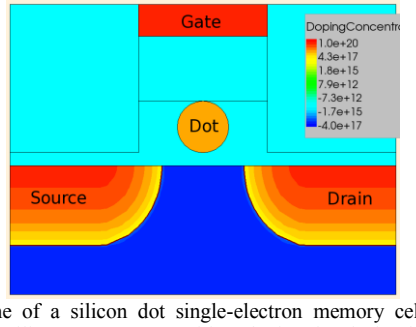

Fig. 1. Scheme of a silicon dot single-electron memory cell with doping distributions in silicon. n-type – positive doping levels in the source/drain doped regions, p-type – negative doping levels in the silicon body. Doping concentration is shown in cm^{-3}.

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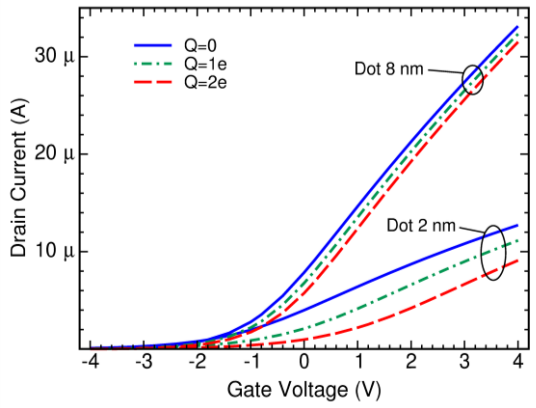

Fig. 2: Impact of the dot-charge state (charge on the dot Q=0, one electron, and two electrons) on the drain current at a drain voltage of 0.1 V of the MOSFET structure envisaged for the memory-cell-state reading for silicon dot diameters of 2 and 8 nm, respectively.

structure described by Hinds et al. [5]. This setup ensures, that only tunneling between channel and QD is relevant. Tunneling between gate and QD can be neglected due to the large distance. A temperature of 300 K was used for the nextnano simulations and the tunneling rate calculations.

Writing to the memory device is conducted at a suitably high positive gate voltage, which will allow electrons to tunnel from the channel to the QD. Likewise, a low gate voltage will promote tunneling from the dot to the channel and erase the stored charge. An intermediate gate voltage is applied while reading the QD charge state. This voltage should be chosen in a way that both erased and charged states are preserved as long as possible. Criteria to choose these voltages in an optimum way are discussed at the end of this paper.

The drain current of the MOSFET is used to read out the stored charge. Since the charge-state-dependent voltage on the dot induces a charge-dependent voltage on the surface of the semiconductor, the source-drain current in the MOSFET is sensitive to the charge state of the dot. The target for optimization should be low power operation while retaining reliable readout of the charge state. Thus, a change of the charge state by single electrons should lead to a maximum change of the source-drain current at a minimum absolute current value. Fig. 2 shows the simulated drain current of the MOSFET for different dot sizes and charge states. Lower gate voltages lead to lower currents while the voltage shift induced by the dot charge is approximately independent on the gate voltage. This indicates, that low gate voltages are favorable for reading of the stored information. However, as described in the following, the gate voltage has a strong influence on the charge lifetime. For a maximum charge holding time, the gate voltage during reading must be at a certain value determined by the tunneling time constants. Hence, the optimization of the MOSFET characteristics should be conducted after the storage of charges on the QD is characterized. When the optimum gate bias for maximum storage times has been determined, the MOSFET should be designed such as to minimize the drain current for this gate voltage.

The electrostatics of the device can be understood from the capacitances between the dot and the surroundings, most prominently gate electrode and channel/substrate. We

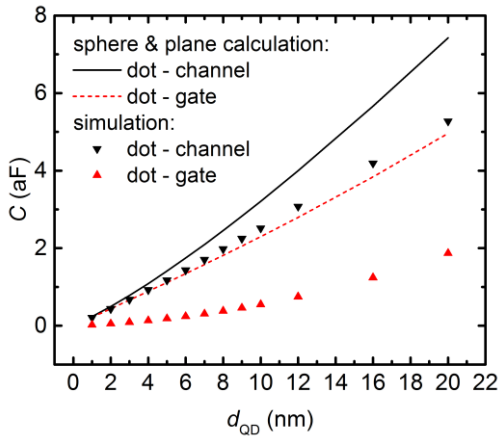

Fig. 3: 3D numerically simulated capacitances between the dot and gate and substrate electrodes in comparison to an analytical description of a conducting sphere and an infinite plane electrode.

calculated capacitance values with Sentaurus, using a model with cylindrical symmetry where the dot is located between the planar aluminum gate and the silicon substrate. With Sentaurus two different contact types can be used for the dot, either a contact which applies a constant voltage (V-contact) or a floating contact which carries a certain charge Q but does not fix the electrostatic potential (Q-contact). Because the dot consists of undoped silicon and hence is no equipotential region, the dot should not be modelled with a V-contact. We used a Q-contact to simulate different dot charge states Q and evaluated the average change of the electrical potential V_{dot}. The total dot capacitance is given by $C_{dot}=Q/\Delta V_{dot}=C_{DG}+C_{DC}$ with the dot-gate capacitance C_{DG} and dot-channel capacitance C_{DC}. Considering the series connection of C_{DG} and C_{DC} in forming the gate-channel capacitance, the relation to the respective voltages at total dot charge Q=0 is given by

$$C_{DG}/C_{DC} = V_{DC}/V_{DG}. \quad (1)$$

In Fig. 3 we compare C_{DG} and C_{DC} in dependence on the dot diameter to analytical calculations of the capacitance between a metallic sphere and an infinite plane. It can be seen, that the simulated values are significantly lower, partly due to the finite size of the electrodes and partly due to the non-metallic dot. Thus, an accurate treatment by numerical simulation is necessary to avoid large errors in the device characteristics derived from the capacitances. Additionally we investigated the influence of quantum corrections in the TCAD simulations. Using the density gradient model resulted in slightly lower capacitances, but the relative change was for all dot sizes below 2%. We conclude, that quantum corrections can be neglected when calculating capacitances for the presented device.

The filling of the dot with electrons is governed by the Coulomb blockade. A simple model for the energy necessary to add an electron to the dot charge is given by $\Delta E=e^2/C_{dot}$, which corresponds to a voltage $\Delta V_{DC}=\Delta E/e$ between channel and dot. Using (1), the total gate-channel voltage $V_{GC}=V_{DC}+V_{DG}$ is determined by $V_{GC} = V_{DC}(C_{DG}+C_{DC})/C_{DG} = V_{DC}C_{dot}/C_{DG}$. Hence, to change the dot charge by one electron a gate-channel voltage change of $\Delta V_{GC}=e/C_{DG}$ is necessary. For dots with diameter of 4 nm, 6 nm and 8 nm we obtain a ΔV_{GC} of 1.2 V, 0.66 V, and 0.42 V, respectively.

III. Electron Tunneling and Lifetimes

While the charging energy can be described by electrostatics as described above, the calculation of such important quantities like tunneling rates and life times demands a quantum mechanical description of the system. This is due to the fact, that the electrons on the dot occupy quantized states which couple individually to the electrodes. We employed the quantum simulator nextnano in order to obtain tridimensional electron wave functions for the quantum dot in an electrical field. Nextnano does not provide a Q-contact in order to simulate different charge states. However, the charge state of the dot can be modelled by using a contact type which sets the Fermi energy on the dot but does not fix the potential (Fermi-contact). A model for the description of a system with a quantum dot and tunneling to two planar electrodes has been described by Sée *et al.* [9]. They derive an analytical expression for the electrode wave functions and use Bardeen's formula for the calculation of tunneling rates $\Gamma_{C\to D}$ to the dot and $\Gamma_{D\to C}$ from the dot. Subsequently, the occupation probabilities $P(N)$ for the individual charge states N are calculated by a master equation formalism:

$$0 = P(N)\,(\Gamma_{D\to C}(N) + \Gamma_{C\to D}(N)) \qquad (2)$$
$$- P(N+1)\,\Gamma_{D\to C}(N+1) - P(N-1)\,\Gamma_{C\to D}(N-1)$$

The probabilities $P(N)$ determine the equilibrium charge state distribution in a dot at a certain bias. The average charge on the dot can be expressed as weighted sum $N_e = \sum N\,P(N)$. The lifetime for a charge state is given by

$$\tau = 1/\,|\,\Gamma_{D\to C}(N) - \Gamma_{C\to D}(N)|. \qquad (3)$$

A one-dimensional profile of the conduction band edge along the vertical axis through QD and Si channel is presented in Fig. 4, together with ground state energy and wave function. The quantities are shown for a gate bias of 6 V and for four different charge states N_e. It can be seen, that additional electrons on the dot increase both the band edge and the ground state energy in the dot. For a certain dot charge, the energy level becomes higher than the channel conduction band edge, prohibiting the charging with additional electron. This illustrates graphically the equilibrium occupation of the QD

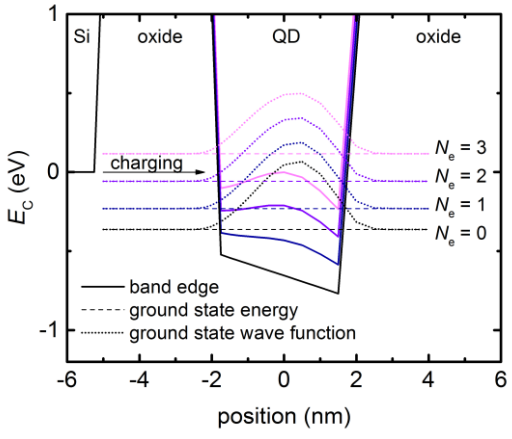

Fig. 4: Conduction band edge and ground state in a 4 nm dot at 6 V bias for different charge states N_e. The substrate/oxide interface is at -5 nm, the arrow indicates tunneling from the substrate to the dot. Only charge states with energy below the substrate band edge can receive an additional electron.

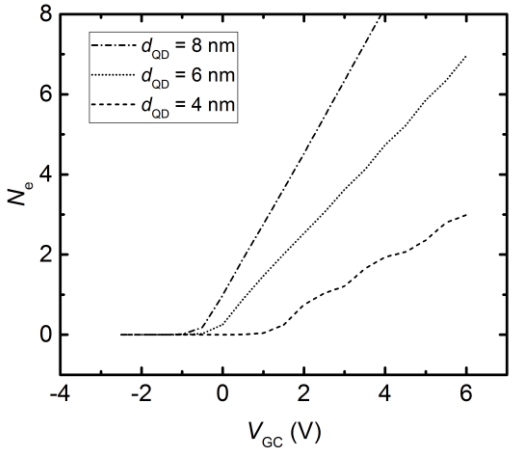

Fig. 5: Equilibrium charge state for different dot sizes dependent on the gate-channel bias voltage. The step-like appearance for low diameters is due to the larger spacing between energy levels for smaller dots.

at a certain bias voltage. The average charge on the dot in dependence on the bias calculated with the master equation formalism are shown in Fig. 5. For smaller dots the energy levels have a larger spacing, which leads to step-like features in the curves. From the derivative of the shown characteristics we can calculate the voltage ΔV_{GC} necessary to change the dot charge by one electron. For dots with diameter of 4 nm, 6 nm and 8 nm we obtain 1.6 V, 0.91 V, and 0.56 V, respectively. These values are in the same order as those calculated from the capacitances above. The difference of about 30% could is largely due to depletion/accumulation of the silicon channel, which was respected in the Sentaurus simulations but not within the nextnano model.

The lifetime of electrons on the dot was investigated by Hinds *et al.* [5] after charging at V_{GC} = 6 V. We calculated the equilibrium charge state at 6 V for d_{dot} of 3 nm, 4 nm, 6 nm, and 8 nm and obtained 1, 3, 7, and 12 electrons, respectively (compare Fig. 5). We calculated the tunneling rates from dot to channel at different bias voltages for an initial condition obtained from the equilibrium charge state at 6 V. The results are compared to the experimental values in Fig. 6. We obtained the best agreement for d_{dot} = 3 nm and t_{tunnel} = 3 nm, while [5] reported d_{dot} = 8 nm and t_{tunnel} = 2 nm. However, a natural oxide with thickness up to 1.5 nm around the QD was reported

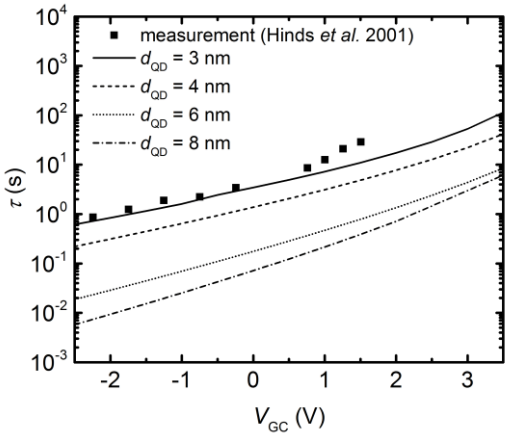

Fig. 6: Calculated electron lifetimes after charging at 6 V in comparison to experimental values by Hinds *et al.* [5].

for similarly prepared dots [1]. This would lead to effective values of reported d_{dot} = 5 nm and t_{tunnel} = 3.5 nm, which is in better agreement with our results.

The lifetime after charging as depicted in Fig. 6 is only one benchmark criterion for the operation of a memory cell. Of similar importance is the lifetime of a state with low charge (erased state) at reading voltage, in order to enable the device to memorize at least two states, e.g. logical zero and one. The lifetimes of charge states from N_e = 0 up to N_e = 5 are shown in Fig. 7 in dependence on the gate-channel voltage. Discharging curves are smooth, because the tunneling target is the continuous distribution of unoccupied states in the channel conduction band. For charging, the channel conduction band must align energetically with one of the discrete dot levels for maximum tunneling rates. Thus the charging curves appear as wavy lines. Note, that the curves for charging and discharging of a certain initial state never overlap. The lifetimes diverge at the voltage where the respective charge state is stable under equilibrium conditions (cmp. Fig. 5). For operation as memory cell, we must consider at least two different charge states which represent the information stored in the cell. In order to store this information sufficiently long, a gate voltage must be found which maximizes the storage time for both states simultaneously. From Fig. 7 suitable candidates can be determined at crossings between charging and discharging time constants. One such crossing, close to V_{GC} = 0 V, is marked in Fig. 7 by a circle. At this point, both states N_e = 0 and N_e = 1 have time constants above 1000 s, which seems to be the maximum storage time achievable with the geometry in this example. Another possibility would be V_{GC} = 1 V, where the states N_e = 1 and N_e = 2 have maximum mutual stability.

In order to achieve longer lifetimes, it is possible to increase the thickness t_{ox} of the tunneling barrier. Our simulations show, that each nanometer of t_{ox} increases the time constants up to five orders of magnitude. However, it must be noted that charging and discharging times increase by the same factor as the storage time. For memory operation the difference between charging/discharging times and storage time is decisive. Fig. 7 shows that the discharging times can be easily

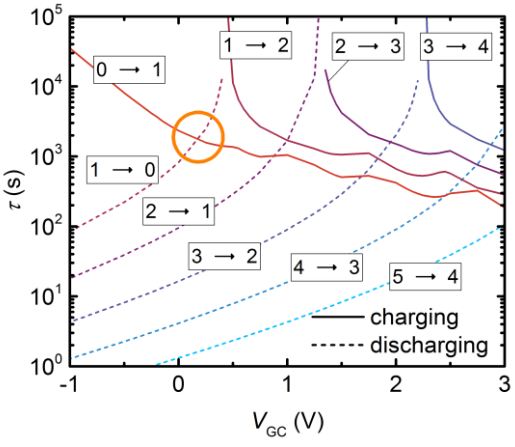

Fig. 7: Charging and discharging time constants for a dot diameter of 6 nm and a tunneling oxide thickness of 3 nm. Each line stands for a certain transition, the respective electron numbers are shown in the figure next to each line. The circle denotes the position, where states N_e = 0 and N_e = 1 have their maximum mutual lifetime.

decreased about 3 orders of magnitude compared to the storage time by lowering the gate voltage below 0 V. For charging the situation is less favorable, as the time constants drop much slower when increasing the gate voltage. An increase of 4 V reduces the lifetimes only by a factor of about 10. This is due to the fact, that a negative gate bias shifts the maximum probability density of the electron states on the dot in the direction of the channel, while a positive gate bias increases the effective distance for tunneling. A possible solution is to decrease the dot size, which reduces the bias dependence of tunneling rates.

IV. Summary

We investigated a memory device based on silicon quantum dots. Electrostatic simulations using Sentaurus TCAD were applied to calculate capacitances which are related to the energy necessary for charging the dot with electrons. For the calculation of tunneling rates and lifetimes we applied numerical tridimensional quantum mechanical simulations with nextnano++. Simulated life times were compared to experimental results and are in a reasonable agreement within the measurement uncertainties. The simulations point out that for smaller dot diameters a change of the dot charge leads to a larger change of the MOSFET drain current and hence can be better distinguished by the reading circuit. Furthermore, the charge state can be controlled more precisely in comparison to larger dots where the energy levels are more dense. Thus, smaller dots are favorable for single-electron operation. The suitability of the proposed device for memory application was discussed by investigation of charging and discharging time constants and charging holding time. Especially for the enlargement of the ratio between holding time and charging time further improvements of the single electron memory devices are necessary.

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