Compact Modeling of Power Devices Embedded in Advanced Low-Power CMOS Circuits

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***Abstract*— A compact model for power devices with advanced technology is developed which considers the geometry dependent potential distribution along the device explicitly. The model solves key potential nodes within the device iteratively to realize accurate modeling of the underlap, which occurs in HV\MOSFETs, as well as of the non-monotonous potential-distribution region. With use of the developed model it is verified that the suppression of the switching loss can be done by optimizing the device geometry, because all geometry parameters are explicitly considered in this modeling.**

Keywords—compact model; embedded high-power MOSFET, low-power CMOS circuits; potential distribution, switching loss

I. Introduction

Our investigation focusses on the development of a compact model for embedded high-voltage (HV) MOSFETs in low power circuits with advanced technologies. Important integration requirements are, that the HV-MOSFETs must sustain high applied voltage, realize small power loss and reduced size penalty at the same time. These requirements make device optimization, including the circuit-level considerations, necessary. For this purpose, compact model development reflecting the device-structure features is a prerequisite. Consequently, we aim at compact modeling with applicability to any structural variation, analyze three typical HV-MOSFET structures, and develop a universal model, which is applicable to any kind of HV-MOSFET structure optimization. Using this universal model, we demonstrate that the power loss is determined by the carrier dynamics within the device, and that the reduction of leakage currents is the key to realize reduced power loss for embedded HV-MOSFETs.

HV-MOSFET integration architectures in CMOS circuits are mainly driven by the need for optimized utilization of the core low-power CMOS technology [1]. For example, an embedded HV-MOSFET structure with an ultra-thin body and buried-oxide SOI technology has been proposed [2]. The main task for developing embedded power-device structures is the reduction of the maximum field peak to achieve high breakdown voltage under the constraint of small device area. Additionally, the switching loss must be suppressed as much as possible. Consequently, the reported investigation achievement is a predictive compact model for accurate simulation of power sub-circuits characteristics, embedded in advanced CMOS circuits, under any structural HV-MOSFET variation.

II. 2D-Device Simulation Study

The conventional scaled CMOS technology is applied here as the base technology for studying the optimization scheme of the embedded power device to focus on modeling of the highly resistive part. However, the developed model can be applied for any other CMOS-base technology. 2D numerical device simulation has been utilized for studying effects caused by structural features [3]. The three analyzed HV-MOSFET structures are depicted in Fig. 1a. Device A is a conventional MOSFET structure. Devices B and C use laterally and vertically extended drain contacts, respectively. The I_{ds}-V_{ds} characteristics are compared in Fig. 1b. The breakdown voltage is efficiently increased by extending the resistive region and the highest resistivity is realized with Device C. Namely, Device C is the most attractive structure for high-breakdown purposes.

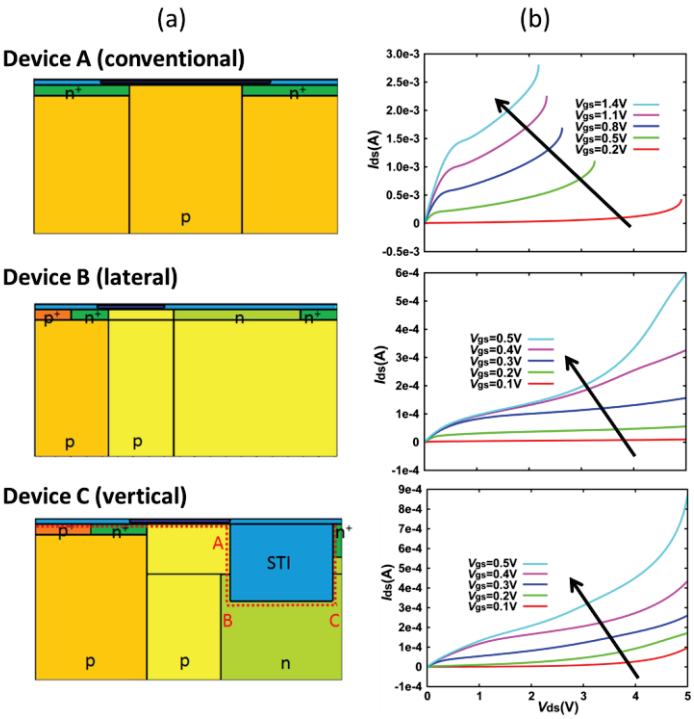

Fig. 1. (a) Studied three device structures, where total length of the resistive region is the same for Devices B and C, and (b) corresponding I_{ds}-V_{ds} characteristics.

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The internal potential distributions along the device surface are compared in Fig. 2 for Devices B and C, together with electron concentration and mobility. The lateral Device B shows a monotonous potential increase, resulting in a smooth distribution of the electron density as well as the mobility within the resistive region. On the contrary, a specific feature of the vertical Device C is the step like potential increase towards the drain contact. The non-monotonous potential distribution results in drastically-varying physical quantities as shown in Figs. 2b and c. This step like plateau also causes nearly bias independent carrier density and mobility between points B and C. This results in carrier relaxation from the high field stress. However, the length of the plateau reduces with increased V_{ds}. If the plateau disappears, the potential increase cannot be absorbed any more, and the high field effect becomes obvious as seen in Fig. 1b of the current increase.

Fig. 3a compares the switching performance of the two devices. The circuit used for the simulation is depicted in Fig. 3b. The lowest power loss is achieved with Device B at V_{DD}=3V as shown in Table 1. The reason for the higher power loss of Device C is mainly because of the tail current after V_{gs} is switched off. Fig. 4 shows logarithmic plots of the I_{ds}- V_{gs} characteristics. An obvious feature of Device C is the strong leakage current in the subthreshold region, which prevents fast switching as is observed in Fig. 3. Therefore, reduction of the subthreshold leakage current is necessary for device optimization.

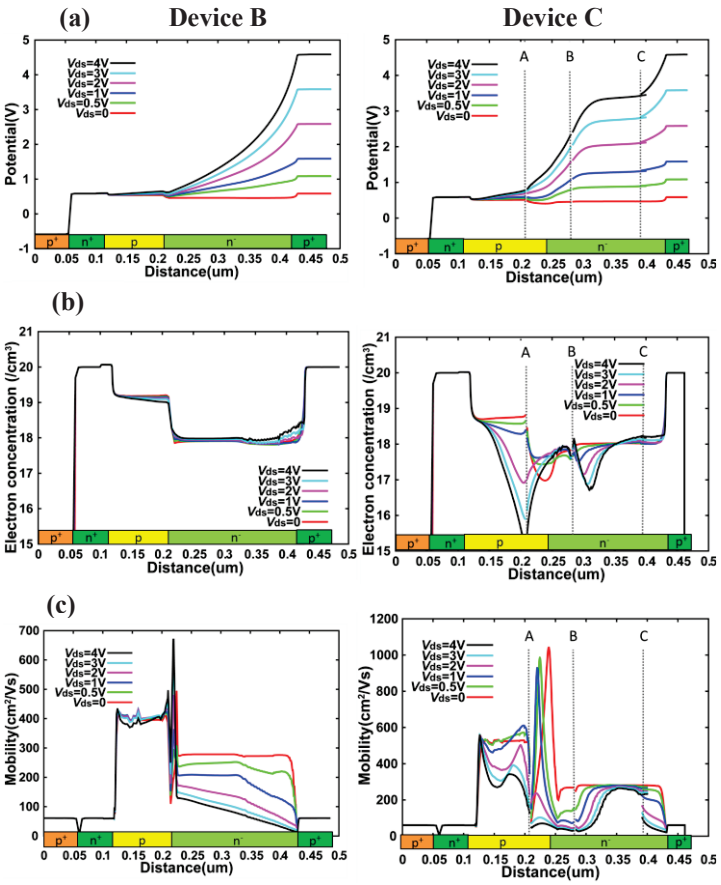

Fig. 2. 2D-device simulation results, (a) Potential distribution within Device B and Device C, (b) corresponding electron concentration, and (c) mobility along the device.

The reason for the strong leakage current is attributed to the direct current flow from the source to the drift region as depicted in Fig. 5. This leakage current increases the subthreshold current as V_{ds} increases, resulting in the loss of V_{gs} control. By reducing the leakage current the power loss can be reduced as depicted in Fig. 6. An interesting feature of Device C is that the current gathers at the point B (see Fig. 1) despite of the wide current distribution flowing from the source. Thus it is concluded that device-geometry optimization is possible to minimize the leakage current. To prevent the leakage current flow, device optimization is analyzed among structural parameters such as channel length, channel depth, and n^- width. The impurity concentrations are also important parameters to be optimized together. Fig. 7 summarizes the important structural parameters for explicit consideration in compact modeling, with Device B defined as a special case of Device C.

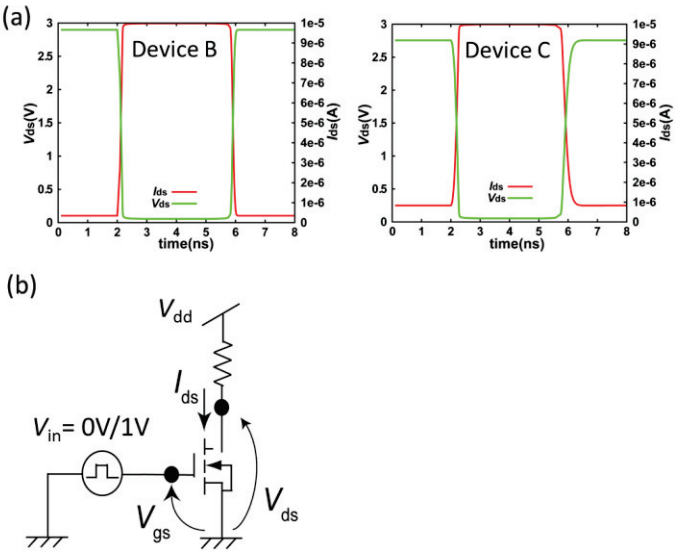

Fig. 3. 2D-device simulation results of (a) switching performances for Device B and Device C at V_{cc}=3V, (b) circuit used for the simulation.

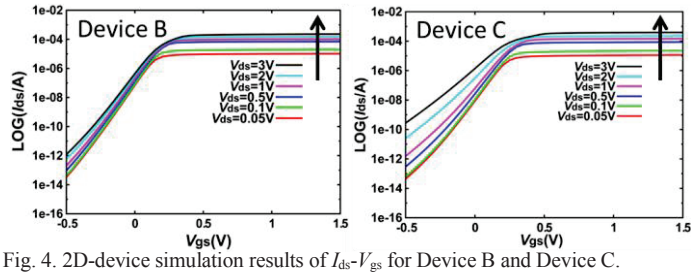

Fig. 4. 2D-device simulation results of I_{ds}-V_{gs} for Device B and Device C.

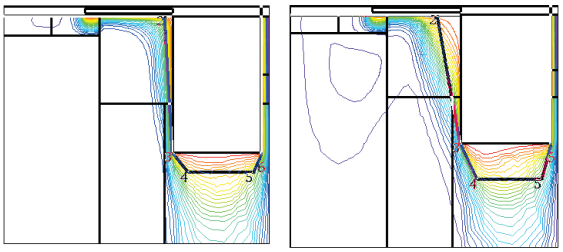

Fig. 5. 2D-device simulation results of current path in Device C, at V_{ds}=0.5V (left side) and at 3V (right side) with V_{gs}=0.5V.

Table 1. Simulated switching loss for studied structures at V_{DD}=3V and V_{gs} swept from 0 to 1V.

	Switching loss
Device A	4.43fW
Device B	2.32fW
Device C	4.42fW

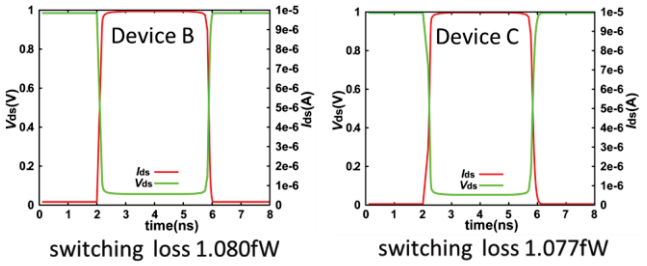

Fig. 6. 2D-device simulation results of switching performance for Device B and Device C for V_{cc}=1V, where no leakage current is seen.

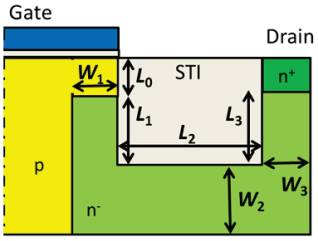

Fig. 7. Geometrical parameters of Device C considered in modeling. Device B refers the case L_1= L_3=0.

III. Compact Model Development

For modeling of structural features, the total potential distribution along the device must be calculated correctly, namely, the potential values at points A, B, and C in Fig. 8 must be accurately calculated. Therefore, the path resistance is divided into three parts, as also schematically shown in Fig. 8, which refer the potential drops between A-B and B-C, C-Drain. As obvious from Fig. 2, the potential drop occurs mostly along STI of the left side (between A and B). However, Fig. 5, indicates that the current flow is not along the device surface, but flows deep into the substrate, gathers at point B and diverges again along the bottom of STI. The current density distribution underneath the STI is the same as that of Device B within the resistive region. This concludes, that the current governed by V_{gs} is switched to the current governed by V_{ds} at B. Thus, the important potential node to accurately solve for modeling the general high-voltage MOSFET structure is node B.

The HiSIM_HV modeling approach is followed for accurate modeling of the potential distribution. The currents in the channel region, governed by V_{gs}, and in the resistive region, governed by V_{ds}, must be equal along the device, especially at point B. Thus the node potential at B is solved iteratively to preserve the current continuity within the channel part and the resistive part. The channel current is written as [4]

$$I_{ds} = \frac{W_{eff}}{L_{eff}} \cdot \mu \cdot \frac{I_{dd}}{\beta} \tag{1}$$

$$I_{dd} = C_{ox}\left(\beta V_G{}'+1\right)\left(\phi_{SL}-\phi_{S0}\right) - \frac{\beta}{2}C_{ox}\left(\phi_{SL}^2-\phi_{S0}^2\right) - \frac{2}{3}const0\left[\left\{\beta\left(\phi_{SL}-V_{bs}\right)-1\right\}^{\frac{3}{2}} - \left\{\beta\left(\phi_{S0}-V_{bs}\right)-1\right\}^{\frac{3}{2}}\right] + const0\left[\left\{\beta\left(\phi_{SL}-V_{bs}\right)-1\right\}^{\frac{1}{2}} - \left\{\beta\left(\phi_{S0}-V_{bs}\right)-1\right\}^{\frac{1}{2}}\right]$$

where the surface potential values ϕ_{S0} and ϕ_{SL} at the source side and at the end of the gate oxide, respectively, are obtained by solving the Poisson equation under the V_{gs} stress. The current I_{ds} is a function of the node potential at B in comparison to ϕ_{SL}.

The difference of Device C in comparison to the conventional MOSFET is the non-overlapped part in the channel region. This underlap means practically that there is no gate control in spite of the channel p region. Modeling of the underlap region is done with the channel-length-modulation model [3]. The pinch-off region is controlled mostly by the lateral electric field, namely by the field induced by V_{ds} at the position B for the studied case. The pinch-off region is written as a function of the surface potentials at the source side and the drain side. The model is extended to represent the phenomenon within the fixed length of L_0, shown in Fig. 7. Due to the weakened gate control, the I_{ds}-V_{ds} characteristic shows no clear saturation behavior, but increases gradually, as actually observed in Device C. This is a typical HV-MOSFET characteristics, well modeled in HiSIM_HV [5].

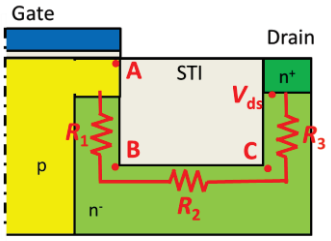

Fig. 8. Modeling-concept explanation, where underlap and 2D effect are considered as pinch-off and resistance network, respectively.

The current I_{res} between points B and C is written as

$$I_{res} = W_{eff,LD} \cdot X_{ov} \cdot q \cdot N_{drift} \cdot \mu_{drift} \frac{V_{BC}}{L_{drift} + RDRDL1} \tag{2}$$

where $W_{eff,LD}$, N_{drift}, and μ_{drift} are channel width, impurity concentration, and mobility of the resistive drift region, respectively. X_{ov} denotes the current width entering into the drift region, which refers to W_1 modified by V_{gs}. The length *RDRDL1* is a model parameter describing the extended current path due to the expansion deep into the substrate. The elementary charge is denoted by q. Two of the three resistances (see Fig. 8) are connected in series and modeled independently as

$$I_{\text{res}} = \frac{V_{\text{BC}}}{R_2 + R_3} \tag{3}$$

where

$$R_2 = \rho \frac{L_2}{S_2} = \rho \frac{L_2}{W_2 \cdot W_{\text{eff,LD}}} \tag{4}$$

$$R_3 = \rho \frac{L_3}{S_3} = \rho \frac{L_3}{W_3 \cdot W_{\text{eff,LD}}} \tag{5}$$

The volume resistivity ρ is written as

$$\rho = \left(q \cdot N_{\text{drift}} \cdot \mu_{\text{drift}}\right)^{-1} \tag{6}$$

IV. Comparison with Measurements

The device optimization has been carried out to achieve the best performance on the basic circuit level with Device C for V_{DD}=5V. Fig. 9 compares calculation results of the *I-V* characteristics, obtained with the developed model, to measurements. It is seen, that the leakage current is well suppressed by the device optimization, and that agreements are satisfactory. The switching performance is additionally demonstrated in Fig. 10. It is seen, that the switching loss is reduced by the optimization from 4.42fW to 3.92fW, even for V_{DD}=5V. For comparison, Device B optimization is also carried out for V_{DD}=3.3V, resulting in 3.8fW power dissipation. However, the optimization advantage is not as drastic as that realized with Device C, because the structure of Device B provides less structural possibilities for optimization than Device C. Thus, it is concluded that the structural optimization with the developed model is more efficient for rather complicated structures.

V. Conclusion

The reported compact model of power devices embedded in advanced low-power CMOS circuits is developed by solving the Poisson equation iteratively, without approximations. The model considers underlap and non-monotonous potential-distributions due to a 2D current flow. It is verified that the developed model can reproduce all observed DC as well as transient characteristics automatically.

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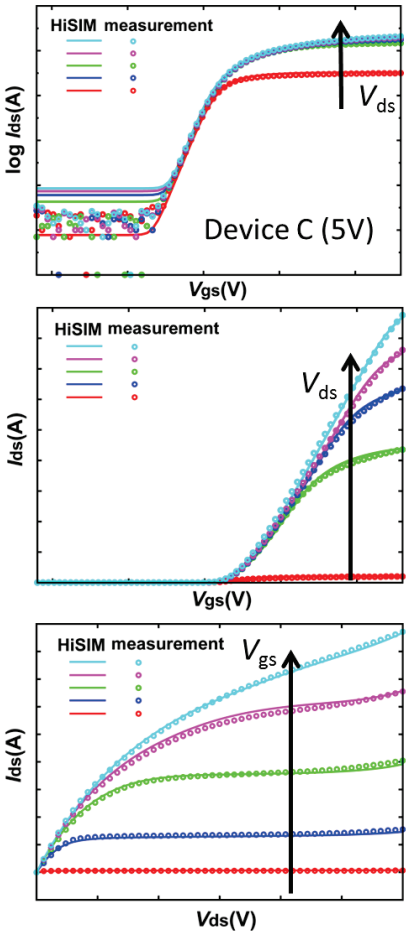

Fig. 9. Comparison of modeled and measured results for Device C.

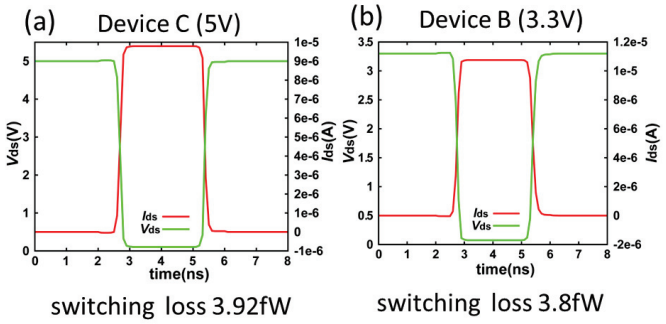

Fig. 10. Switching characteristics simulated with the developed model for (a) Device C optimized for 5V, (b) Device B optimized for 3.3V.