Reconfigurable FET SPICE model for design evaluation

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Abstract*—A lot of works have been done to propose and study alternative devices for future electronics. Between the possible candidates (Tunneling FETs, stacked nanowires…), Reconfigurable FET (RFET) appears as an interesting option to achieve reprogrammable logic in future circuits. The first step to evaluate the potentialities of new devices at circuit level is compact modeling. For the first time we propose a simple compact model of Fully-Depleted SOI RFET validated by TCAD simulations. Our model is implemented in Verilog-A to evaluate circuit-level performance with conventional CAD tools.

Keywords*— Compact model, RFET, Tunneling current, Fully-Depleted-Silicon-On-Insulator (FDSOI), SPICE, TCAD.

I. INTRODUCTION

The downscaling of CMOS technologies aims to improve performance and to increase circuit density. Among all possible candidates (Tunneling FET, nanowires ...), Reconfigurable transistor, RFET [1], stands as an interesting solution to achieve reprogrammable logic in future circuits [1-3]. From physical modeling point of view, very few papers have studied this type of architecture [2-3], especially from SPICE model point of view. Nevertheless, different works has already been done for particular cases of Schottky contact at source and drain such as Carbon Nanotube FET (CNFET) as detailed in ref. [4-5], where authors proposed solution to calculate the current for modeling point of view.

The paper is organized as follows: in Section II, we explain the global behavior of the RFET operation thanks to some TCAD simulation. In section III we detail the core equation of this SPICE model including some confrontation with TCAD in term of current and capacitance. In section IV, we proposed an illustration at circuit level of the SPICE model including a clear analysis of spacer thickness limited RFET performance.

II. TCAD ANALYSIS OF RFET OPERATION

The RFET device is composed of intrinsic silicon channel with metallic source and drain aligned with 2 Polarity Gates (PG) (figure 1.a). The RFET can be considered as a tunneling Schottky Barrier (SB) in series with channel. Thus, the drain current of RFET is limited by SB where its modulation is induced by two laterals. As it can be seen on figure 1.b; a positive (resp. negative) PG bias creates an accumulation of electrons (resp. holes) under the PG region. These accumulation regions are equivalent to source and drain

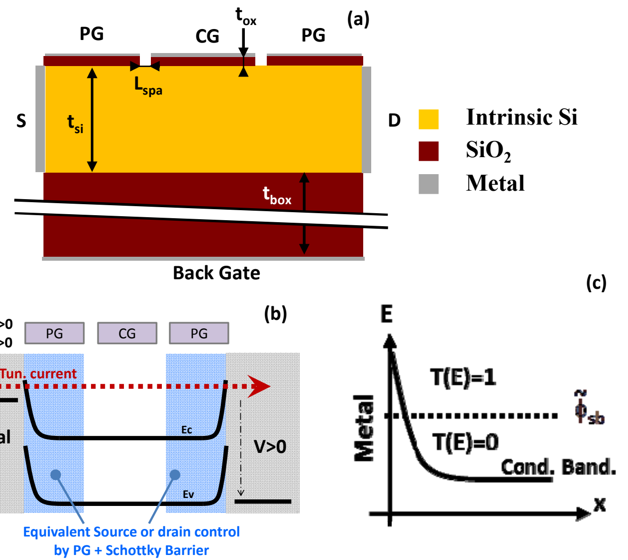

Fig 1. Some RFET schematic used: (a) RFET structure definition. (b) Schematic band diagram shows the tunneling mechanism between metal and silicon film in n-type configuration for positive bias. (c) Schematic representation of the analytical approximation on the tunneling probability used for current calculation.

regions by analogy to usual MOSFET. Carriers transport in the channel region is then controlled by both the Control Gate (CG or G) and the drain voltage like classical MOSFET. Usually, the Source/Drain (S/D) metal Work Function (WF) is chosen closed to the silicon mid-gap to obtain symmetrical transfer characteristics for n- and p-type devices.

Contrary to usual MOSFET where the S/D Fermi level is fixed by the doping concentration, here the carrier accumulation below PG has a floating quasi-Fermi level determined by both tunneling probability and electrostatics. To understand the electrostatic behavior of RFET structure, the geometry described in Fig. 1 has been simulated with TCAD tools accounting for non-local tunneling [7] and neglecting quantum confinement. TCAD Tunneling parameters such as effective mass are discussed in [3].

In figure 2, the surface potential and the quasi-Fermi level of long-channel RFET are shown for different bias conditions. We can observe that the potential or the quasi-Fermi level of

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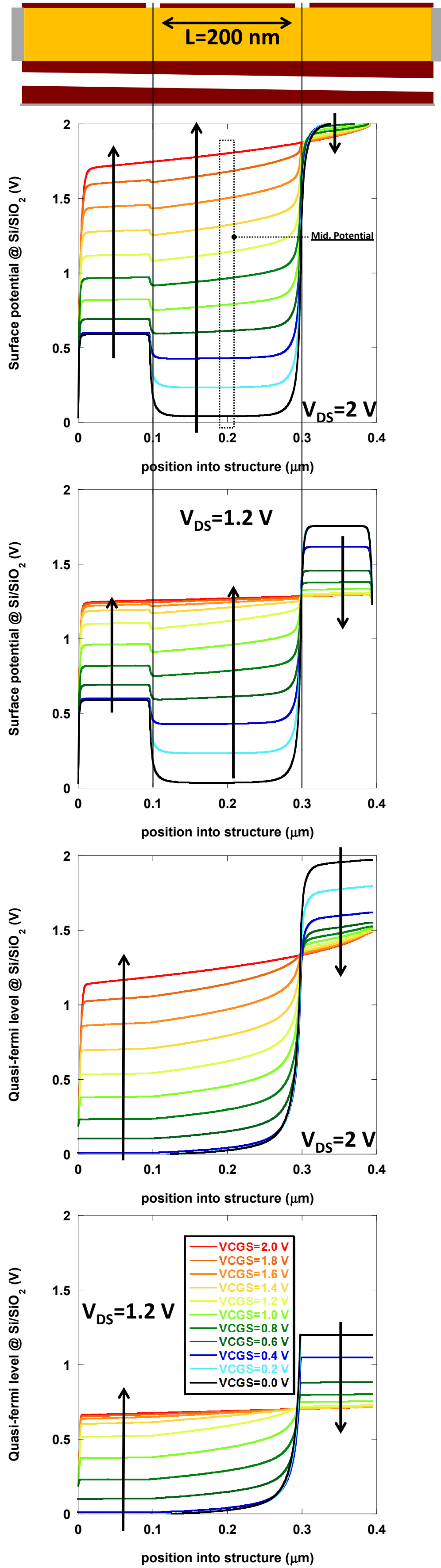

Fig 2. Surface potential and quasi fermi level obtained with TCAD simulation versus position for different bias condition. These simulations are realized with the corresponding geometry: t_{si}=10 nm, t_{box}=145 nm and t_{ox}=1nm.

the equivalent S/D region (below PG) balances with channel potential when sweeping from off-state to on-state regime. This variation is the direct impact of both Schottky barrier control by the Source-PG and Drain-PG at the source and drain junction. In addition, the potential gradient into the channel appears very small and is equivalent to the linear regime in MOSFET. These results confirm that the transport (tunneling) in RFETs is largely dominated by electrostatics and shows that middle channel potential is the key point of electrostatic behavior.

III. Model Description

Thanks to TCAD evidence, we need an analytical formulation of the Surface Potential (SP) in the middle of the channel to calculate the current and the charge. With previous developments successfully introduced in the Leti-UTSOI model [6], the mid-channel SP has an analytical formulation by considering the MOS-like capacitance architecture. After that it is possible to build a current and charge model.

A. *Surface Potential based modeling approach*

Based on the previous TCAD observations (through figure 2) and due to the complexity of RFET operation, the proposed compact solution is a combination of the following steps. First the low drain voltage surface potential (φ_L) is calculated as the native solution of surface potential with quasi-Fermi level clamped to the SB height (represented on figure 3.a & b):

$$\varphi_L = \mathrm{MIN}\left[\psi(V_{nL}, \alpha_L.V_{GS}), \phi_{sb}.\gamma_{mid} + V_{nL}, 0.0005\right] \quad (1.a)$$

$$V_{nL} = \left|V_{DS}/r\right| \quad (1.b)$$

where the definition of minimum function is: $\mathrm{MIN}(x,y,s)=[x+y-((x-y)^2+\delta)^{1/2}]/2$, α_L & γ_{mid} are calibration parameter, r is a fitting parameter, ϕ_{sb} is the Schottky barrier and Ψ correspond to the surface potential calculation [6]. Then the high drain voltage surface potential (φ_H) is calculated considering that the quasi-Fermi level now equals the difference of applied drain voltage and SB height:

$$\varphi_H = \psi(V_{nH}, \alpha_H.V_{GS}) \quad (2.a)$$

$$V_{nH} = \mathrm{MIN}(V_{DS} - \phi_{sb}.\gamma_{mid}, E_{qflS}, \delta_H) \quad (2.b)$$

where parameter E_{qflS} is a clamp value of the quasi-fermi potential to limit at the mid-channel potential, α_H & γ_{mid} are calibration parameter and δ_H is a smoothing parameter between E_{qflS} & (V_{DS}- ϕ_{sb}). Figure 3.a & b show mid-channel potential versus V_{GS} and V_{DS} respectively and illustrated the general behavior of equation 1 and 2. Finally, these two asymptotic solutions are combined through a smoothing function:

$$\varphi_{mid} = \mathrm{MAX}(\varphi_L, \varphi_H, \delta) \quad (3)$$

where the definition of maximum function is: $\mathrm{MAX}(x,y,s)=[x+y+((x-y)^2+\delta)^{1/2}]/2$ and δ is a smoothing parameter between φ_L & φ_H. All related model parameters used in equation (1-3) are defined in table I.

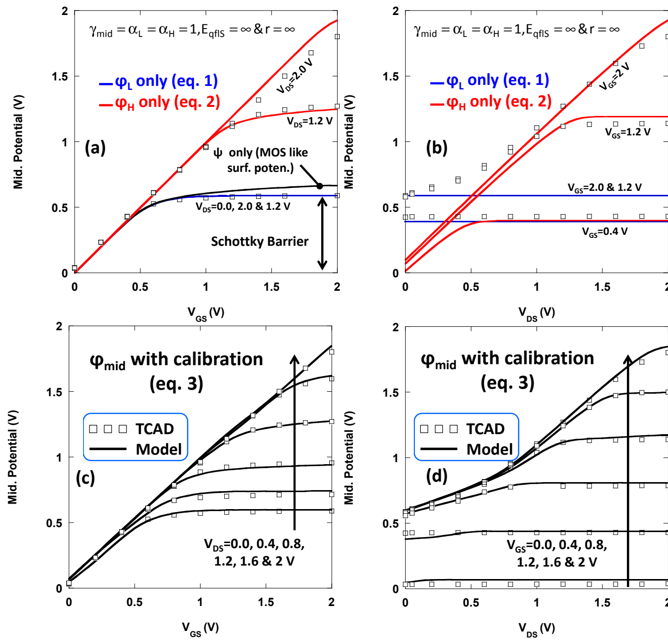

Fig 3. Comparison between surface potential at the middle of the channel length obtained with TCAD simulation and model for different bias condition. Potential at the middle of the channel versus V_{GS} without (a) and with calibration (c) & V_{DS} without (b) and with calibration (d).

As illustrated in figure 3.c & d, the proposed surface potential solution demonstrates a very good agreement in all regimes with TCAD simulations and, by construction, allows a clear extraction strategy of different parameter introduced in equations (1-3). Even if this model seems to be simple, it describes the general behavior of the potential in different bias conditions.

TABLE I. DEFINITION OF KEY PARAMETERS

ϕ_{sb}	Schottky Barrier
$\tilde{\phi}_{sb}$	Effective SB for Tunneling windows
E_{qflS}	Maximum Quasi-fermi potential
α & ɣ	Calibration parameter
r & δ	Smoothing parameter
n & Voff	Subthreshold parameter
A & B	Pre and exp factor for tunneling
CFR	Fringe Capacitance

B. Current model based on mid-channel SP solution

Tunneling current is classically based on Landauer equation: $\int T_{(E)}.(f_{s(E)}-f_{D(E)}).dE$ with T(E) the tunneling probability resulting from the WKB approximation [4] and f the fermi integral. Solving this equation introduces some numerical complexities clearly incompatible with compact modeling. Then we used the "effective SB" notion proposed by Knoch et al [5] and successfully introduced for Schottky Carbon Nanotube FET modeling [4]. Here the tunneling

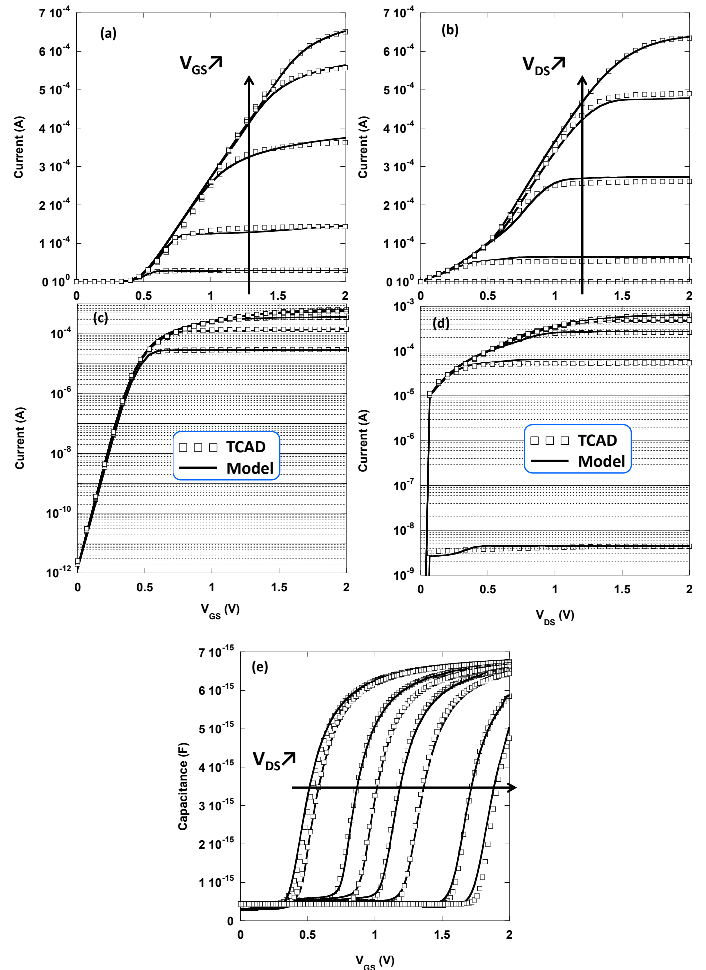

Fig 4. Comparison between TCAD (symbol) and model (line): Current versus V_{GS} (respectively V_{DS}) in lin scale (a) (respectively (b)) and log scale (c) (respectively (d)) for different V_{DS} (respectively V_{GS}). (e) Comparison on C_{CGCG} capacitance. These simulations are realized with the corresponding geometry: t_{si}=10 nm, t_{box}=145 nm and t_{ox}=1nm.

probability T(E) is equal to 0 under the "effective SB" and 1 otherwise (as illustrated on figure 1.c). By using this basic description, we provide an efficient and fully analytical solution for the source to channel current:

$$I \propto A.F.\ln\left(1+e^{-B.(\gamma.\tilde{\phi}_{sb}-\varphi_{mid})/(2.n.ut)}\right) \quad (4.a)$$

$$F=\frac{2.n}{1+e^{-B.(\gamma.\tilde{\phi}_{sb}-\varphi_{mid}-2.V_{off})/(2.n.ut)}} \quad (4.b)$$

Note "F" function is used to describe the subthreshold regime as already proposed in classical BSIM approach. Concerning the charge model, our solution proposed for the mid-channel potential is also used for the calculation of the charge under the CG as represented in this equation:

$$Q_G = C_{ox}.\left(V_{GS}-\psi\left(V_{nQ},V_{GS}\right)\right).W.L+CFR.V_{GS} \quad (5.a)$$

$$V_{nQ}=MAX(V_{DS}-\phi_{sb}.\gamma_{mid},0,\delta_Q) \quad (5.b)$$

The other Source, Drain and Polarity Gate charge is not modeled in this paper. In fact, the charge sharing is particularly difficult to formalize in presence of two Schottky barriers where Tunneling phenomena strongly impact capacitance behavior. It is why in the rest of the paper we supposed an equivalent charge sharing between source and drain.

Due to the native approach proposed here, we need to extract some parameter already listed in Table I. Finally, after the extraction from TCAD data of the different key parameters, a good agreement is obtained with TCAD simulations as illustrated on figure 4 for both current and C_{CGCG} capacitance for large range of V_{CGS} and V_{DS} for a given value of V_{PGS}. As expected, current versus V_{DS} depicted a superlinear regime as opposed to ohmic regime for MOSFET which is representative of tunnel device.

IV. Spacer as the Main Electrostatic Limitation of the RFET

In RFET devices, the distance between the PG and the CG (spacer-like behavior) directly impacts the On-state regime. In previous TCAD simulations, very small spacer thickness (which is systematically used in different studies [1-2]) has been considered. Thanks to our compact model, we have realized two libraries with or without spacer in order to calculate the corresponding delay of ring oscillators highlighting the impact of spacer. As expected, to increasespacer thickness adds series resistance (in intrinsic region between PG and CG) and limits the current which degrades performance of RFETs. Through Verilog-A implementation and SPICE simulation, the figure 5 illustrates the inverter ring oscillator delay reduction due to spacer thickness increase.

Don't forget that one the key optimization of such device is their integration in process flow for design application. But actually different papers discus about functionality [1-2] but do not include in their analysis the strong impact of the addition of two contacts (PG) in term of silicon area and performance. Finally, the proposed model allows further investigation to study RFET performances and especially the interest of reversibility at circuit level.

V. Conclusion

In this work, we developed a SPICE model for Fully-Depleted RFET transistor including physical behavior of Schottky barrier and its impacts on RFET electrostatic. Thanks to TCAD evidence and analysis, we develop a surface potential based analytical model to describe the mid-channel potential which is the concatenation of low and high drain cases. This solution is used to build our current and charge model. These models need some enhancement especially on the description of the charge sharing.

In the following, we have implemented this model in Verilog-A environment and after some parameter extraction, we have obtained a good agreement with TCAD data on both current and capacitance. Finally we have exhibited one of the main limitations of the RFET structure by evaluating the impact of spacer thickness on Ring Oscillator Delay.

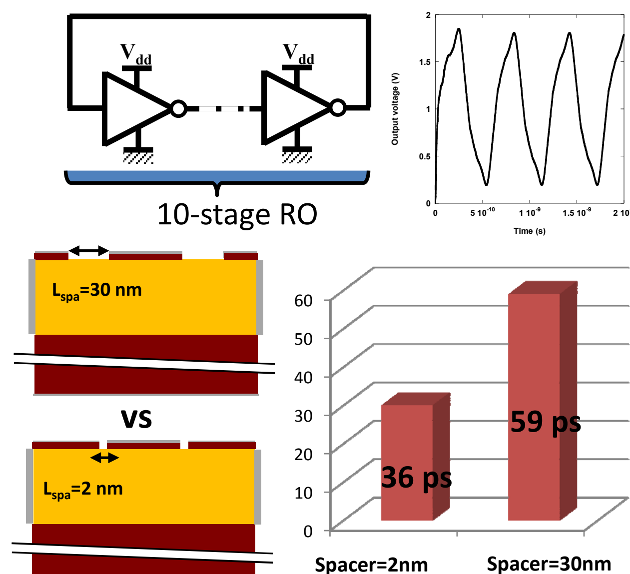

Fig 5. Delay of 10 Ring oscillator simulation with thin (2 nm) and thick spacer (30 nm). Here the n type and p type RFET is symmetrical.

Acknowledgment

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