Thermal effect and Compact model in three-dimensional (3D) RRAM arrays

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***Abstract*—A physical and electro-thermal Compact model for thermal effect and crosstalk in 3D RRAM arrays has been firstly proposed. The simulation results show that the transient thermal effect will dominate reset process. The proposed model is based on 3D Fourier heat flow equation and electro-thermal analogy which can couple thermal network to its electrical schematic. The comparison between the Compact model simulation results and numerical simulation shows a good accuracy. The proposed electro-thermal model then was written in Verilog-A by using Spectre on Cadence platform and had been verified by using ANSYS software.**

Keywords—resistive switching memory; three dimentional integration; compact model; thermal effect;

I. INTRODUCTION

High density 3-dimensional (3D) integrated technology in RRAM, such as 3D 1D1R crossbar array (1D1R: one Diode one RRAM), is a very promising candidate for future non-volatile memory integration applications [1-4]. 1D1R cell usually displays unipolar switching (Set and Reset operation at the same voltage polarity), and the Reset process is controlled by Joule heat [5]. The physical understanding of the programming and reliability mechanisms in unipolar 1D1R array requires a detailed characterization of the electrical and thermal transport performance of the memory cell. It is well known that the Joule heat can lead to the increase of the temperature of the device inside, which can induce the uneven distribution of thermal stress [6]. Therefore, the Joule heating effect would seriously affect the stability, reliability and life of semiconductor devices [7, 8]. With the increase of the integration level in 3D integrated RRAM devices, which will sharply enhance storage unit number and chip area, the thermal effect caused by Joule heat will become more serious. In this work, the thermal effect and thermal crosstalk of 3D RRAM array have been systematically investigated, and an electro-thermal model for 3D RRAM arrays has been presented.

II. THEORETICAL MODEL

The resistive switch mechanism here is in terms of the creation and breakdown of conductive filament (CF) in oxide layer [9, 10]. That is, the SET process is attributed to the dielectric soft breakdown and creation of CFs, and the RESET process is attributed to CF rupture due to the recombination of oxygen vacancies with the oxygen ions migrating from the electrode/oxide interface.

A. Thermel effect model

Figure 1(a) and (b) shows a schematic diagram of 3D RRAM crossbar structure with the basic 1D1R structure (D: diode (blue), R: RRAM (red), WL and BL: word line and bit line (gray)). Based on 3D Fourier heat flow equation, the thermal behavior in 3D RRAM is written as

$$\nabla k_{th}\nabla T + \sigma|\nabla V|^2 - c\rho\frac{\partial T}{\partial t} = 0, \quad (1)$$

here k_{th} is thermal conductivity, T is the temperature, c is the thermal capacity, ρ is the mass density of materials, V is the imposed voltage, t is time and σ is the electric conductivity which empirically reads as

$$\sigma = \sigma_0/(1+\alpha(T-T_0)), \quad (2)$$

here σ_0 is the electric conductivity at room temperature T_0, α is the resistivity temperature coefficient. WL or BL in the top and bottom layers of 3D array are assumed to be connected with ideal heat dissipation packaging structure and keep at room temperature T_0 during calculation, as

$$T - T_0|_{BC} = 0, \quad (3)$$

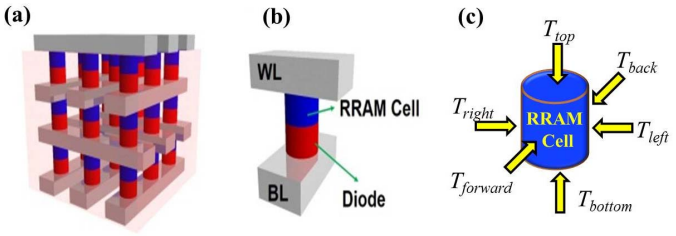

Fig. 1 Schematic diagram of 3D 1D1R crossbar structure (a), and 1D1R storage element (b), and (c) six-direction inputs of temperature.

B. Temperature model

The temperature of RRAM cell can be evaluated with Joule heat and heat dissipation as

$$T_{RRAM} = \int_{t_0}^{t_1} \frac{W_j - W_d}{C \cdot V_{volume}} dt \ , \quad (4)$$

where W_j is the Joule heat, W_d is the heat dissipation, C is the heat capacity, V_{volume} is the volume of the active region in the RRAM cell, and $W_j = I^2 \times R$ is the heating power of RRAM device. The heat dissipation W_d is expressed according to the change of thermal energy Q to time,

$$W_d = \frac{\partial Q}{\partial t} = -A \cdot \sum k_{\text{th}} \cdot \nabla T_{RRAM} \ , \quad (5)$$

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where A is cross-sectional area of heat conduction, and ∇T_{RRAM} is the temperature dispersion around the active region. Then, ∇T_{RRAM} can be reduced to the temperature gradient in three directions (*x, y, z*) in 3D RRAM device as

$$\nabla T_{RRAM} = \frac{\partial T_{RRAM}}{\partial x} + \frac{\partial T_{RRAM}}{\partial y} + \frac{\partial T_{RRAM}}{\partial z} = \frac{T_{RRAM} - 300}{d_{RRAM}}, \quad (6)$$

where d_{RRAM} is the distance for T_{RRAM} to decrease to the room temperature. Here we also assume that the temperature outside the active region is close to the room temperature. By combining Eqs. (4)-(6), T_{RRAM} is written as

$$T_{RRAM}(t) = \frac{d_{RRAM} W_j}{A \cdot k}\left[1 - \left(\frac{-k \cdot A}{d_{RRAM} C V_{volume}} t\right)\right] + 300. \quad (7)$$

By solving in Eq. (7), and applying an equivalent RC model to analog such temperature behavior with time constant given by:

$$\tau = RC = \frac{d_{RRAM} C V_{volume}}{k \cdot A}. \quad (8)$$

C. Temperature feedback

Based on Eq. (7), the temperature of a single RRAM cell can be obtained by assuming ambient temperature of 300 K. However, the ambient temperature of a single RRAM cell in 3D RRAM arrays depends on the neighboring cells in the six directions, such as, forward, back, right, left, top, and bottom, as shown in Fig.1(c). Therefore, to calculate the ambient temperature in 3D array, six inputs for the temperature to RRAM module should be added as

$$T_{ambient} = (1-\lambda) \times \frac{T_{back} + T_{forward} + T_{left} + T_{right}}{4} + \lambda \cdot \frac{T_{top} + T_{bottom}}{2}, \quad (9)$$

where λ is the weighting factor of the temperature for metal line (BL and WL). Every RRAM cell has a temperature output T_{out} that can provide the calculated temperature feedback for the cell and neighboring cells.

D. Termal-electrical analogy

A thermal system can be generally simulated by using a discrete element electrical circuit, composed by thermal resistances and thermal capacitances, where the temperature and thermal power are retained as voltages and currents, respectively. Due to a close relationship with physical reality of the 1D heat flow, the parameters for RC equivalent circuit diagram can be derived directly from the following Eq. (10). The physical variables are specified in their thermal equivalents by using a geometry and thermal conductivity and thermal capacity of materials. Then one can define thermal resistance and thermal capacitance as

$$\begin{cases} R_i \approx R_{thi} = \dfrac{d_i}{\kappa \cdot A} \\ C_i \approx C_{thi} = c \cdot d_i \cdot A \end{cases}, \quad (10)$$

where d_i is the thickness for the *i*th cell, *k* and *c* is the thermal conductivity and special heat capacity.

III. Resuts and Discussion

A. Thermal effect and crosstalk in 3D RRAM

Figure 2(e)-(h) show simulated temperature evolution during reset process for different arrays in Figure 2(a)-(d). It is found that the thermal change is faster along the WL/BLs and the CFs of RRAMs in both horizontal and vertical directions due to their higher thermal transfer ability. Figure 3(a) shows the operated time dependence of temperature in programmed device in Figure 2. Figure 3(b) shows the time t_s of reaching thermal steady state as a function of array. It is found that the temperature and t_s increase with increasing array, i.e., t_s is 50 ns for a 1D1R element, which is much higher than that of an individual RRAM (<10 ns), and t_s is 550 ns for a 3×3×3 block array.

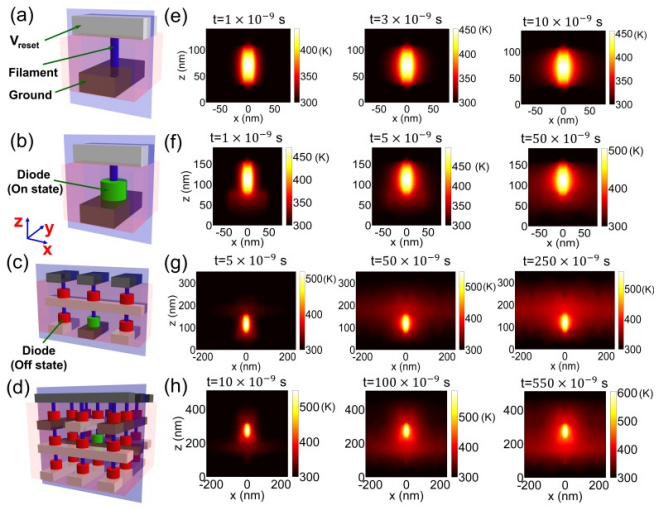

Fig. 2. Schematic diagram of the device structure: (a) an individual RRAM cell, and (b)-(d) 1D1R crossbar blocks with 1×1×1, 3×1×2, and 3×3×3 array, respectively. (e)-(f) Temperature evolution maps of the cross-sections (blue planes) in (a)-(d), respectively.

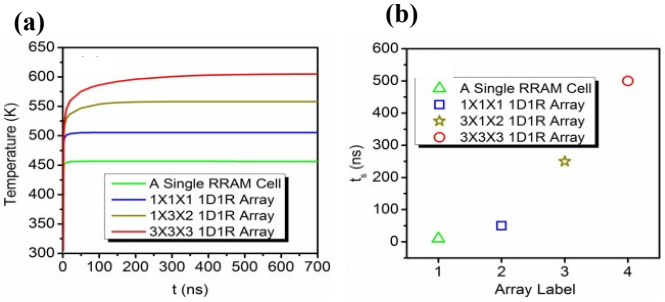

Fig. 3. Highest temperature evolution in the programmed RRAM cell with selected array structures in Fig. 2. (b) t_s (the time reaching thermal steady state) as a function of array.

Figure 4(c)-(d) and (e)-(f) show the calculated potential distributions and temperature evolutions of the cross-sections in the 3D array systems, respectively, corresponding to the two selected cases in Figure in Fig. 4(a)-(b). It is found obviously that the increase of temperature in the programmed RRAM devices is much larger than that in the unprogrammed ones.

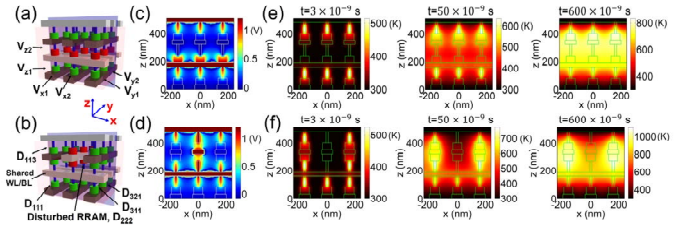

Fig. 4. (a)-(b) Schematic diagram of two selected 'worst cases' in thermal crosstalk. (c)-(d) Potential maps in the array structures in (a)-(b). (e)-(f) Temperature maps of the cross-sections (blue planes in (a)-(b)) for two array structures at different time, respectively. Disturbed RRAM device (labeled as D222) locates in the center of the array, which is surrounded by several programmed RRAM cells.

B. *Simulation of Compact model in 3D RRAM array*

After analyzing the thermal effect and crosstalk of 3D RRAM array, we perform simulation for the proposed electro-thermal model (written in Verilog-A) by using Spectre on Cadence platform. Figure 5 shows circuit diagram in a 3×3×3 RRAM arrays. The input parameters are shown in Table 1. Figure 6 shows the simulated transient temperature curve. Figure 7 shows the temperature and current curves of center RRAM cell operation in 3D RRAM array applied pulse voltages.

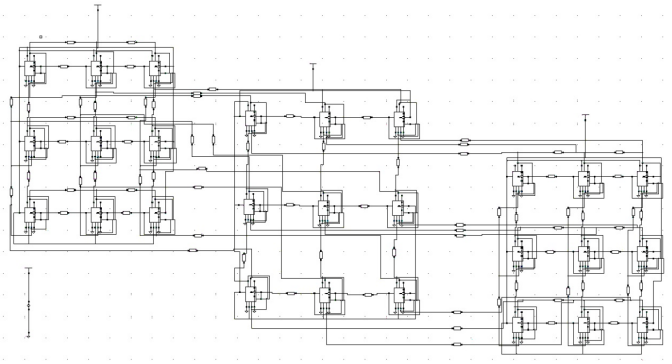

Fig. 5. Circuit diagram of 3D RRAM array.

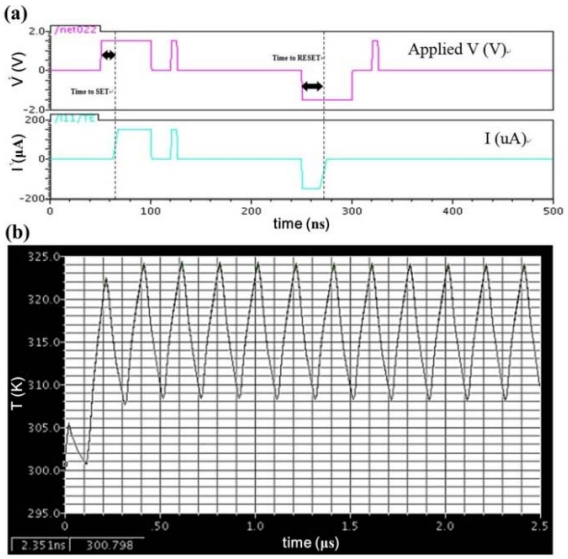

Fig. 6. (a) Pulse voltage, current curve during programing, (b) simulated transient temperature curve in 3D RRAM array.

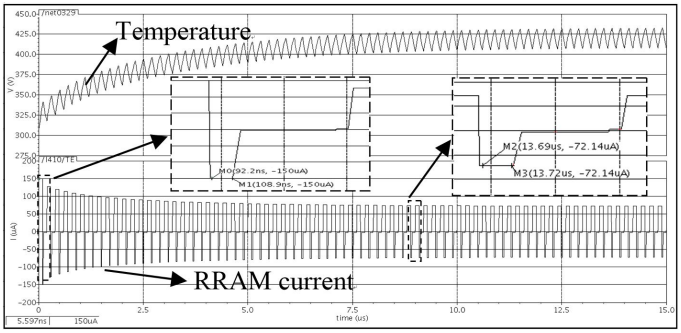

Fig. 7. Simulated temperature and current curves of center RRAM cell operation in 3D RRAM array applied pulse voltages.

C. *Model verification*

To verify the proposed model, we performed a numerical simulation by using ANSYS software. The initial ambient temperature is 300 K. In order to approach real heat transfer condition, heat convection between the surface of metal line and air is set to a high value making analogy of the heat conduction between metal lines. Figure 8-10 show the simulation results by using ANSYS for 1×1×1, 2×2×2, 3×3×3 RRAM arrays, respectively, at which all RRAM cells are applied pulse voltage. One can see that a good agreement between Compact model and numerical simulation is observed.

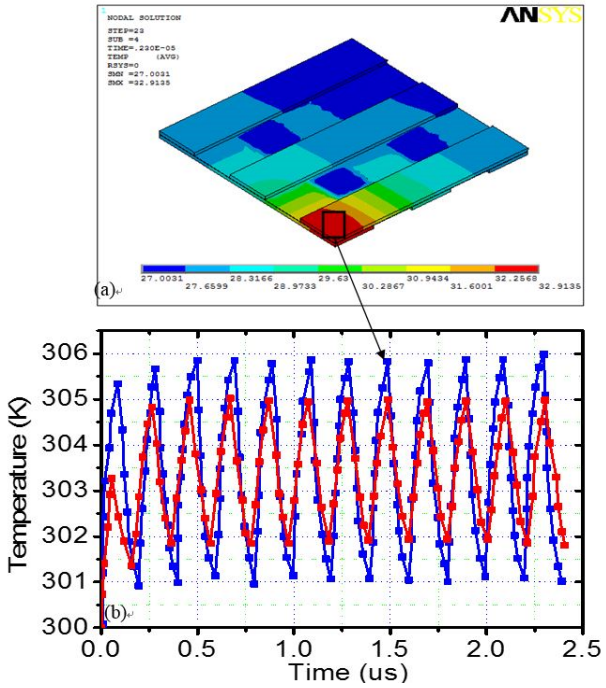

Fig. 8. RRAM 1×1×1 array simulation results in ANSYS, only a single RRAM cell is applied by pulse voltage.

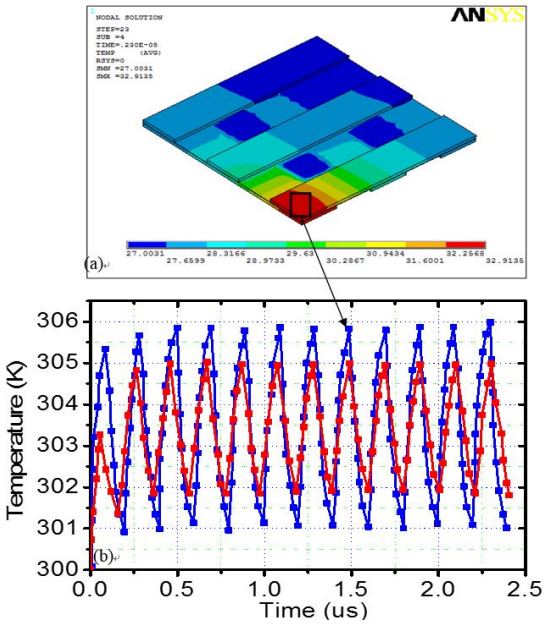

Fig. 9. RRAM 2×2×2 array simulation results in ANSYS, here two rows RRAM cells are applied by pulse voltage.

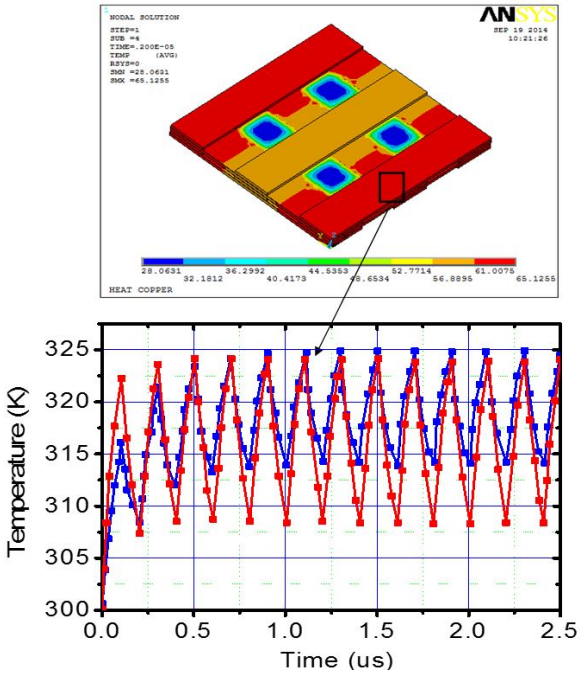

Fig. 10. RRAM 3×3×3 array simulation results in ANSYS, here two rows in 3 layers RRAM cells are applied by pulse voltages.

IV. Conclusion

We proposed a theoretical model and electro-thermal Compact model to study the thermal effect for 3D RRAM arrays. It is revealed that the time system consumes to reach steady thermal state increases with the increase of array stack layer, and individual device models based on thermal steady state are not applicable in 3D arrays. The comparison between the simulation results of Compact model and numerical simulation shows a good agreement. This model can be used to predict temperature distribution and analyze thermal crosstalk in 3D RRAM arrays. Finally, the proposed electro-thermal model (written in Verilog-A) was performed by using Spectre on Cadence platform.

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TABLE I. Parameters for Simulation

Materials	k W/(m.K)	C (J/(m^3.K))	d (nm)	A (μm^2)
HfO_2	1.1	1.161×10^6	20	200
Cu	40	3.404×10^6	20	100