TCAD Proven Compact Modelling Re-centering Technology for Early 0.x PDKs

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***Abstract*— Well-calibrated predictive TCAD simulations are employed to generate target data for compact models for better pre-V1.0 PDK development. A reliable re-centering technology has been developed which can accurately migrate the global and local variability and the corresponding corners. FinFETs calibrated to published data by Intel at the 14nm technology node are employed as test-bed devices.**

Keywords—Compact modelling; TCAD; FinFET

I. Introduction

Compact models (CM) in early pre-V1.0 PDKs for new CMOS technologies usually reflect the early spec of the foundries' marketing departments. The creation of such early compact models, years before the technology is fully developed, partially relies on the very limited predictive features of the CMs. In CMs, the complex transistor operation is approximated with (semi) analytical expressions, and the accuracy of the models is achieved by fitting a large number of 'adjustable' model parameters to measured transistor characteristics. At early stages of technology development, measured target characteristics are not available for all electrical targets (ETs) and available data may be inconsistent or unreliable. Further to this any early silicon characteristics are usually inferior to the final target characteristics for a mature technology. As a result the creation of the pre-V1.0 compact models involves the black magic of 're-centering' – shifting early silicon performance to the targeted mature technology levels. This process involves extracting CMs from silicon data that does not meet the technology performance target, and this is migrated by changing compact model parameters to meet the expected performance characteristics of the future mature technology. This difficult process entirely depends on the experience and the intuition of the CM experts and even when performed with care can result in inconsistent compact models that can deliver misleading circuit simulation results, increasing the pain of early fabless adopters of the technology. A better pre-V1.0 PDK CM approach is to use well-calibrated predictive TCAD simulations to generate target data for CMs. The more physical and predictive nature of the TCAD simulations guaranties trustable and consistent target characteristics for CM extraction, reduces the discrepancy between early and more mature PDKs and ensures consistency in early CMs. TCAD simulation also allows for more accurate variability and reliability data to be included in the pre-V1.0 CMs at early stages when such measurements are not available from silicon. In this paper we use predictive TCAD simulations to develop a reliable re-centering technology that accurately migrates the global and local variability and the corresponding corners.

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II. TCAD Setup

FinFETs calibrated to published data by Intel at the 14nm technology node are employed as test-bed devices in this study. Fin geometry information is extracted from TEM image of Intel fins, as illustrated in Figure 1. The device 3D structure implemented in the GSS simulator Garand [1] is depicted in Figure 2, with silicon, metal gate and source/drain contact highlighted in Figure 2 (b). Based on the published I-V characteristics [2], a reverse engineering study was carried out to set up the original TCAD deck. The Id-Vg characteristics of n- and p-FinFET obtained from original TCAD decks are shown in Figure 3, demonstrating TCAD setup coming from reverse engineering is able to reproduce silicon measurement results.

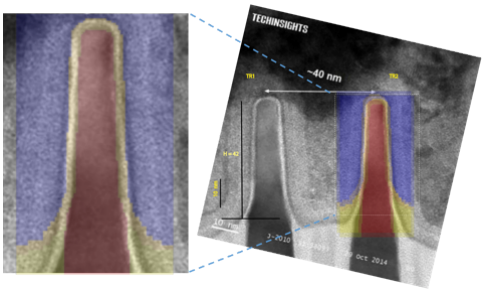

Fig. 1. Fin cross-section generated by GSS structure editor, including the fin, gate oxide and STI, against the TEM image

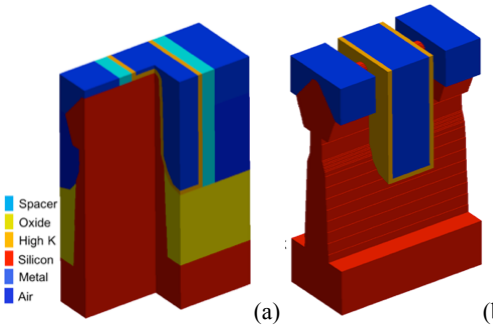

Fig. 2. The 14nm FinFET structure generated by GSS structure editor

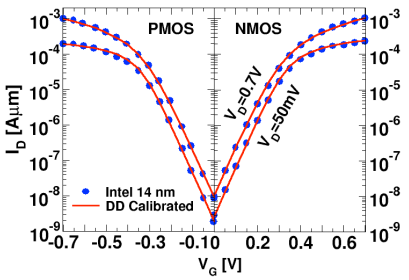

Fig. 3. Device Id-Vg characteristics obtained from calibrated TCAD decks against silicon measurements

Furthermore, a shifted design is setup based on the original TCAD to provide an updated TCAD deck, to represent the new generation of technology where the improvement of device performance is introduced by the improvements on the HK-metal gate process (reduction of EOT), strain process, lithography and etching process (reduction in metal gate length), annealing process (reduction on self-diffusion of S/D doping). In comparison to the old generation, the on-current displays around 20% improvement without degradation at subthreshold region.

In order to capture the impact of the re-centered device on global variations, Design of Experiments (DoE) simulations are performed for both the original TT and the shifted TT on respective 5x5 DoE spaces, with fin width, Wfin varying from 6nm to 10nm for both devices and gate length, Lg varying from 16nm to 21nm for the original TT and from 13nm to 19nm for the shifted TT. Figures of merit (FoM) extracted from the simulation results are illustrated in Figure 4, showing the migration from the original DoE to the shifted DoE. The DoE simulations provide the essential information for process corner characterization in PDK. Moreover, statistical simulations have also been performed over the respective 5x5 DoE spaces, illustrated in Figure 5, based on which the total corners of the original and shifted designs can be provided in PDK as well.

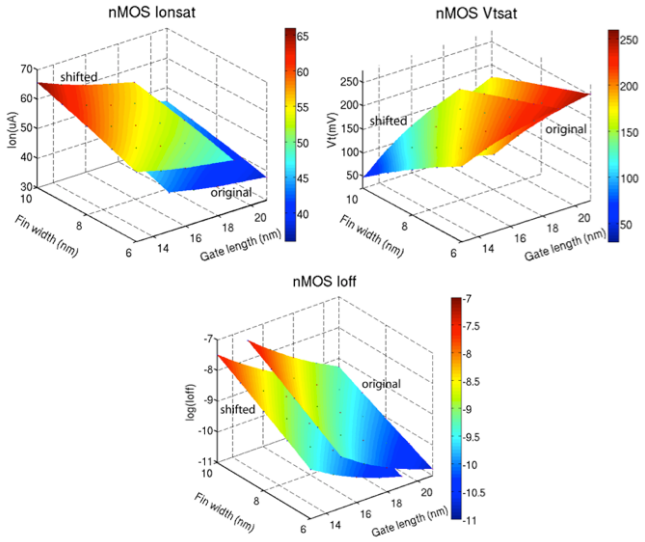

Fig. 4. Figures of Merits for nFinFETs, showing moving from the original DoE to the shifted DoE

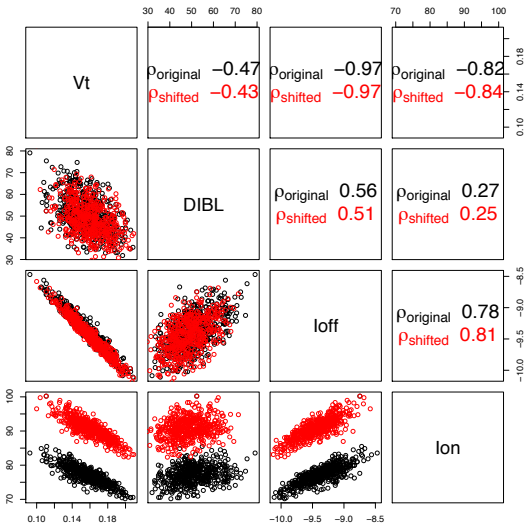

Fig. 5. Statistical TCAD simulations, showing the correlations between Figures of Merits for TT nFinFETs at original and shifted design point, highlighting the good control of subthreshold performance, and much improved drivability in shifted design

III. Methodology and Results

As a starting point, comprehensive compact modeling extraction is performed on the original TT devices with BSIMCMG. The schematic of the re-centering compact modeling procedure is illustrated in Figure 6. Using the original TT compact model as a base model, figures of merit, defined based on new performance targets, are used as the target data for re-centering, and only a small subset of carefully selected compact model parameters will be re-extracted at this stage. Based on careful analysis, the FoM specification used as a target for re-centering is illustrated in Figure 7. A four step re-centering strategy, involving only 7 BSIMCMG parameters in this case, has been developed using GSS compact model extraction tool Mystic [1].

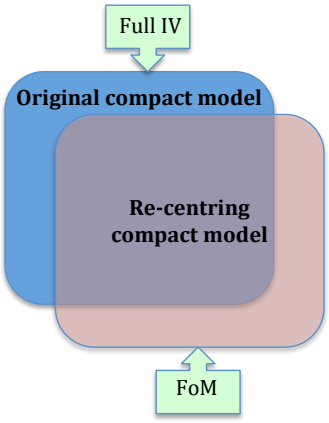

Fig. 6. Schematic of compact model re-centering procedure

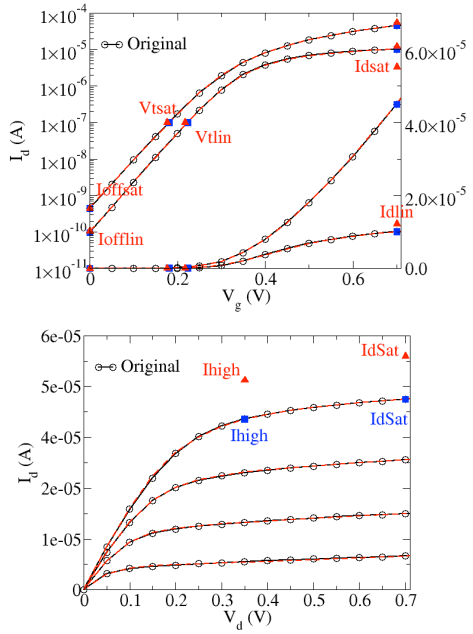

Fig. 7. FoM target used in compact model re-centering study

For the TT devices, excellent agreement is obtained between the original and re-targeted compact model, as shown in Figure 8. For this particular case, although only 7 parameters are used in the re-centering study, it can accurately reproduce full IV curves obtained from TCAD simulation, with less than 1.5% of overall RMS error for the full I-V curves, and the RMS errors of all FoM are less than 1%.

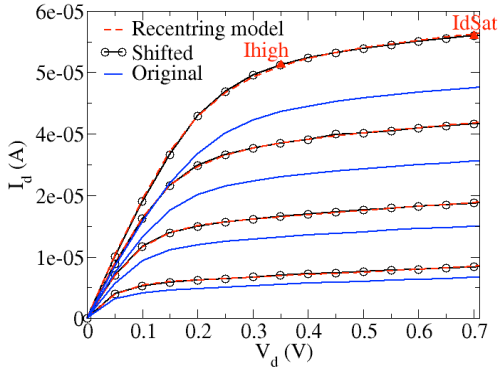

Fig. 8. IdVd characteristics of re-centering model against TCAD results.

Based on these TT model cards, a subset of the re-centering parameter-set is identified and re-extracted for process variations covering DoE space, using Mystic. Special care is taken in the extraction strategy to ensure the smooth distribution of the extracted model parameters over the DoE, as shown in Figure 9. Response surface models are then built based on the extracted parameters, which are regenerated using ModelGen [1]. TCAD simulation results are used to validate the models, which shows excellent accuracy: Using the n-type shifted FinFET as an example, the relative error of saturation on-current is less than 1% over the whole 5x5 DoE, and the deviation of the threshold voltage is less than 3mV over the whole DoE, as demonstrated in Figure 10.

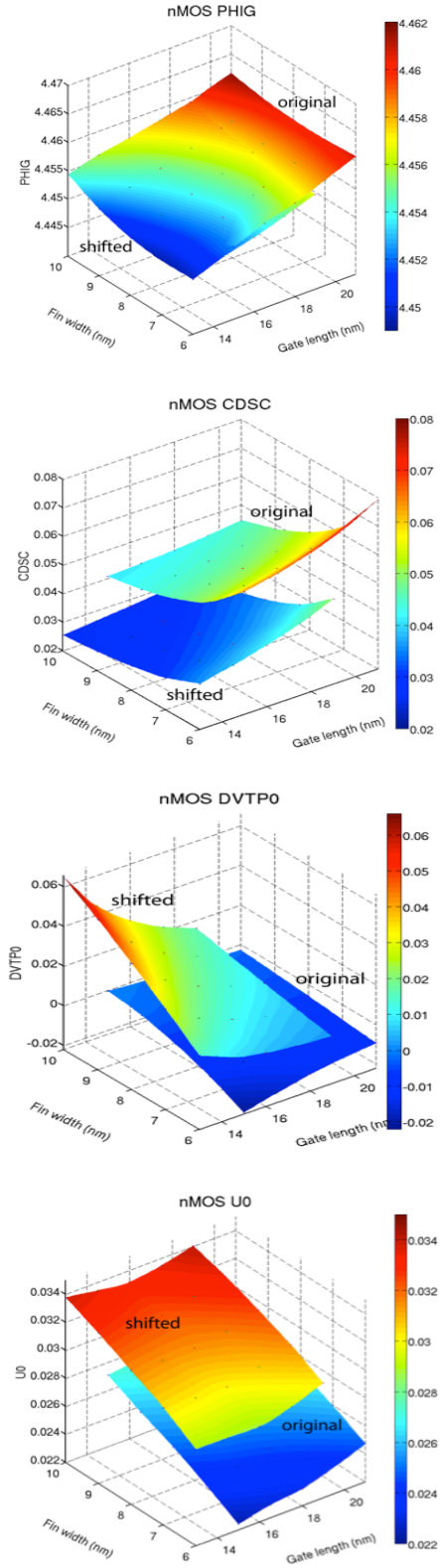

Fig. 9. BSIM-CMG parameter distributions over the shifted DoE space comparing to the orginal DoE.

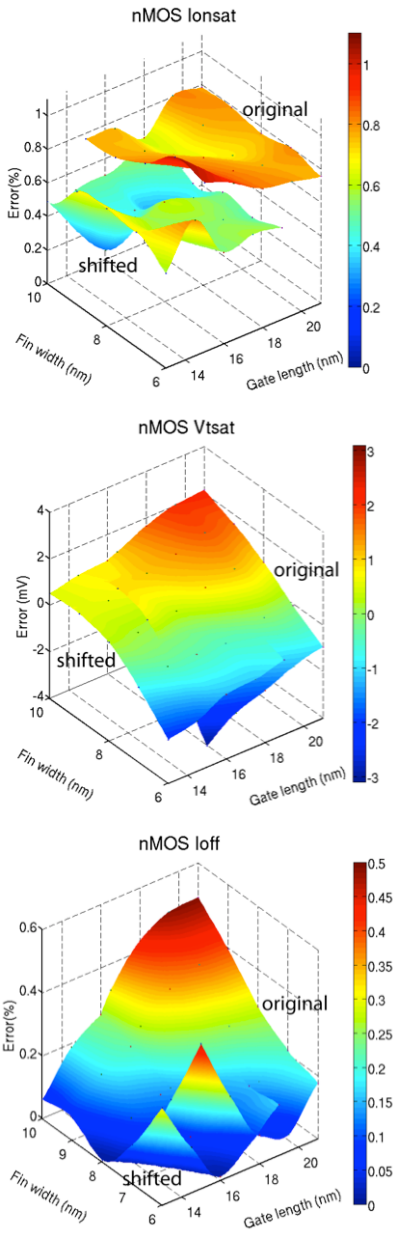

Fig. 10. The extraction errors of compact models with respect to TCAD results over both the shifted DoE and the original DoE, showing excellent accuracy achieved for Figures of Merits.

Furthermore, statistical compact modeling over the DoE space has been performed to capture both the global and local variations. The mean values and standard deviations of some extracted statistical parameters are shown in Figure 11, demonstrating the smooth evolvement of statistical compact model parameter distributions across both DoE spaces, with the design shifted from original to re-centered. As the fitting errors in Figure 12 demonstrate, the statistical compact modeling procedure shows excellent accuracy compared to the TCAD simulations.

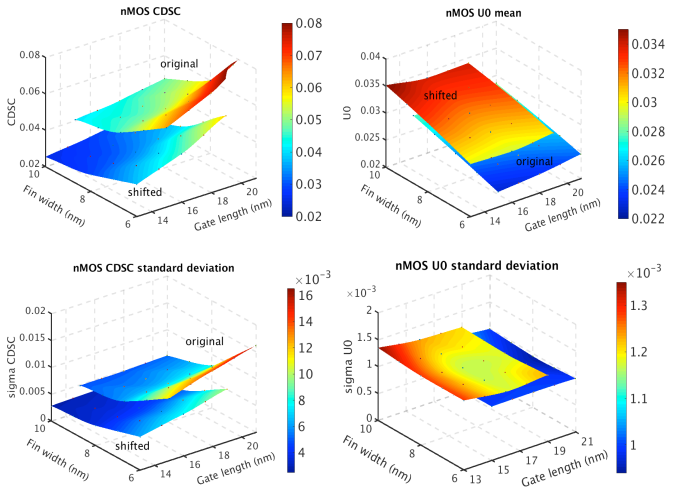

Fig. 11. The mean and standard deviation of some BSIM-CMG parameters extracted from statistical compact modelling for both original and shifted design.

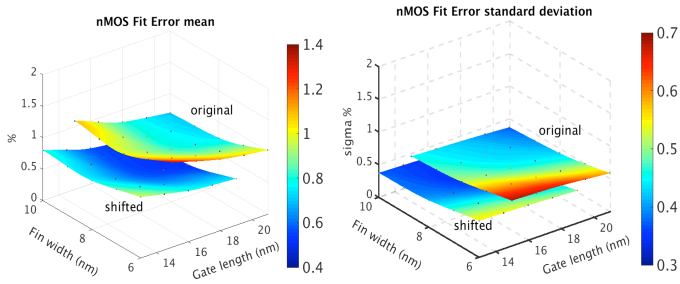

Fig. 12. The fitting errors of statistical compact models with respect to TCAD results.

IV. Conclusions

A TCAD based compact model re-centering strategy is proposed for early 0.x PDK development. Some results are presented for well-calibrated FinFETs at the 14nm technology node. Based on these, total corners of new generation design can be be evaluated by combination of re-centering and response surface modeling approaches provided in ModelGen. These lay the essential foundation and can be used to investigate the circuit performance variations, such as SNM and yield of SRAM. Excellent accuracy has been demonstrated by the compact model re-centering strategy. The proposed strategy will help to achieve rapid adaption of new technologies in IC design.

References

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