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3D TCAD analysis of the effect on dI/dt of cathode shorts in Phase Controlled Thyristors

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***Abstract*—This work presents a comprehensive overview of role played by cathode shorts in Phase Controlled Thyristors (PCTs), combining large scale 3D TCAD simulations and experimental data. The impact of shorts on breakdown voltage (BV), dV/dt and on-state voltage (V_T) is reviewed, discussing tradeoffs and optimization in device design based on the placement of the shorts. Moreover, the present work utilizes large scale 3D simulations of Phase Controlled Thyristors to shed more light on the impact of shorting patterns on the dI/dt of PCTs. The use of complex meshes with a realistic short pattern and ad-hoc post-processing techniques offer additional insight on phenomena that have been treated mainly with simplified analytical models [1][2][3] or approximate numerical methods [4], allowing for improved device design.**

I. Introduction

Even with the increase in recent years of IGBT-based Modular Multilevel Converters (MMC), thyristors remain crucial devices in HVDC and many industrial applications [5][6]. Reasons to employ thyristors in a wide variety of uses include their optimal carrier density configuration (i.e. very low on-state losses), device area up to 6 inches (large current capability), and low fabrication cost. For example, the next generation UHVDC systems to be operated at power breaking level of 10 GW and with DC link voltages rated over 1000 kV are enabled by thyristors with blocking voltages greater than 8.5 kV, carrying currents in excess of 5 kA with an on-state voltage drop lower than 2 V [6][7].

3D TCAD is needed to investigate phenomena that cannot be directly measured or understood through simplified approaches: in our previous work [8], the first large-scale 3D simulations of devices of volume of several mm^3 (500'000 nodes) are presented and the impact of the placement of cathode shorts on breakdown voltage (BV) and dV/dt is discussed.

The present work features simulations of larger structures (up to 1.5 million nodes), with a more realistic short configuration and investigates in detail the turn-on of the thyristor. Ad-hoc visualization techniques are used to understand the role played by the shorts when the device enters conduction mode and to suggest improvements to the dI/dt capability.

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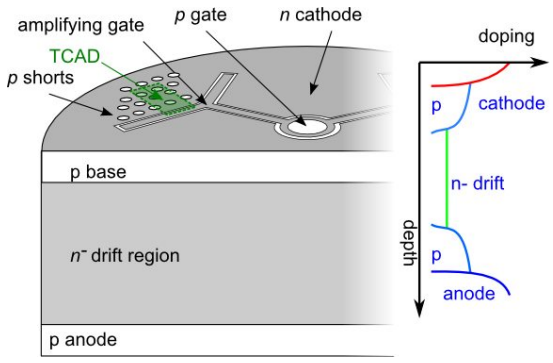

Fig. 1. Sketch of the typical structure of a modern PCT (left). The top side shows the Gate and Cathode contacts and the amplifying gate (AG) structure. The cross section indicates the doping regions. A schematic representation of the doping profiles under the cathode is presented on the right side.

II. Typical PCT structure and operation

Thyristors are characterized by a $n-p-n-p$ structure that operates in a positive feedback loop resulting in a higher carrier concentration than bipolar devices with a gate channel like IGBTs or unipolar devices such as power MOSFETs. As shown in Fig. 1, the deep p diffusions at the cathode and anode sides guarantee blocking in the forward and reverse direction. The device can be triggered in conduction only in the first quadrant with a gate current pulse. Typically thyristors employ an amplifying gate (AG) to reduce the gate current triggering requirements. As holes flow from the gate and the amplifying gate into the p-base, electrons are injected into the n^- drift layer. The so-called "delay time" needed for the electrode to reach the anode can be quite significant for thick, high voltage thyristors. Then, during the "rise time" phase, conductivity modulation occurs in the drift layer, significantly reducing the voltage drop across the device. Initially, conductivity modulation occurs only at the periphery of the amplifying gate, and gradually spreads towards the outer edge of the cathode. This process can be expedited by appropriate amplifying gate geometries (such as the hammer shown in Fig. 1) that initiate conduction on a much larger area. Moreover, as depicted on the left of Fig. 1, the $n+$ cathode area is characterized by a large number of $p+$ shorts that are essential to the ruggedness and performance of the device, as explained in Sections IV

and V.

III. Large scale 3D TCAD simulations and methodology

While 2D TCAD is routinely used in power semiconductor devices because of ease of creation of the model grid and because of speed of simulation, 3D simulations are still rare but are increasingly being used to study particular problems, such as terminations [9][10], GTOs [11], and anode shorts in IGBTs [12]. 3D TCAD can be used to understand physical phenomena in PCTs that are difficult to conclusively measure and explain experimentally. It is a more powerful alternative to simple analytical models [1] or approaches based on equivalent circuit blocks [4].

Power semiconductors are a challenging field for semiconductor simulations. The first difficulty is the size of the mesh: a Silicon high voltage power semiconductor device has a thickness in the range of few hundred microns to more than a thousand microns and an active area in the order of square centimeters, enabling conduction currents from hundred to thousands of Amperes. Since the minimum lithographic feature size is typically in the order of microns for MOS and BiMOS devices and of several tens of microns for bipolar device, the 3D mesh for a representative part of a device ranges from tens of thousand nodes to more than a million nodes.

For such large meshes the Newton method requires excessive amounts of memory. Conversely, the Gummel iteration scheme typically fails at high currents and therefore is not advised for bipolar devices such as IGBTs or thyristors. Therefore, iterative linear solvers are the best approach. However, convergence is guaranteed only if the update operator has a spectral radius smaller than unity. The spectral radius is related to the matrix condition number, which is known to degrade when devices are much bigger than the Debye length, present more p-n junctions than contacts, or are very heavily doped. All these conditions are typical of power semiconductor devices.

In order to facilitate convergence and maintain acceptable simulation times, it is necessary to optimize the device mesh. Since commercial software is based on the OCTREE algorithm, the simulation domain is represented by a cuboid with Manhattan geometry (i.e. round shorts are approximated by squares) [13]. Also, the mesh discretization is applied carefully, using powers of 2 as the number of mesh divisions to maintain control over the number of points.

Finally, because of the shorts, the cathode electrode forces an equipotential boundary condition across many highly doped $p-n$ junctions. Imposing the charge neutrality condition typical of ideal ohmic contacts results in inconsistencies and severely hampers convergence. In the simulator sdevice from Synopsys, the "EqOhmic" boundary condition uses the electrostatic potential calculated with the contact removed instead of the builtin potential as the boundary condition, resulting in a better approximation and improved convergence [13].

All simulations in this work are based on the drift diffusion approximation, with Shockley-Read-Hall generation recombination, Auger recombination, Philips unified mobility model, Okuto-Crowell impact ionization, and Slotboom bandgap narrowing. Effective position-dependent lifetime is used to account for lifetime engineering, as explained in [8].

IV. Current understanding of the role of shorts in PCTs

The most obvious effect of shorts is to limit the current gain of the npn transistor under forward blocking, especially at high temperatures, providing a distributed path for the removal of leakage current, and to avoid excess electron injection in the $n-$ drift layer. Shorts are also useful during high dV/dt transients applied to the anode, as they collect the displacement current, preventing an accidental device triggering up to transients of several $kV/\mu s$. Simulations in [8] indicate that, as expected, dV/dt capability increases with the percentage of shorted area, as confirmed by experimental data reported in [14]. Simulations also indicate that the first rows of shorts in the close proximity of the amplifying gate are crucial to obtain high dV/dt capability.

Therefore effective device designs feature a dense and uniform distribution of shorts, with a small diameter and in close proximity to the AG. Thus, a high dV/dt transient triggers the AG, igniting quickly the thyristor and preventing localized conduction and potential device failure [8].

However, shorts also create so-called "dead zones" in the cathode where the current gain is limited and hence regenerative action is not possible, resulting in local lower conductivity modulation and in overall increased on-state voltage V_T. As reported in [14], the size, position, shape, array configuration and separation of shorts affect on-state voltage, dV/dt, and other parameters of interest. 3D TCAD simulations in Fig. 2 and Fig. 3 compare two structures with identical total shorted area but with different shorts sizes and amount of shorts [14]. Not only larger shorts result in a wider dead zone in the horizontal plane as indicated by the current density plot in Fig. 2 but also affect the conductivity modulation in the vertical direction, resulting in a less homogeneous current distribution as visualized by the electron density plot in Fig. 3.

Other important parameters of interest for thyristors are the circuit-commutated turnoff time t_q (the total time from the instant reverse recovery current begins to flow to the start of forward blocking) and the reverse recovery charge Q_{rr} (defined as the integral of the reverse current during commutation starting and ending at the changes of current direction). As discussed in detail in [14], the removal of excess charge during turn-off is facilitated by a larger shorted area, offering an advantageous alternative for lifetime engineering for industrial thyristors since accurate Q_{rr} banding is not required. TCAD simulations shown in Fig. 4 illustrate the tradeoff between V_T and Q_{rr} [14].

Concluding this review, it should be remarked that designing an appropriate shorting pattern for a thyristor is not trivial, as any undershorted area could turn into a potential point of failure.

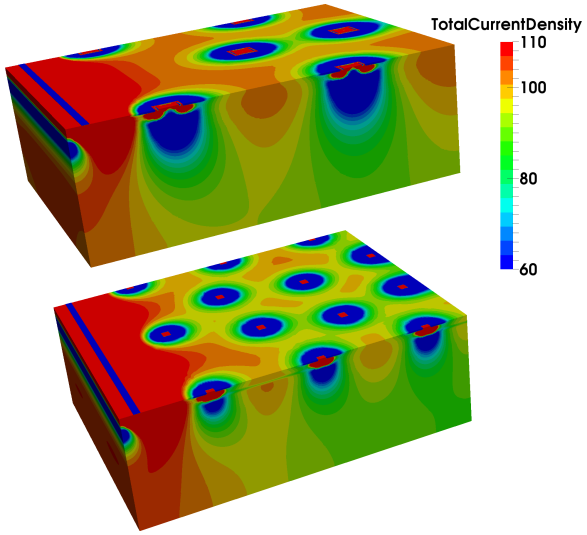

Fig. 2. 3D TCAD simulations of current density for PCTs with the same shorted area but with different short size [14].

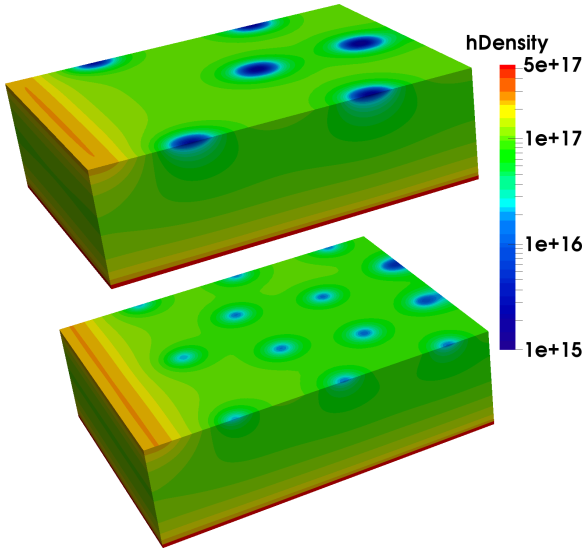

Fig. 3. 3D TCAD simulations of hole density for PCTs with the same shorted area but with different short size. The top part of the structures is clipped off at 50 μm[14].

Since large area thyristors include a complex amplifying gate structure, necessary to reduce the triggering current, designing a highly uniform short pattern is not simple. The short design procedure proposed in [15] is based on a Delaunay triangulation of the cathode. Optimizing for triangles as close to equilateral triangles as possible, as shown in Fig. 5, reduces the overall variance of the short distance and eliminates extreme outliers, which are a reliability concern.

V. Analysis of dI/dt with 3D TCAD simulations

Shorts also affect the turn-on process and in particular the plasma spreading velocity [16], limiting the dI/dt [2][3].

Previous studies of the effects of shorts on turn-on and dI/dt infer the device behavior from the dynamic forward

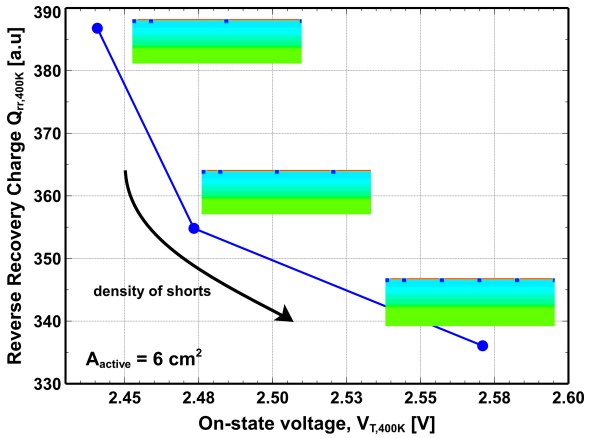

Fig. 4. Simulated tradeoff between V_T and Q_{rr} for structures with varying total shorted cathode area. V_T is simulated at a current $I_T = 4\,kA$, while Q_{rr} is obtained at $I_T = 2\,kA$, $T = 400\,K$, with snubber parameters $R_S = 20\,\Omega$ and $C_S = 5\,\mu F$ [14].

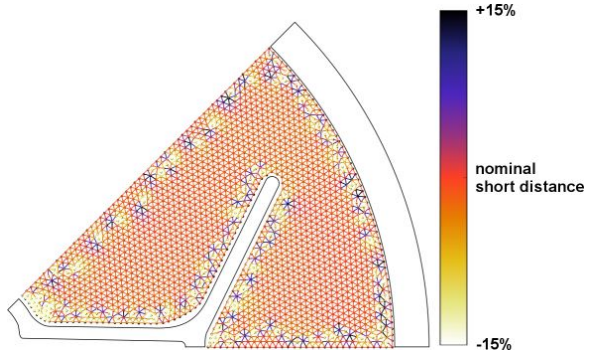

Fig. 5. Illustration of a triangulation-based short placement technique, based on a spatial partitioning algorithm. The geometrical distances of the structures and the short distances have been altered for improved readability. The color of the segments represents the variation from the desired short distance and indicates the uniformity of the short placement [15].

drop on samples with different short configurations [17], from IR imaging [18], from reflection of microwave energy [19], or from localized voltage probing of the p base - cathode junction [20][21][22].

The simulation structures used in [8] are adequate to understand the impact of shorts on dV/dt, ruggedness and breakdown voltage. To understand in greater depth the effects on dI/dt, much more complex structures with a realistic short pattern are simulated. To keep the mesh below 1.5 million points a very dense short pattern is used, which is the most interesting case for practical applications.

Fig. 6 illustrates the PCT turn-on combining a horizontal slice showing the electron current density (J_e) in the p base under the cathode with a 3D isosurface of J_e through the device. The insert in the top shows the short configuration for the device. Importantly, the shorts indicated by the green ellipse exhibit a higher proximity to other shorts.

The turn-on process is greatly affected by the distance and position of the shorts, as can be seen in Fig. 7, which shows a 2D cut of the electrostatic potential and the components of the

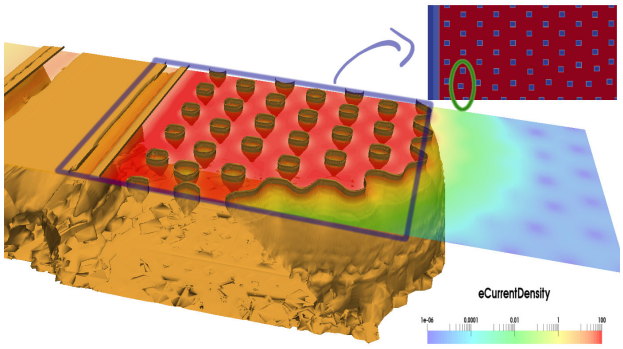

Fig. 6. 3D TCAD simulation showing the turn-on of a PCT. As shown in the inset on the top, the short pattern is not completely regular. The green ellipse highlights two shorts with a noticeably smaller distance from the others. The main figure is composed by a horizontal slice showing the electron current density (J_e) in the p base, a few microns under the cathode and by the 3D isosurface for $J_e = 5A/cm^2$.

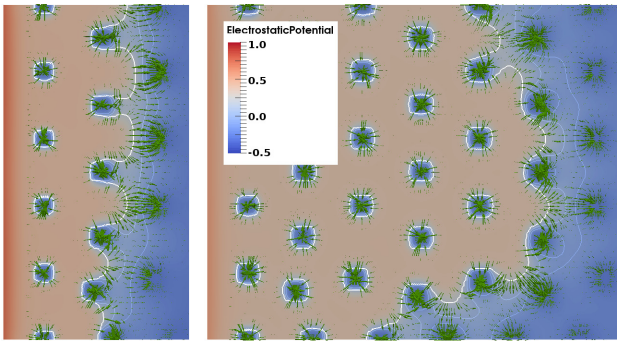

Fig. 7. This figure shows the electrostatic potential in the p base, in a horizontal slice a few microns under the cathode for two instants in time. The white contour line indicates the isosurface for the $J_e = 1A/cm^2$. The arrows show the components of the electric field in the horizontal plane.

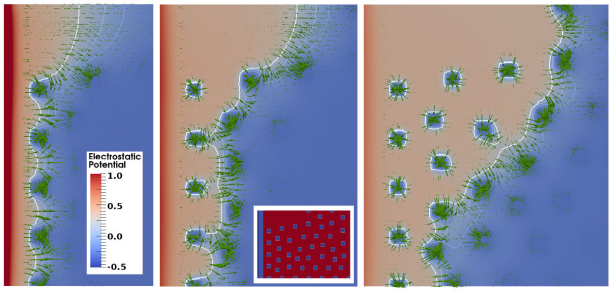

Fig. 8. This figure performs the same analysis of Fig. 7 on the short pattern represented in the inset. As indicated in the inset, a number of shorts in the top part of the structure are intentionally omitted.

electric field in the same horizontal plane depicted in Fig. 6. Also, Fig. 6 indicates that, due to diffusion, the conducting region of the thyristor in the drift layer significantly extends in the radial direction with respect to the the conducting area of the cathode.

Fig. 6 additionally shows that shorts affect the current at significant depths in the p base: a higher local short density hinders the current flow in the radial direction and slows down the cathode turn-on.

Simulations indicate that once the AG is ignited, diffusion spreads carriers from the center to the edge of the device. However, in the p base the voltage difference between the conducting and non-conducting part of the base results in an electric field that has two effects. First, this electric field generates a electron drift current that hinders the diffusion of electrons in the p-base [23]. The electric field also partially aids the drift of holes toward the non-conducting region of the p base. However, part of these holes are diverted to the shorts, thereby limiting the available base current and the turn-on speed. Dense cathode shorting and deep shorts exacerbate this effect, draining base current from the npn transistor.

By contrast Fig. 8 shows how careful localized removal of shorts can significantly increase the current spreading [17].

VI. Conclusion

This work presents a review of current understanding of the role of shorts in Phase Controlled Thyristors (PCTs) and extends the applicability of large scale 3D simulations of PCTs, offering additional insight on the behavior of inrush current and dI/dt capability. The impact of short patterns is discussed with the aid of ad-hoc visualizations.

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