A Simulation Model for SiC Power MOSFET Based on Surface Potential

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***Abstract*—In this paper, we propose a surface-potential-based simulation model of SiC power MOSFETs for accurate circuit simulation. By considering physical structure and behavior of vertical power SiC MOSFETs, the proposed model reproduces static and dynamic characteristics upon wide range of bias voltages. Through experiments using a commercial SiC power MOSFET, good agreements have been observed between measurement and simulation in I-V, C-V characteristics. Good match in transient behavior beyond 1 MHz is also confirmed.**

***Index Terms*—Silicon Carbide, Power MOSFET, Device modeling, Surface potential, Circuit simulation**

I. Introduction

Silicon Carbide (SiC) is one of the most expecting materials to realize high-frequency switching power converters that operate in high-currents and voltages with low power loss [1], [2]. As the operating frequency of the power converters becomes higher, design optimization using circuit simulators becomes an increaslingly important step. The simulation accuracy for power converters that utilizes SiC power MOSFETs highly depends on the accuracy of simulation model of the MOSFETs. It is increasingly important to precisely model behaviors of SiC power MOSFETs for accurate circuit simulations.

In the analysis of power converters using SiC devices, silicon-based empirical models have been applied [3], [4]. However, the fitting of those models to the characteristics of SiC power MOSFETs, such as dc currents and capacitance, is not necessarily satisfactory. Recently, surface-potential-based compact models have been successfully applied for simulating lateral silicon devices [5], [6].

In this work, we propose an accurate SiC power MOSFET model that is based on surface potential. The proposed model assumes the vertical MOSFET structure, shown in Fig. I, which is widely used in high-breakdown-voltage applications. In the proposed model, I-V and C-V characteristics are represented on the basis of device physics, forming an equivalent circuit as shown in Fig. 2. Through experiments on a commercial SiC device, accuracy of the proposed model has been verified, for the first time, beyond kW range to comprehensively cover typical operating regions of practical power converters. Table I provides the nomenclature for the symbols and parameters used in our proposed model.

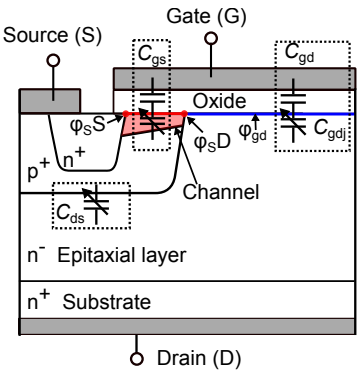

Fig. 1. Cross section of a SiC power MOSFET cell.

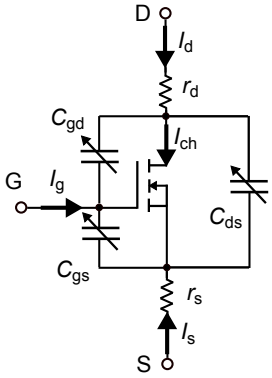

Fig. 2. Equivalent circuit of SiC power MOSFET.

II. Simulation model of SiC power MOSFET

A. Surface potential

In the proposed model, a surface potential ϕ_s of a channel formed in the p^+ region is computed. By applying Gauss's law, Q_s, the total charge density at the MOS interface, is derived from the Poisson equation shown in Eq. (1). In addition, Q_s can also be expressed as a product of C_{ox} and V_{ox}, as represented in Eq. (2), from the charge neutrality condition at the MOS interface. In Eq. (2), $C_{ox} = \varepsilon_{ox}/\mathbf{TOX}$. Eliminating Q_s from Eqs. (1) and (2), a nonlinear equation Eq. (3) for ϕ_s is derived. Then, charge of the inversion layer is calculated from ϕ_s.

$$Q_s = \sqrt{2q\varepsilon_{SiC}\cdot\mathbf{NA}}\sqrt{\phi_t e^{-\phi_s/\phi_t} + \phi_s - \phi_t + e^{-(2\phi_F+\phi_f)/\phi_t}(\phi_t e^{\phi_s/\phi_t} - \phi_s - \phi_t)} \tag{1}$$

$$Q_s = C_{ox}V_{ox} = C_{ox}(V_{gs} - \mathbf{VFBC} - \phi_s) \tag{2}$$

$$C_{ox}(V_{gs} - \mathbf{VFBC} - \phi_s) = \sqrt{2q\varepsilon_{SiC}\cdot\mathbf{NA}}\sqrt{\phi_t e^{-\phi_s/\phi_t} + \phi_s - \phi_t + e^{-(2\phi_F+\phi_f)/\phi_t}(\phi_t e^{\phi_s/\phi_t} - \phi_s - \phi_t)} \tag{3}$$

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By integrating the charge from the drain to the source of the channel, a channel current $I_{\rm ch}$ is derived. Also, the derivative of the surface potential gives a capacitance at the channel of the MOSFET. In [5]–[8], the surface potential $\phi_{\rm s}$ is derived by solving the nonlinear equation shown in Eq. (3).

B. I-V characteristic

In the proposed model, constant **RD** and **RS** represent the drain and source parasitic resistances, respectively. In the rest of this paper, drain and source voltages in the model calculation, $V_{\rm ds}$ and $V_{\rm gs}$, are the effective voltages considering voltage drop of the parasitic resistances.

The inverted charge of the channel is described as the function of the surface potential. Hence, the channel current $I_{\rm ch}$ can be computed by $\phi_{\rm sS}$ (derived by calculating Eq. (3) at $\phi_{\rm f} = 0$) and $\phi_{\rm sD}$ (derived by calculating Eq. (3) at $\phi_{\rm f} = V_{\rm ds}$), as follows [4,5,7]:

$$I_{\rm ch} = \mathbf{K} \cdot I_{\rm DD}, \tag{4}$$

$$\begin{aligned} I_{\rm DD} &= C_{\rm ox}(V_{\rm gs} - \mathbf{VFBC} + \phi_{\rm t})(\phi_{\rm sD} - \phi_{\rm sS}) \\ &- \frac{1}{2}C_{\rm ox}(\phi_{\rm sD}^2 - \phi_{\rm sS}^2) \\ &-\frac{2}{3}\phi_{\rm t}\sqrt{2\varepsilon_{\rm SiC}kT\cdot\mathbf{NA}}\left\{(\frac{\phi_{\rm sD}}{\phi_{\rm t}}-1)^{3/2}-(\frac{\phi_{\rm sS}}{\phi_{\rm t}}-1)^{3/2}\right\} \\ &+\phi_{\rm t}\sqrt{2\varepsilon_{\rm SiC}kT\cdot\mathbf{NA}}\left\{(\frac{\phi_{\rm sD}}{\phi_{\rm t}}-1)^{1/2}-(\frac{\phi_{\rm sS}}{\phi_{\rm t}}-1)^{1/2}\right\} \end{aligned} \tag{5,6}$$

where $\mathbf{K} = M \cdot \mu \cdot (W/L)$ and it is treated as a current gain factor. By considering channel length modulation and mobility degradation, Eq. (9) is rewritten as follows [7]:

$$I_{\rm ch} = \frac{1}{1+\mathbf{THETA}\cdot V_{\rm gs}}(1+\mathbf{LAMBDA}\cdot V_{\rm ds})\cdot\mathbf{K}\cdot I_{\rm DD}. \tag{7}$$

$V_{\rm ds_{mod}}$ is defined to replace $V_{\rm ds}$ in Eq. (6) to represent smooth transition between linear and saturation regions:

$$V_{\rm ds_{mod}} = \frac{V_{\rm ds}}{\left[1+(\frac{V_{\rm ds}}{V_{\rm gs}})^{\mathbf{DELTA}}\right]^{1/\mathbf{DELTA}}}, \tag{8}$$

where **DELTA** is a parameter to compensate mismatches of pinch-off voltages between measurement and simulation due to the gradual channel approximation [4,5].

The terminal currents, $I_{\rm d}$, $I_{\rm s}$, and, $I_{\rm g}$, in the MOSFET are obtained as follows:

$$I_{\rm d} = I_{\rm ch} + \frac{{\rm d}Q_{\rm ds}}{{\rm d}t} - \frac{{\rm d}Q_{\rm gd}}{{\rm d}t}, \tag{9}$$

$$I_{\rm s} = -I_{\rm ch} - \frac{{\rm d}Q_{\rm ds}}{{\rm d}t} - \frac{{\rm d}Q_{\rm gs}}{{\rm d}t}, \text{ and} \tag{10}$$

$$I_{\rm g} = \frac{{\rm d}Q_{\rm gs}}{{\rm d}t} + \frac{{\rm d}Q_{\rm gd}}{{\rm d}t}. \tag{11}$$

Here, $Q_{\rm gs}$, $Q_{\rm ds}$, and $Q_{\rm gd}$ are charges stored in each terminal capacitance described in Sec. II-C.

C. C-V characteristic

As shown in Fig. 2, the simulation model of a power MOSFET consists of three terminal capacitances: gate-source capacitance $C_{\rm gs}$, drain-source capacitance $C_{\rm ds}$, and gate-drain capacitance $C_{\rm gd}$. In particular, $C_{\rm ds}$ and $C_{\rm gd}$ are highly nonlinear and have considerable impacts on the transient characteristic of the high-frequency switching process [4], [9]. In the proposed model, the three capacitances are modeled as follows:

$$C_{\rm gs} = \mathbf{CGS0}, \tag{12}$$

$$C_{\rm ds} = \mathbf{ADS}\cdot\varepsilon_{\rm SiC}\sqrt{\frac{q\cdot\mathbf{ND}}{2\varepsilon_{\rm SiC}(\mathbf{VBI}+V_{\rm ds})}}, \text{ and} \tag{13}$$

$$C_{\rm gd} = \mathbf{COXD} \parallel C_{\rm gdj}. \tag{14}$$

The gate-source capacitance $C_{\rm gs}$ is a series capacitance of the nonlinear MOS capacitance formed at the channel surface and the constant gate oxide capacitance. The change of the MOS capacitance depends on $\phi_{\rm s}$. However, in the proposed model, $C_{\rm gs}$ is approximated using a constant capacitance **CGS0** as shown in Eq. (12), because the change of the MOS capacitance can be considered insignificant as compared to $C_{\rm ds}$ and $C_{\rm gd}$.

The drain-source capacitance $C_{\rm ds}$ is a bias-dependent junction capacitance which changes with depletion at the PN junction between the $\rm p^+$ region and the $\rm n^-$ epitaxial layer as shown in Fig. I. Hence, $C_{\rm ds}$ is calculated based on the capacitance model of the PN junction as represented in Eq. (13).

The gate-drain capacitance $C_{\rm gd}$ is given by Eq. (14), which is a series capacitance of gate oxide capacitance **COXD** and MOS capacitance $C_{\rm gdj}$. With considering the body effect [8], $C_{\rm gdj}$ is a function of the surface potential $\phi_{\rm gd}$ of the hole channel formed on the drain region under the JFET region as shown in Fig. I. Here, $C_{\rm gdj}$ is represented in Eq. (15). $\phi_{\rm gd}$ is computed similarly to the $\phi_{\rm s}$ calculation using Eq. (3) by replacing ($V_{\rm gs}, \phi_{\rm f}, \mathbf{NA}$, **VFBC**) with ($V_{\rm gd}, V_{\rm ds}, \mathbf{ND}$, **VFBD**), respectively.

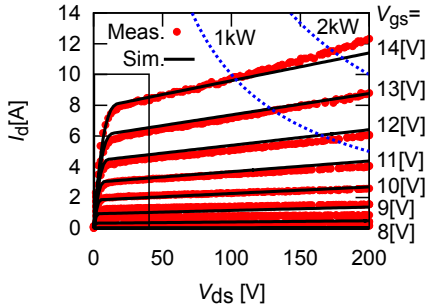
$Q_{\rm gs}$, $Q_{\rm ds}$, and $Q_{\rm gd}$ in Eqs. (9), (10), and (11) are derived as products of capacitances and time derivatives of voltages as follows:

$$Q_{\rm gs} = C_{\rm gs}\frac{{\rm d}V_{\rm gs}}{{\rm d}t}, \tag{16}$$

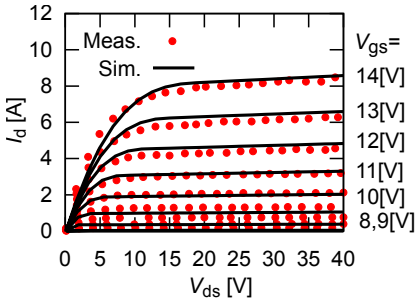
$$Q_{\rm ds} = C_{\rm ds}\frac{{\rm d}V_{\rm ds}}{{\rm d}t}, \text{ and} \tag{17}$$

$$Q_{\rm gd} = C_{\rm gd}\frac{{\rm d}V_{\rm gd}}{{\rm d}t}. \tag{18}$$

$$C_{\rm gdj} = \mathbf{AGD}\cdot\sqrt{2q\varepsilon_{\rm SiC}\cdot\mathbf{ND}}\,\frac{1-e^{-\phi_{\rm gd}/\phi_{\rm t}}+e^{-(2\phi_{\rm F}+V_{\rm ds})/\phi_{\rm t}}(e^{\phi_{\rm gd}/\phi_{\rm t}}-1)}{2\sqrt{\phi_{\rm t}e^{-\phi_{\rm gd}/\phi_{\rm t}}+\phi_{\rm gd}-\phi_{\rm t}+e^{-(2\phi_{\rm F}+V_{\rm ds})/\phi_{\rm t}}(\phi_{\rm t}e^{\phi_{\rm gd}/\phi_{\rm t}}-\phi_{\rm gd}-\phi_{\rm t})}} \tag{15}$$



(a) $0\,\mathrm{V} \leq V_{\mathrm{ds}} \leq 200\,\mathrm{V}$



(b) $0\,\mathrm{V} \leq V_{\mathrm{ds}} \leq 40\,\mathrm{V}$

Fig. 3. Measured and simulated I-V characteristics.

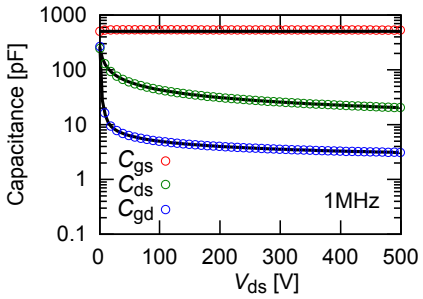


Fig. 4. Measured and simulated C-V characteristics.

III. Experimental Results

To validate the proposed model, I-V, C-V, and transient characteristics are compared to measurement results on a commercial SiC power MOSFET (ROHM, SCT2450KE, 1200 V, 10 A [10]). The I-V curves of the SiC power MOSFET have been obtained by using a dedicated curve tracer that utilizes very short pulse to avoid self-heating effect [11]. The C-V curves have been measured by a commercial curve tracer (Keysight Technologies, B1505A [12]) at 1 MHz. The proposed surface-potential-based model has been implemented using Verilog-A. I-V, C-V, and transient characteristics are calculated by a commercial circuit simulator (SIMetrix Technologies, SIMetrix [13]). Model parameters are determined by a simulated annealing method [14].

The measured and simulated I-V and C-V characteristics are shown in Figs. 3 and 4. The proposed model accurately reproduces wide range of the I-V and C-V characteristics of the SiC MOSFET. In Fig. 3(a), dashed lines express contours of the power dissipation. It should be noted that our model

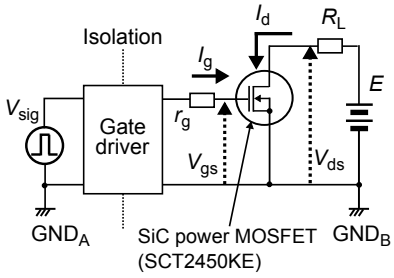


Fig. 5. Resistive load switching circuit.

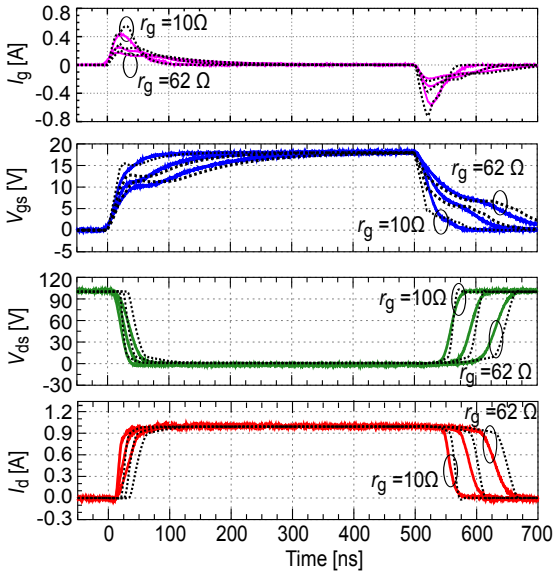


Fig. 6. Measured (solid) and simulated (dashed) gate current (I_{g}), gate-source voltage (V_{gs}), drain-source voltage (V_{ds}), and drain current (I_{d}) waveforms of the SiC power MOSFET in 1 MHz operation.

can accurately simulate the I-V curve in the high-power region of more than 1 kW in which practical high-power converters operate. Figure 3(b) shows the I-V curves in the rectangle at the left bottom of Fig. 3(a). From Fig. 3(b), a good agreement between simulation and measurement is also observed in the low-power region.

The transient waveforms are also compared to the measurement of a switching circuit with a resistive load as shown in Fig. 5. The parasitic impedances of the packages and the passive components have been measured with an impedance analyzer (Agilent Technologies, 4294A [15]), and the impedances are modeled in the transient simulation. The drain supply voltage E and the resistive load R_{L} are 100 V and 100 Ω, respectively. The gate pulse voltage V_{sig} is 18 V and its switching frequency is 1 MHz. The gate series resistance r_{g} is varied ($r_{\mathrm{g}} = \{10, 33, 62\ \Omega\}$). Figure 6 shows both simulated (dashed) and measured (solid) waveforms. From Fig. 6, the proposed model can simulate the high-speed switching waveforms of the SiC power MOSFET successfully for all r_{g} values.

IV. Conclusion

In this paper, a surface-potential-based simulation model for SiC power MOSFETs is proposed. In the proposed model, I-V and C-V characteristics are consistently represented by the surface potential equations that reflect the structure of the vertical power MOSFET. Experimental results using a commercial SiC power MOSFET show that the proposed simulation model successfully reproduces I-V and C-V characteristics, and accurate transient simulations at high frequencies become possible.

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TABLE I
List of Symbols (Model parameters in **bold**)

Symbol	Description
k	Boltzmann's constant [J/K]
q	Elementary charge [C]
T	Absolute temperature [K]
$\varepsilon_{\mathrm{SiC}}$	Permittivity of SiC [F/m]
$\varepsilon_{\mathrm{ox}}$	Permittivity of gate oxide [F/m]
L	Channel length [m]
W	Channel width [m]
M	Number of MOSFET cells [-]
μ	Channel mobility [$\mathrm{cm}^2/\mathrm{Vs}$]
ϕ_{F}	Fermi level [V]
ϕ_{f}	Quasi-fermi level [V]
ϕ_{t}	Thermal voltage (kT/q)[V]
ϕ_{s}	Surface potential [V]
ϕ_{sS}	Surface potential at the source side [V]
ϕ_{sD}	Surface potential at the drain side [V]
ϕ_{gd}	Surface potential of the drain depletion layer under the gate [V]
V_{ox}	Electric potential at the gate oxide [V]
I_{ch}	Current through MOSFET channel [A]
I_{d}	Drain current [A]
I_{g}	Gate current [A]
I_{s}	Source current [A]
V_{gs}	Effective gate-source voltage [V]
V_{ds}	Effective drain-source voltage [V]
V_{gd}	Effective gate-drain voltage [V]
C_{ox}	Oxide capacitance per unit area [F/cm^2]
C_{gs}	Gate-source capacitance [F]
C_{ds}	Drain-source capacitance [F]
C_{gd}	Gate-drain capacitance [F]
C_{gdj}	Gate-drain junction capacitance [F]
Q_{gs}	Charge stored in C_{gs} [F]
Q_{ds}	Charge stored in C_{ds} [F]
Q_{gd}	Charge stored in C_{gd} [F]
	I-V model parameters
TOX	Oxide thickness [m]
VFBC	Flat-band voltage of channel region [V]
NA	Acceptor concentration [cm^{-3}]
K	Current gain factor [cm^2/V]
RS	Parasitic resistance at the source side [Ω]
RD	Parasitic resistance at the drain side [Ω]
LAMBDA	Channel length modulation [1/V]
THETA	Channel mobility degradation [1/V]
DELTA	Smoothing parameter for gradual transition between linear and saturation regions [-]
	C-V model parameters
CGS0	Gate-source capacitance (constant) [F]
ADS	Drain-source overlap area [cm^2]
ND	Donor concentration [cm^{-3}]
VBI	Built-in potential of PN junction [V]
COXD	Gate-drain oxide capacitance [F]
AGD	Gate-drain overlap area [cm^2]
VFBD	Gate-drain flat-band voltage [V]