Performance Evaluation of FinFETs: from Multisubband BTE to DD Calibration

(Invited Paper)

Seonghoon Jin, Anh-Tuan Pham, Woosung Choi
Device Lab, AHQ(DS) R&D
Samsung Semiconductor Inc.
San Jose, CA, USA
Email: s.jin@samsung.com

Mohammad Ali Pourghaderi, Jongchol Kim,
Keun-Ho Lee
Semiconductor R&D center
Samsung Electronics
Hwasung-si, Gyeonggi-do, Korea

Abstract—This paper presents a hierarchical approach to link the advanced multisubband Boltzmann transport equation (MSBTE) solver to the conventional drift-diffusion (DD) model for performance evaluation of non-planar transistors in logic technology development. An automated, physics-based procedure to extract the DD model parameter set from the MSBTE simulation is described. An update on the surface roughness scattering model valid for finite barriers is also shown. As an application, the MSBTE to DD calibration is performed for a silicon nanowire transistor. The calibrated parameter set is applied to a dual channel nanowire transistor, and the effects of the source/drain series and contact resistances are studied.

I. INTRODUCTION

The increased complexities of logic technology introduced by new channel materials, strains, novel 3D structures, and intrinsic/extrinsic variations have made TCAD simulation an essential part of technology development. Although the macroscopic approach based on the drift-diffusion (DD) equation has been and will continue to be the workhorse of the TCAD device simulation, it requires in advance model parameter calibrations from experiment or from more advanced transport models in order to retain its predictability in nanoscale feature size.

As a complementary tool, a microscopic approach based on the multisubband Boltzmann transport equation (MSBTE) has recently gained significant attention as it captures the essential physics of nanoscale transistors such as bandstructure (and its quantization/stress response), quasi-ballistic transport, and microscopic scattering mechanisms [1]–[5]. In addition, the reduction of the transistor size (simulation domain) and the advancement of the computational power and parallel computing have made the approach a practical solution for early stage path finding work. A few commercial TCAD software vendors also start to provide MSBTE solvers [6], [7].

Within the MSBTE framework, accuracy strongly depends on the employed bandstructure (Hamiltonian) and scattering models. As an update to the MSBTE framework, we will cover our recent improvement on the surface roughness (SR) scattering model for finite barriers in Section II.

We have found that bridging the DD and MSBTE is a key factor for successful adoption of the MSBTE solver to real technology development since we still need to heavily rely on the DD simulations in order to properly take into account realistic process conditions, complex 3D topography, and various non-ideal effects. In [3], [4], we tried to overcome the limitations of the DD and the MSBTE solvers to some degree by introducing a coupled DD/MSBTE solver where the MSBTE is solved in the channel region and the DD equation is solved in the source/drain region. However, this approach has several drawbacks in terms of computational burden and flexibility to be used for wider applications.

In this work, we choose to take a more standard, hierarchical procedure as follows:

- Perform MSBTE simulation for the intrinsic part of transistors with simplified source/drain geometry.
- Calibrate the DD model parameter set to reproduce the MSBTE simulation results.
- Run DD simulation for realistic device structures where the calibrated parameter set is employed in the intrinsic part of the device.

In order to achieve the above workflow, it is essential to have an efficient and automated procedure to extract the DD model parameter set from the MSBTE simulation results. Our approach on this topic will be presented in Section III.

In Section IV, we will show the detailed MSBTE as well as the calibrated DD simulation results for single and dual channel gate-all-around (GAA) nanowire FET (NWFET) structures. Conclusion will be followed in Section V.

II. SR SCATTERING FOR FINITE BARRIERS

SR scattering due to the asperity of the semiconductor/insulator (SI) interfaces is one of the key scattering mechanisms in non-planar transistors especially when the geometric quantization is strong [8], [9]. The SR scattering model derived in [3] is applicable for general 2D cross sections for the $\mathbf{k} \cdot \mathbf{p}$ Hamiltonian as long as the wavefunction penetration can be neglected. In this paper, we extend this model for finite barriers where the wavefunction penetration needs to be taken into account.
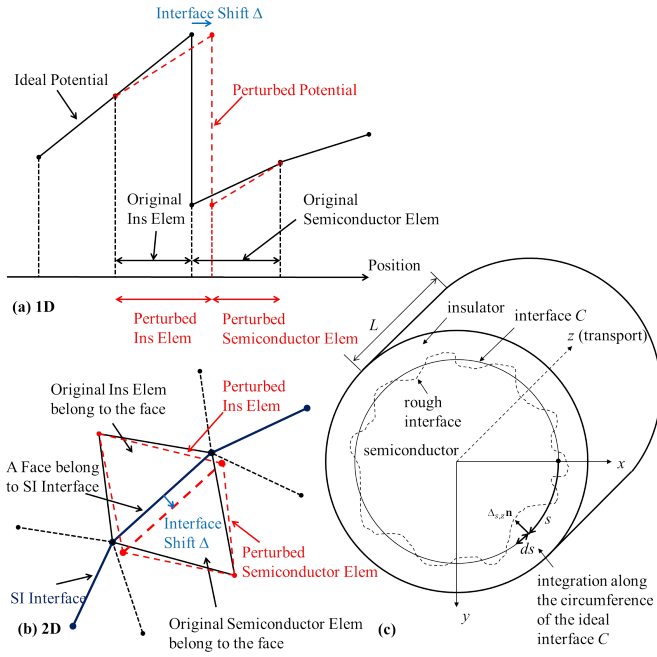
Fig. 1. Schematic diagram of the potential energy and the element volume perturbations near the SI interface due to the SR induced interface shift for the (a) 1D and (b) 2D quantization. For each face belong to the SI interface, the computation of the SR matrix element involves the pair of the neighbor elements belong to the face. Fig. (c) shows the definition of circumference coordinate s, interface normal vector $\mathbf{n}$, and the surface roughness $\Delta_{s,z}$.

We assume that the SR introduces the spatial fluctuations of the SI interface boundary, and these boundary fluctuations perturb the propagating carrier wavefunctions as there exist abrupt changes in the potential and the kinetic energy operators across the interface as shown in Fig. 1.

For an arbitrary 2D cross-section, we define the circumference coordinate s, the interface normal vector $\mathbf{n}$, and the roughness profile $\Delta_{s,z}$ as shown in Fig. 1 (c), where it is assumed that the transport is along the z-direction and the 2D confinement is in the x-y plane.

The matrix element for the SR scattering can be written as [3]:

$$\left\langle \left| V^{SR}_{q_z;\mu\mu'} \right|^2 \right\rangle = \sum_{n=-n_c}^{n_c} \left| \Gamma_{\mu\mu' q_s = \frac{2\pi n}{C}} \right|^2 \left\langle \left| \Delta_{q_s = \frac{2\pi n}{C}, q_z} \right|^2 \right\rangle \quad (1)$$

$$\left\langle \left| \Delta_{q_s,q_z} \right|^2 \right\rangle = \frac{\pi \Delta^2 \Lambda^2}{LC} \left[1 + \frac{\Lambda^2}{2} \left(q_s^2 + q_z^2 \right) \right]^{-\beta} \quad (2)$$

$$\Gamma_{\mu\mu' q_s} = \oint_C ds \sum_{i=1}^{b_{max}} \sum_{j=1}^{b_{max}} \Gamma^{(ij)}_{\mu\mu'}(s) e^{iq_s s} \quad (3)$$

where μ and μ' represent the subband indices for the initial and final states, $q_z = k - k'$ is the 1D momentum transfer, C is the circumference of the interface, Δ is the reference rms value of roughness, Λ is the correlation length, $n_c \approx 2C/(\pi\Lambda)$ is the largest index of the Fourier components of the SR, and

b_{max} is the number of bands (1 for EMA, 6 for six-band $\mathbf{k} \cdot \mathbf{p}$ Hamiltonian, etc.).

When the wavefunction penetration can be neglected, $\Gamma^{(ij)}_{\mu\mu'}(s)$ can be written as [3]:

$$\Gamma^{(ij)}_{\mu\mu'}(s) = \frac{\Delta_{ori}}{\Delta} \left[\left(\nabla \Psi^{(i)*}_\mu \cdot \mathbf{n} \right) H^{(ij)}_{nn} \left(\nabla \Psi^{(j)}_{\mu'} \cdot \mathbf{n} \right) \right]_{sem} \quad (4)$$

with

$$H^{(ij)}_{nn} = \sum_{\alpha=x}^{y} \sum_{\beta=x}^{y} M^{(ij)}_{\alpha\beta} n_\alpha n_\beta \quad (5)$$

where Ψ^i_μ is the wavefunction for $k = 0$. n_α is the α-component of $\mathbf{n}$. $M^{(ij)}_0$ and $M^{(ij)}_{\alpha\beta}$ are the coefficients of the bulk Hamiltonian as:

$$H^{(ij)}_{bulk} = M^{(ij)}_0 + \sum_{\alpha=x}^{z} \sum_{\beta=x}^{z} M^{(ij)}_{\alpha\beta} k_\alpha k_\beta \quad (6)$$

$\Delta_{ori}(s)$ is the surface-orientation-dependent rms value of roughness.

When the wavefunction penetration needs to be considered, (4) can be generalized to:

$$\Gamma^{(ij)}_{\mu\mu'}(s) = \frac{\Delta_{ori}}{\Delta} \left[\left(\nabla \Psi^{(i)*}_\mu \cdot \mathbf{n} \right) H^{(ij)}_{nn} \left(\nabla \Psi^{(j)}_{\mu'} \cdot \mathbf{n} \right) + \right.$$
$$\left. \Psi^{(i)*}_\mu \left(\frac{E_\mu + E_{\mu'}}{2} - U - M^{(ij)}_0 \right) \Psi^{(j)}_{\mu'} \right]_{sem}$$
$$- \frac{\Delta_{ori}}{\Delta} \left[\left(\nabla \Psi^{(i)*}_\mu \cdot \mathbf{n} \right) H^{(ij)}_{nn} \left(\nabla \Psi^{(j)}_{\mu'} \cdot \mathbf{n} \right) + \right.$$
$$\left. \Psi^{(i)*}_\mu \left(\frac{E_\mu + E_{\mu'}}{2} - U - M^{(ij)}_0 \right) \Psi^{(j)}_{\mu'} \right]_{ins} \quad (7)$$

where U is the potential energy.

Note that for each face belong to the SI interface, the computation of (7) involves the pair of the neighbor elements (the semiconductor and the insulator elements) belong to the face as shown in Fig. 1 (a) and (b), whereas the computation of (4) involves only the semiconductor element. In each element (edge in 1D and triangle in 2D), the first term represents the change of the kinetic energy while the second term represents the change of the potential energy and the normalization. For the second term, the element average (over the element-nodes), not the face average, should be performed as it is originated from the element volume change.

Fig. 2 shows the calculated electron mobility as a function of silicon body thickness of symmetric double gate channel depending on the SI boundary condition (BC). When the geometric quantization is not significant (field-driven quantization), the finite barrier BC increases the SR scattering and reduces the SR-limited mobility as it increases the proximity of inversion carriers to the surface. On the other hand, the finite barrier BC increases the SR-limited mobility when the geometric quantization is dominant as it reduces the geometric quantization and the variation of the subband energy. When (4) is used with the finite barrier BC, the SR-limited mobility is overestimated.
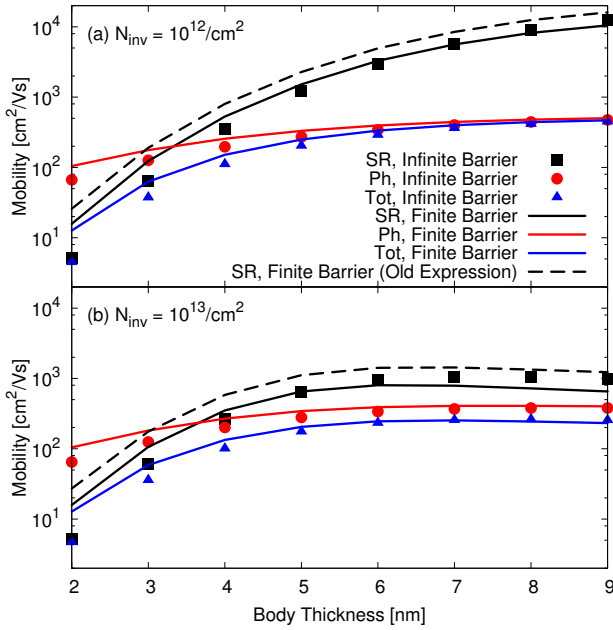
Fig. 2. Comparison of calculated electron mobility as a function of silicon body thickness of symmetric double gate channel depending on the BC. (110) surface orientation/$\langle 110 \rangle$ channel orientation is assumed. When the geometric quantization is not significant, the finite barrier BC increases the SR scattering and reduces the SR-limited mobility as it increases the proximity of inversion carriers to the surface. On the other hand, the finite barrier BC increases the SR-limited mobility when the geometric quantization is dominant as it reduces the geometric quantization and the variation of the subband energy. When (4) is used with the finite barrier BC, the SR-limited mobility is overestimated (dashed line).

Fig. 3. Comparison of calculated and measured ([12]–[14]) inversion layer mobility for (100) and (110) surface orientations and for different silicon body thicknesses [channel direction is along $\langle 110 \rangle$].

III. DD MODEL CALIBRATION

A. Baseline low-field Mobility Model

In order to perform DD simulations for finFETs, we need to calibrate the baseline low-field mobility model for different surface/channel orientations as well as for different degree of geometric quantization effectively represented by a body thickness parameter. We have slightly extended the models from [10], [11] and performed extensive calibrations by using a global optimization technique to reproduce the available experimental data [12]–[14] for different surface/channel orientations and body thicknesses. Fig. 3 compares the calibrated DD mobility and experiment data for different surface orientations and body thicknesses.

B. Automated MSBTE to DD Calibration

For realistic simulations, we eventually need to run the DD simulation. Therefore, a well-defined and efficient procedure to obtain the calibrated DD model parameters from the MSBTE simulation results is highly desirable.

In this work, we propose an automated calibration procedure without a feedback loop for fast turn-around time. The calibration procedure requires the following 8 target variables obtained from the MSBTE simulation:
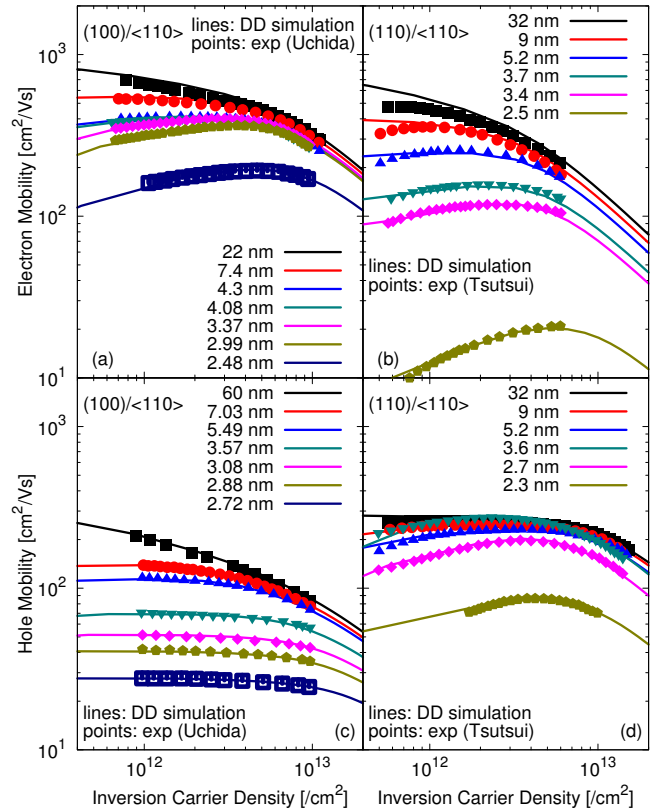
- $N_{\mathrm{inv,off}}$ and $N_{\mathrm{inv,on}}$: equilibrium integrated inversion charge density at the center of the channel when $V_{\mathrm{G}} = 0$ V and V_{GG}.
- μ_{SD}: low-field mobility at the source/drain.
- $\mu_{\mathrm{Ch,mid}}$ and $\mu_{\mathrm{Ch,on}}$: low-field mobility at the center of the channel when $V_{\mathrm{G}} \approx V_{\mathrm{GG}}/2$ and V_{GG}.
- $I_{\mathrm{off,lin}}$, $I_{\mathrm{on,lin}}$, and $I_{\mathrm{on,sat}}$: drain current when $(V_{\mathrm{G}}, V_{\mathrm{D}})$ is $(0, V_{\mathrm{Dlin}})$, $(V_{\mathrm{GG}}, V_{\mathrm{Dlin}})$, and $(V_{\mathrm{GG}}, V_{\mathrm{DD}})$, respectively.

Note that the preparation of the target variables requires only 3 different non-equilibrium MSBTE solutions (in addition to 3 equilibrium solutions which can be obtained efficiently).

Then, we consider the following calibration parameters:

- f_γ: a multiplication factor of the density gradient model parameter γ [15] (we have used an anisotropic density-gradient model [16] where the quantum correction along the channel direction is completely turned-off for consistency with the MSBTE simulation).
- a_{sign}, f_{a}: a sign (± 1) and a multiplication factor of the density gradient high density correction term [4]:

$$\Lambda_{\mathrm{hd}} = -a_{\mathrm{sign}} kT \ln \left[1 + \min \left(n/(n_0 f_{\mathrm{a}}), 10 \right) \right] \quad (8)$$

where n is the electron density and n_0 is the reference density.

- $f_{\mu\mathrm{min}}$: a multiplication factor of the parameter μ_{min} in the Philips unified mobility model [17], which mainly

controls the low-field mobility in the source/drain extensions.

- $f_{\mu Ch}$: a common multiplication factor of the parameter μ_{max} in the Philips unified mobility model [17] and the inversion layer mobility [10], [11], [18], which mainly controls the low-field mobility in the channel region.
- f_{body}: a multiplication factor of the body thickness parameter in the geometric quantization dependent mobility model [10], [11].
- $f_{\mu low}$: a multiplication factor of the total low field mobility (affects the low-field mobility in the entire domain).
- f_{vsat}: a multiplication factor of the saturation velocity.

The calibration procedure is composed of three steps as follows:

1) Calibrate the equilibrium electrostatics by solving for f_γ and $[a_{sign}, f_a]$ to match $N_{inv,off}$ and $N_{inv,on}$, respectively.
2) Calibrate the low-field mobility in the long channel limit by solving for $[f_{\mu min}, f_{\mu Ch}, f_{body}]$ to match $[\mu_{SD}, \mu_{Ch,mid}, \mu_{Ch,on}]$ simultaneously.
3) Calibrate the non-equilibrium transport properties by solving for $[f_\gamma, f_{\mu low}, f_{vsat}]$ to match $[I_{off,lin}, I_{on,lin}, I_{on,sat}]$ simultaneously.

The multi-dimensional Newton-Raphson method is employed in the above procedure where the Jacobian and the rhs are computed in parallel by submitting the necessary DD simulation jobs in a grid engine concurrently. As a result, it takes only about an hour of elapsed time to finish the calibration procedure for the given reference data. As the quantum potential γ factor is re-calibrated at the last step to match the drain current, the fitting of the inversion charge is slightly degraded for the better matching of the drain current. Similarly, the re-calibration of $f_{\mu low}$ at the last step can capture the influence of the quasi-ballistic transport on low-field mobility.

IV. SIMULATION RESULTS

As an application, we consider silicon GAA NWFETs having single and dual channels as shown in Fig. 4. For the MSBTE simulation and the DD calibration, a simplified structure [Fig. 4 (e)] is used. After the calibrated DD parameter set is obtained from the automated procedure, we employ the obtained parameter set to the intrinsic part (including the channel and the source/drain extensions [see Fig. 4 (c)]) of the original structure [Fig. 4 (a) and (b)] and perform DD simulations including extrinsic effects such as the contact resistance. This approach is found to be more practical than the DD/MSBTE coupled scheme [3], [4] when more complex geometries are involved.

In the MSBTE simulations, the electron bandstructure in silicon is modeled in a standard way accounting for the six ellipsoidal valleys with nonparabolic correction [9]. The wavefunction penetration into the oxide is taken into account (oxide effective mass of $0.5\ m_0$ is assumed).

As for the scattering mechanisms, phonon, surface roughness, and Coulomb scattering (due to ionized impurities) are
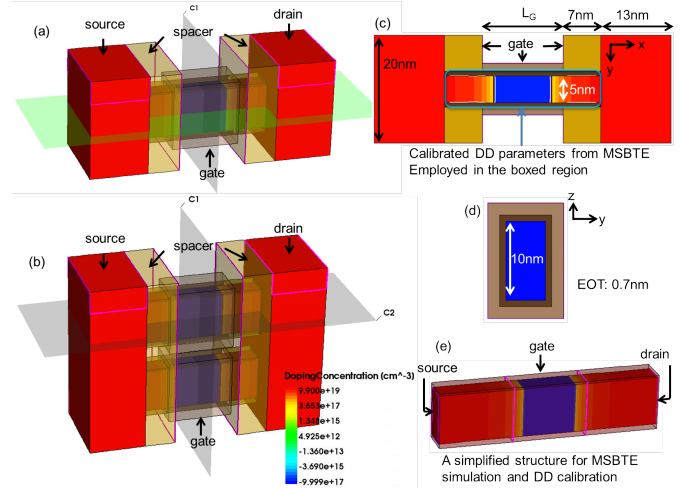

Fig. 4. Simulated silicon GAA NWFET structures with (a) single and (b) dual channel and their 2D cross-sections in (c) $x-y$ plane and (d) $y-z$ plane. The channel is along the $\langle 110 \rangle$ direction with the (110) side walls. The gate length (L_G) is varied from 10 to 50 nm. For the MSBTE simulation and the DD calibration, a simplified structure (e) is employed where the cross-section dimension, effective oxide thickness (EOT), and doping profile are consistent with the original structure while the source and drain is simplified. As for the bias condition, V_{GG} of 0.6 V, V_{Dlin} of 0.05 V, and V_{DD} of 0.5 V are assumed.

included. The Coulomb scattering rate is computed in a rigorous manner [1] (numerical computation/storage of the point charge Green's functions, tensorial screening, etc.), which requires significant computation and memory. In order to reduce the computational burden, the form factors of the Coulomb scattering are computed in a few automatically selected cross-sections based on the change of the integrated total doping concentration. Fig. 5 shows the doping profile along the channel direction and the component-wise electron mobility obtained from the MSBTE simulation. Since the form factors of the Coulomb scattering are not computed in the every slice, there exist somewhat abrupt changes in the Coulomb scattering limited mobility in spite of the smooth doping gradient. However, the drain current error introduced by this approximation is acceptable for the considered structure.

The calculated $I_D - V_G$ curves from the MSBTE simulation and from the calibrated DD simulation for different gate lengths are shown in Fig. 6. The calibrated DD simulation can reproduce the $I_D - V_G$ curves from the MSBTE quite well. In addition to the terminal characteristics, the calibrated DD simulation can provide relatively good overall accuracy in terms of internal quantities such as the average conduction band energy, the average velocity, and the integrated electron density as shown in Fig. 7, which demonstrates that the calibration procedure is not arbitrary, but it actually captures the key features of the MSBTE results in a systematic way. Closer look on Fig. 7 also reveals some differences between the two models due to the intrinsic limitation of the DD model. For example, the MSBTE predicts less potential drop in the drain extension than the source side while the DD model gives symmetric potential drop between the source and
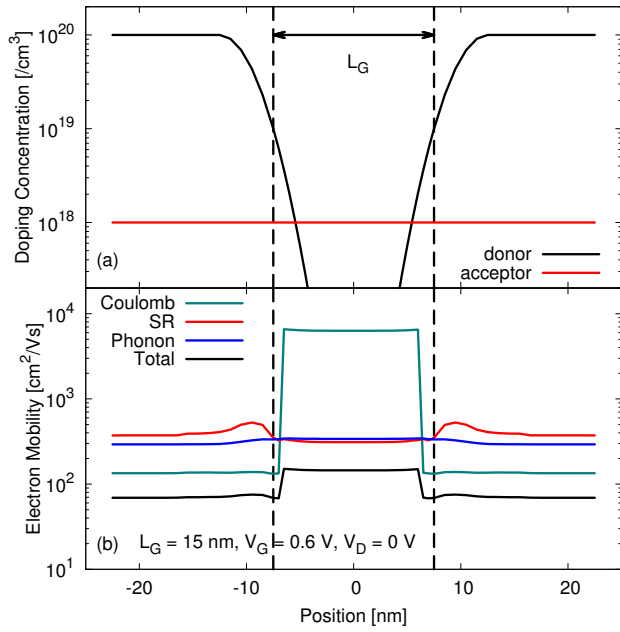
Fig. 5. (a) Doping profile and (b) Component-wise electron mobility obtained from the MSBTE simulation along the channel direction for $L_G = 15$ nm, $V_D = 0$ V, and $V_G = 0.6$ V. Phonon, Coulomb, and surface roughness scattering mechanisms are taken into account.
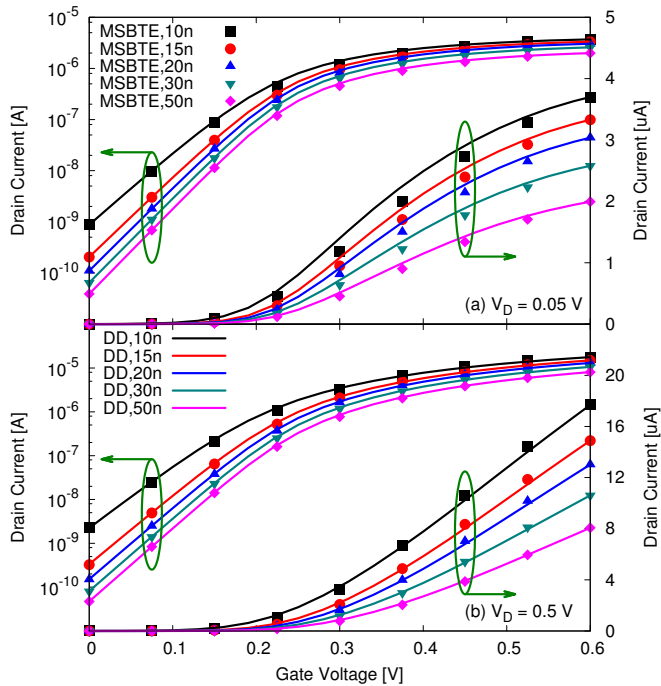
Fig. 6. Comparison of $I_D - V_G$ curves for (a) $V_D = 0.05$ V and (b) $V_D = 0.5$ V obtained from the MSBTE simulation (symbols) and the calibrated DD simulation (lines) for different gate lengths ($L_G = 10$, 15, 20, 30, and 50 nm).
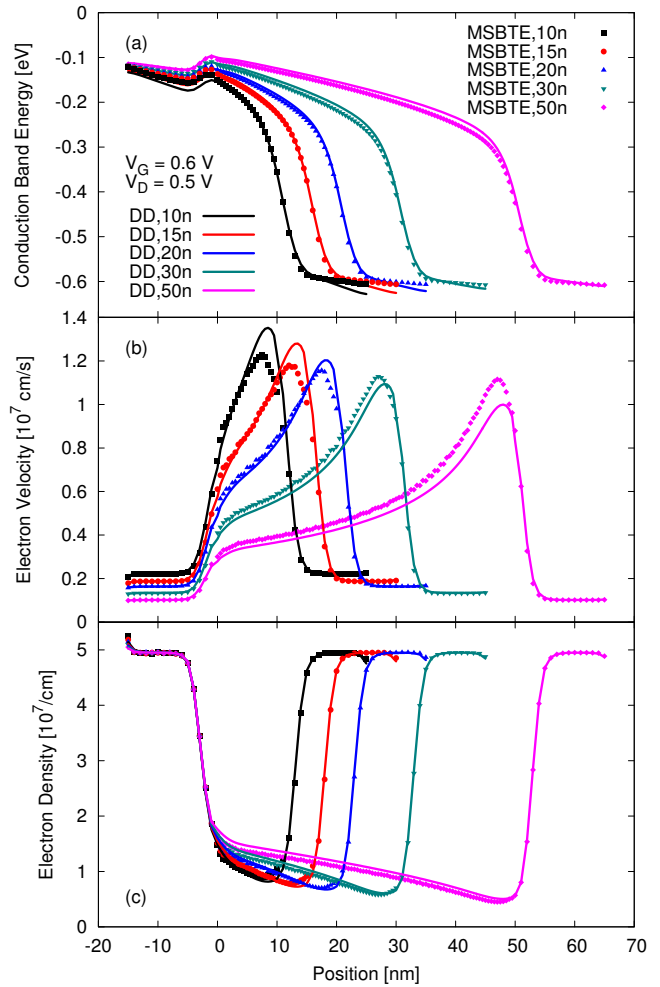
Fig. 7. Comparison of (a) the average conduction band energy, (b) the average electron velocity, and (c) the integrated electron density obtained from the MSBTE simulation (symbols) and the calibrated DD simulation (lines) for different gate lengths ($L_G = 10$, 15, 20, 30, and 50 nm) when $V_D = 0.5$ V and $V_G = 0.6$ V.

drain extensions. It is because the carrier distribution from the MSBTE is not fully thermalized in the drain side while it is near equilibrium in the source side as shown in Fig. 8.

Fig. 9 shows the gate length dependences of the calibration parameters f_{vsat}, f_γ, and $f_{\mu low}$ obtained from the automatic calibration procedure. As the gate length is reduced, the calibrated low-field mobility is reduced while the saturation velocity is enhanced in order to match the I-V curves from the MSBTE simulations. The reduction of the low-field mobility can be attributed to the ballistic mobility [19], whereas the increase of the saturation velocity can be explained by the increase of the average velocity in the channel as electrons experience less scattering.

It is somewhat difficult to understand the gate length dependence of the quantization related parameter f_γ. As we mentioned in Section III-B, f_γ is re-calibrated at the last step to match the drain current. In Fig. 9, we also plot f_γ right
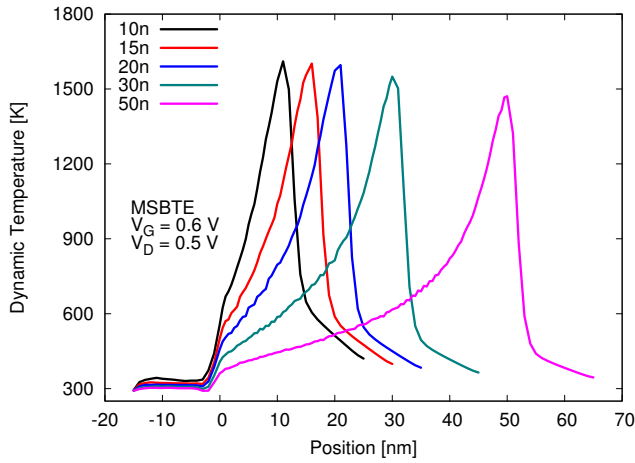
Fig. 8. Calculated dynamic temperature along the channel direction obtained from the MSBTE for different gate lengths ($L_G = 10, 15, 20, 30,$ and 50 nm) when $V_D = 0.5$ V and $V_G = 0.6$ V. The dynamic temperature at the source extension is close to the equilibrium value (≈ 300 K), whereas the temperature at the drain extension is higher due to the incomplete thermalization of electrons injected from the channel.
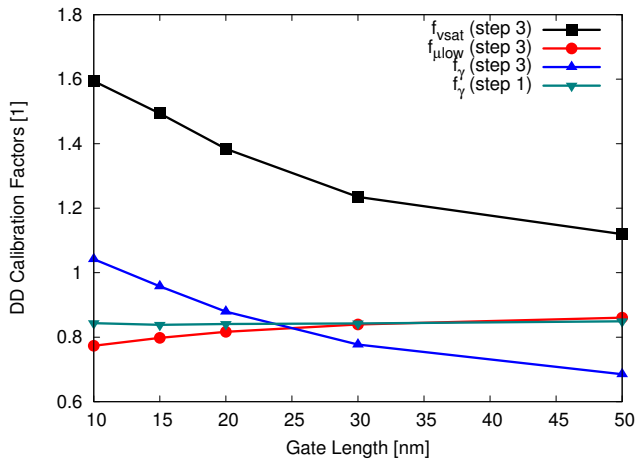

Fig. 9. Gate length dependence of the calibration parameters f_{vsat}, $f_{\mu\text{low}}$, and f_γ obtained from the automatic calibration procedure (Other parameters are not shown as they are determined from the equilibrium conditions and are not sensitive to the gate length). Also shown is f_γ right after the equilibrium off-state inversion charge calibration (green line). Due to the increased portion of the ballistic transport, the low-field mobility is reduced while the saturation velocity is increased with decreasing gate length.

after the off-state inversion charge calibration (step 1), which is more or less independent of the gate length as expected. We think that the gate length dependence of f_γ is closely related to the gate length dependence of f_{vsat}. Increase in f_{vsat} tends to overestimate the carrier velocity in the off state, which is compensated by the increase in f_γ in order to match the off-current. Introducing a bias dependent saturation velocity may remove the gate length dependence of f_γ. According to our study not shown here, however, it does not necessarily improve the accuracy of the overall drain current fitting in spite of the additional complications due to the increased number of parameters.
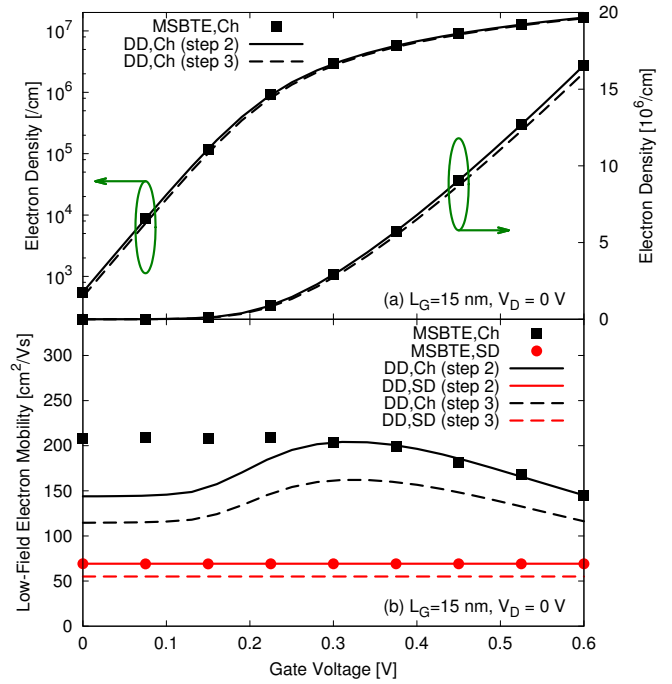

Fig. 10. Comparison of (a) the integrated electron density at the center of the channel and (b) the low-field mobility at the channel (Ch) and at the source/drain (SD) as a function of the gate voltage obtained from the MSBTE (symbols) and from the DD (lines) for $L_G = 15$ nm and $V_D = 0$ V. The non-equilibrium calibration performed at the step 3 slightly degrades the density matching while it improves the current fitting. In addition, the low-field mobility from the DD simulation is reduced at the step 3 to fit the current.

The impact of the non-equilibrium calibration (step 3) on the inversion layer electron density and the low field mobility is shown in Fig. 10.

Using the calibrated DD parameter, we finally perform the DD simulation for the original single and dual channel GAA NWFETs and investigate the influence of the source/drain series and contact resistances in Fig. 11. For the single channel NWFET without the contact resistance, I-V characteristics agree quite well with the simplified structure. Compared with the single channel structure, the dual channel structure gives slightly less drain current per channel due to the increased series resistance in the source/drain. Fig. 12 clearly shows a significant potential drop in the source/drain.

V. CONCLUSION

In this paper, we have presented a hierarchical approach to connect the microscopic MSBTE and the conventional DD model for the performance evaluation of non-planar logic devices. As a key step to this approach, an automated way to calibrate the DD model parameter set from the MSBTE simulation results was shown. We also described a new SR scattering model valid for finite potential barriers when the wavefunction penetration is non-negligible. The proposed hierarchical approach as well as the new SR scattering model were applied to the study of single and dual channel silicon

Simulation of Semiconductor Processes and Devices 2016
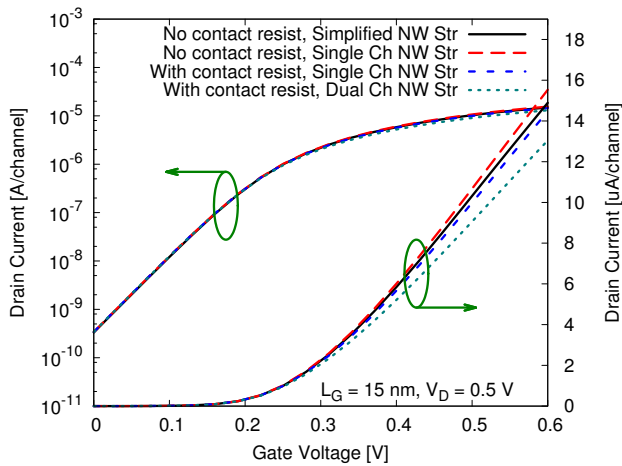Edited by E. Bär, J. Lorenz, and P. Pichler

Fig. 11. Comparison of $I_D - V_G$ curves obtained from the calibrated DD model for the simplified structure, for the original single channel NWFET structure (with/without contact resistance), and for the original dual channel NWFET structure with contact resistance. When the contact resistance is considered, a distributed resistance of 5×10^{-9} Ωcm^2 is assumed at the source/drain contact surface. The drain current is normalized by the number of channels for fair comparison.
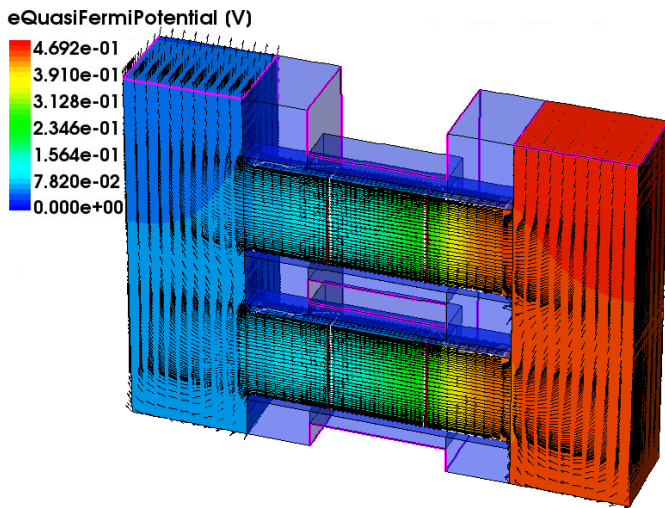

Fig. 12. Calculated electron quasi-Fermi potential and the current vector when $V_D = 0.5$ V, $V_G = 0.6$ V. Potential drop is visible in the source/drain.

NWFETs. Detailed comparison between the MSBTE and the calibrated DD simulation confirmed the validity of the approach. In addition, it also revealed some differences in the internal quantities due to the inherent difference between the two models. The gate length dependence of the calibration parameter set gave us a hint on how we can model the quasi-ballistic effects in the DD model framework. The DD simulation of the dual channel NWFET with the calibrated DD parameter clearly showed the influence of the source/drain and contact resistance on the drain current.

REFERENCES

[1] S. Jin, M. V. Fischetti, and T.-w. Tang, "Theoretical study of carrier transport in silicon nanowire transistors based on the multisubband Boltzmann transport equation," *IEEE Trans. Electron Devices*, vol. 55, no. 11, pp. 2886–2897, 2008.

[2] M. Lenzi, P. Palestri, E. Gnani, S. Reggiani, A. Gnudi, D. Esseni, L. Selmi, and G. Baccarani, "Investigation of the Transport Properties of Silicon Nanowires Using Deterministic and Monte Carlo Approaches to the Solution of the Boltzmann Transport Equation," *IEEE Trans. Electron Devices*, vol. 55, no. 8, pp. 2086–2096, Aug 2008.

[3] S. Jin, S.-M. Hong, W. Choi, K.-H. Lee, and Y. Park, "Coupled Drift-Diffusion (DD) and Multi-Subband Boltzmann Transport Equation (MSBTE) Solver for 3D Multi-Gate Transistors," in *Intl. Conference on Simulation of Semiconductor Processes and Devices*, Glasgow, Sep. 2013, pp. 348–351.

[4] S. Jin, A.-T. Pham, W. Choi, Y. Nishizawa, Y.-T. Kim, K. H. Lee, Y. Park, and E. S. Jung, "Performance evaluation of InGaAs, Si, and Ge nFinFETs based on coupled 3D drift-diffusion/multisubband Boltzmann transport equations solver," in *International Electron Devices Meeting Tech. Digest*, San Francisco, Dec. 2014, pp. 7.5.1–7.5.4.

[5] A.-T. Pham, Z. Jiang, S. Jin, J. Wang, W. Choi, M. A. Pourghaderi, and K.-H. Lee, "On The Efficient Methods To Solve Multi-Subband BTE in 1D Gas Systems: Decoupling Approximations Versus The Accurate Approach," in *Intl. Conference on Simulation of Semiconductor Processes and Devices*, 2016.

[6] L. Smith, M. Choi, M. Frey, V. Moroz, A. Ziegler, and M. Luisier, "FinFET to Nanowire Transition at 5nm Design Rules," in *2015 International Conference on Simulation of Semiconductor Processes and Devices (SISPAD)*. IEEE, 2015, pp. 254–257.

[7] Z. Stanojevic, O. Baumgartner, F. Mitterbauer, H. Demel, C. Kernstock, M. Karner, V. Eyert, A. France-Lanord, P. Saxe, C. Freeman, and E. Wimmer, "Physical modeling – a new paradigm in device simulation," in *2015 IEEE International Electron Devices Meeting (IEDM)*, Dec 2015, pp. 5.1.1–5.1.4.

[8] S. Jin, M. V. Fischetti, and T.-W. Tang, "Modeling of surface roughness scattering in ultrathin-body SOI MOSFETs," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2191–2203, Sep. 2007.

[9] S. Jin, M. V. Fischetti, and T.-w. Tang, "Modeling of electron mobility in gated silicon nanowires at room temperature: Surface roughness scattering, dielectric screening, and band nonparabolicity," *J. Appl. Phys.*, vol. 102, no. 8, p. 083715, Oct. 2007.

[10] L. Silvestri, "Physical Models for Numerical Simulation of Si-Based Nanoscale FETs and Sensors," Ph.D. dissertation, Univ. of Bologna, 2011.

[11] S. Reggiani, E. Gnani, A. Gnudi, M. Rudan, and G. Baccarani, "Low-Field Electron Mobility Model for Ultrathin-Body SOI and Double-Gate MOSFETs With Extremely Small Silicon Thicknesses," *IEEE Trans. Electron Devices*, vol. 54, no. 9, pp. 2204–2212, 2007.

[12] K. Uchida, H. Watanabe, A. Kinoshita, J. Koga, T. Numata, and S. Takagi, "Experimental study on carrier transport mechanism in ultrathin-body SOI n- and p-MOSFETs with SOI thickness less than 5 nm," in *International Electron Devices Meeting Tech. Digest*, San Francisco, Dec. 2002, pp. 47 – 50.

[13] G. Tsutsui, M. Saitoh, and T. Hiramoto, "Experimental Study on Superior Mobility in (110)-Oriented UTB SOI pMOSFETs," *IEEE Electron Device Lett.*, vol. 26, no. 11, pp. 836–838, Nov 2005.

[14] G. Tsutsui and T. Hiramoto, "Mobility and Threshold-Voltage Comparison Between (110)- and (100)-Oriented Ultrathin-Body Silicon MOSFETs," *IEEE Trans. Electron Devices*, vol. 53, no. 10, pp. 2582–2588, Oct 2006.

[15] A. Wettstein, A. Schenk, and W. Fichtner, "Quantum device-simulation with the density-gradient model on unstructured grids," *IEEE Trans. Electron Devices*, vol. 48, no. 2, pp. 279–284, 2001.

[16] J. R. Watling, A. R. Brown, A. Asenov, A. Svizhenko, and M. P. Anantram, "Simulation of direct source-to-drain tunneling using the density gradient formalism: Non-equilibrium green's function calibration," in *Intl. Conference on Simulation of Semiconductor Processes and Devices*, Kobe, Sep. 2002, p. 267.

[17] D. Klaassen, "A unified mobility model for device simulation-i. model equations and concentration dependence," *Solid-State Electronics*, vol. 35, no. 7, pp. 953–959, 1992.

[18] M. Darwish, J. Lentz, M. Pinto, P. Zeitzoff, T. Krutsick, and H. Vuong, "An improved electron and hole mobility model for general purpose device simulation," *IEEE Trans. Electron Devices*, vol. 44, no. 9, p. 1529, Sep. 1997.

[19] M. S. Shur, "Low ballistic mobility in submicron HEMTs," *IEEE Electron Device Lett.*, vol. 23, no. 9, pp. 511–513, 2002.