

# A possible explanation of the record electrical performance of silicon nanowire tunnel FETs with silicided source contact

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**Abstract** — Some experimentally implemented silicon nanowire tunnel FETs with silicided source contacts show an unexpectedly high electrical performance. Simulations using state-of-the-art simulation models and assuming usual device geometries cannot explain the high performance of these transistors: Conventional simulations of such tunnel FETs predict an on-state current which is several orders of magnitude lower than measured. In this work we show that thin silicide nano-spikes extending from the silicided source contact into the silicon channel of the nanowire tunnel FET could be a possible explanation of the high tunnel FET performance observed experimentally.

**Keywords** — nanowire tunnel FET; silicon; silicide; columnar; transfer characteristics;

## I. INTRODUCTION

Some experimentally implemented nanowire tunnel FETs [1–2] exhibit an unexpectedly high electrical performance. For example, the on-current of a p-channel type tunnel FET [1] built on a columnar silicon nanowire of 18 nm diameter amounts to 2.6 A/m. The sharpest inverse sub-threshold slope  $S$  of this tunnel FET is below 30 mV/dec and the current range with a slope below 50 mV/dec covers almost three decades of the current change. For a further comparison with independent simulation results it should be noted that the experimentally measured inverse sub-threshold slope is the lower the smaller the diameter of the nanowire is.

On the other hand side, theoretical predictions of on-currents and of sub-threshold slopes for silicon nanowire tunnel FETs do not forecast such a high performance. For example, in a full quantum mechanical simulation which also accounts for the phonon-assisted tunneling [3] the on-current for a silicon nanowire tunnel FET with a diameter of 3 nm and a gate length of 15 nm was predicted to be 0.031 A/m, and the minimum inverse sub-threshold was only slightly below 60 mV/dec. These simulated performance parameters are much below the ones achieved experimentally on the silicon nanowire tunnel FETs [1–2] with more relaxed device dimensions, a nanowire diameter of 18 nm and a gate length of 140 nm.

We summarize: The reported measured on-state-current of a specific TFET with relaxed geometrical dimensions is more than a factor of 80 higher than the on-state current predicted with the best-in-class simulation approach for a TFET device with smaller wire diameter and shorter gate length. The smaller wire diameter and smaller gate length used in the reference simulation [3], according to the trend observed experimentally [1–2], should improve TFET performance. In fact, the opposite is observed: The experimental TFET device with relaxed device dimensions shows a superior performance compared with simulations.

The superior performance of the nanowire TFETs implemented by Gandhi et al. [1] is explained in this work by a special shape of the source electrode containing nickel-silicide nanorods. Such nanorod-shaped silicide structures can be formed during the silicidation process used [1–2]. There are experimental evidences of such rodlike silicide structures [4–5] formed during the nickel-silicon silicidation in processing conditions similar to the ones used in [1–2].

## II. SIMULATION APPROACH

To study the electrical performance of the nanowire tunnel FET, we simulated the electrical performance of these devices using the Sentaurus Device software [6] of Synopsys. The tunnel FET devices considered were built on round columnar silicon nanowires. In the numerical simulation, we used the cylindrical symmetry of the devices. First, we digitalized the shape of the silicon nanowire from [1] and used these data for the definition of the geometrical shape of the nanowire. Then we simulated with Sentaurus Process [6] the doping distribution of boron resulting from a tilt-free ion implantation for the formation of the drain-doped area. Finally, we emulated the doping distribution in the source region by uniform doping distributions with doping concentrations of  $1 \cdot 10^{20}$ ,  $5 \cdot 10^{20}$ , and  $1 \cdot 10^{21} \text{cm}^{-3}$ , respectively. In the simulation that is presented in Fig. 1, the silicon wire has a diameter of 18 nm in the upper part that builds the source doped area, and the lower part of the silicon column builds the drain electrode doped area in this tunnel FET. Due to the special shape of the bottom part of the nanowire, the distribution of boron in the drain region is smooth and should contribute to a smooth distribution of the electrical field

around the drain electrode with the aim to suppress the ambipolar conduction and to lower the leakage current of the transistor. The non-local tunneling model [6] based on the WKB approximation with two tunneling channels was used in the simulation of the electron transport in TFETs.

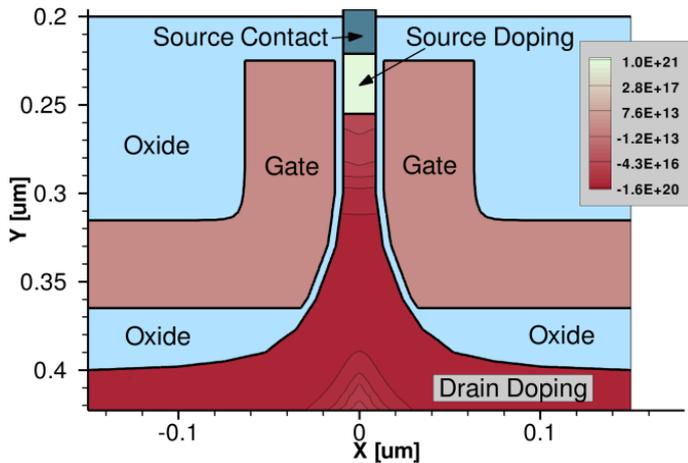


Fig. 1. Geometrical shape of the simulated columnar nanowire p-channel type tunnel FET [1] and doping distribution in silicon.

To ensure the predictive capability of the applied tunneling model, calibrated model coefficients [7] for both tunneling channels, the direct band-to-band tunneling and the phonon-assisted band-to-band tunneling, were used. The contribution of the defect related trap-assisted tunneling was neglected, since the concentration of the charge carrier traps in the devices studied was not known and this tunneling channel usually leads to a degradation of the sub-threshold performance of TFETs. Therefore its application in the simulation would screen the ultimate performance that is possible to achieve with a perfect defect free silicon material.

### III. SIMULATION RESULTS

Two variants of TFET simulations are compared in this section. First, a TFET with a source electrode that has a planar silicide-to-silicon interface and, second, a TFET with a source electrode containing a nanorod-shaped silicide pin penetrating into the active silicon area are considered. The results of the numerical simulation of the first variant of the p-channel tunnel FET are presented in Fig. 2. Three versions of the simulation are shown. Each simulation version used a different doping level in the source-doping region. It is generally expected that the higher the source doping is, the stronger is the tunneling current. This tendency is generally supported by the present simulation, but the effect on the enhancement of the on-current (at negative gate voltages and high negative drain voltage) is very small. In any case, even if the active source doping concentration reaches  $1 \cdot 10^{21} \text{cm}^{-3}$ , which is technologically a very challenging task, the simulated on-current of the TFET considered remains more than 4 orders of magnitude below the actually measured on-current. The simulated maximum on-current of  $0.082 \text{ A/m}$  for the nanowire with a  $18 \text{ nm}$  diameter, if normalized per effective geometrical channel width, is of the same order of magnitude as the result

( $0.031 \text{ A/m}$ ) obtained earlier [3] by quantum mechanical non-equilibrium Green function (NEGF) simulations for a nanowire of  $3 \text{ nm}$  diameter. The minimum of the inverse sub-threshold slope simulated for the first variant of TFET is of about  $60 \text{ mV/dec}$ . That is close to the result obtained by the quantum NEGF method [3] for a nanowire tunnel FET with  $3 \text{ nm}$  diameter but is not as low as measured on the nanowire FETs in [1].

Since the deviation of the simulation from the measurement is extremely large, and the model used [7] is known to describe well the electrical performance of TFETs in which geometry and doping were well known [8–9], we conclude that something must be different in the geometrical shape of this specific TFET to explain its high performance. To enlarge the on-state current, the tunneling generation rate or the area where a high tunneling rate is realized has to be enlarged. This can be done for example by enlargement of the source-doping-to-gate overlap, as suggested in earlier publications [10–11]. In the simulation presented in Figs. 1 and 2 this overlap was equal to  $30 \text{ nm}$ . The overlap covers already about  $1/5$  of the gate length which is equal of about  $140 \text{ nm}$ . Even if we enlarge the source-doping-to-gate overlap by a factor of three we enlarge the on-current in a best case by the same factor. Such current enlargement is far (four orders of magnitude) from what is needed to achieve the agreement with experiment. Therefore, other simulation variants should be considered.

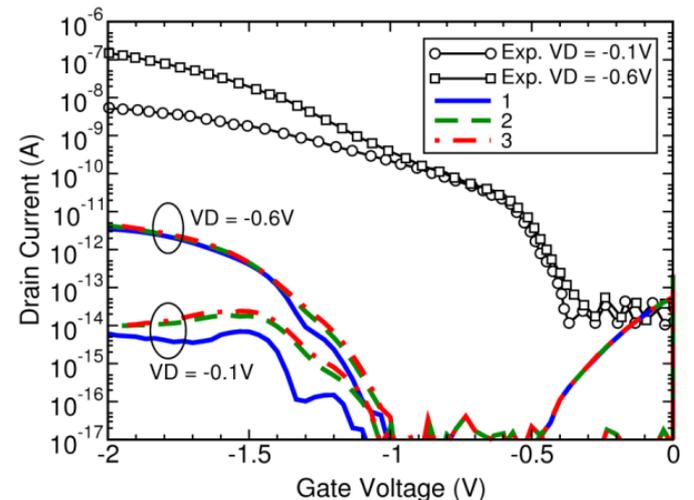


Fig. 2. Transfer characteristics of the columnar nanowire p-channel type tunnel FETs with a flat source contact simulated (1, 2, 3) and measured [1] (Exp.) for drain voltages of  $-0.1 \text{ V}$  and  $-0.6 \text{ V}$ . The simulation variants 1, 2, and 3 use an arsenic doping concentration in the source region equal to  $1 \cdot 10^{20}$ ,  $5 \cdot 10^{20}$ , and  $1 \cdot 10^{21} \text{cm}^{-3}$ , respectively.

In earlier studies [12] of the silicided source electrodes in SOI-based TFETs it was shown that a non-uniform shape of the silicide surface with a deeper penetration of the silicide in the middle of the SOI silicon layer positively impact the electrical performance of SOI based planar TFETs.

In this work, we assume that rodlike silicide structures that penetrate into the silicon channel are built during the contact silicidation process. This assumption is in agreement

with some experimental findings [4–5]. For example, in [4] silicide nanorods with a length of about 10 nm and diameter of about 1 nm were observed after thermal annealing (320°C, 20 min.) of silicon samples with previously formed platelet-shaped nickel silicide precipitates. In [5], micrometer-long nickel-silicide rodlike structures in crystalline silicon were registered after a magnetron deposition of carbon and nickel on silicon at 750°C.

In the second variant of simulation, the source electrode with a rodlike silicide pin as shown in Fig. 3 was used. It has a cylindrical symmetry and consists of two parts: The upper part is a silicide nanowire with a diameter equal to the silicon nanowire diameter and the lower part is a thin silicide nanorod with a diameter varied in these simulations from 0.2 to 6 nm.

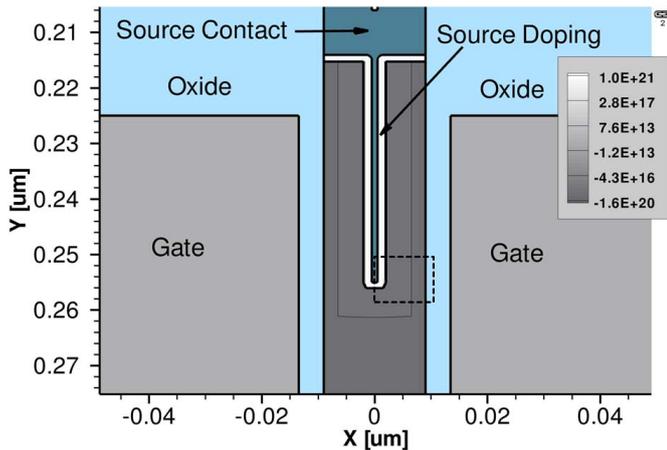


Fig. 3: Shape of the source electrode with a nano-rod silicide structure and doping in the vicinity of the source electrode in the second version of simulation of columnar TFETs. The dashed rectangle indicates position of the area discussed in Figs. 5 and 6.

The thick source-contact nanowire has a 11 nm underlap to the gate edge and the silicide nanorod part of the source-contact penetrates under the gate by 30 nm. The silicide in the source electrode is surrounded by a highly localized and heavily n-type-doped layer in silicon. The thickness of this doped layer was 1 nm and the doping level was  $1 \cdot 10^{21} \text{cm}^{-3}$ . Such a high level of doping in silicon near the silicide-to-silicon interface is known to be formed in case of arsenic doping due to the snow-plug effect in the process of silicidation. Since the effective electrical field in the surrounding of the source contact pin is expected to be dependent on the contact pin diameter, we investigated the dependence of the pTFET transfer characteristics on the diameter of the source-contact nanorod pin (Fig. 4).

To elucidate the physical reasons for the large difference in the electrical performance of the tunnel FETs with a silicide nanorod extending from the source electrode and without such a nanorod (cf. Figs. 2 and 4), we visualized the tunneling generation rates obtained in simulations for these two device variants. Fig. 5 shows the total tunneling generation rate in the tunnel FET device without the nanorod extension in the source contact. The figure shows a cut through the middle of the silicon column. The left border of the figure coincides with the

axis of the column, while the right border shows the interface between the silicon and the gate oxide at 9 nm on the x-axis.

The maximum of the tunneling generation rate in on-state for the tunnel FET with a flat source contact (drain voltage of  $-0.6 \text{ V}$ , gate voltage of  $-2 \text{ V}$ ) is located on the surface of the vertical silicon column. The maximum generation rate amounts roughly to  $2.5 \cdot 10^{26} \text{cm}^{-3} \text{s}^{-1}$ . The tunneling rate distribution extends from the maximum in direction to the middle of the silicon column. The positioning of the maximum of the tunneling generation in on-state near the silicon-to-gate-oxide interface is typical also for planar tunnel FETs. This means that if the source contact is planar, we do not use to a full extent the advantages of three-dimensionality of the columnar structure of the tunnel FETs.

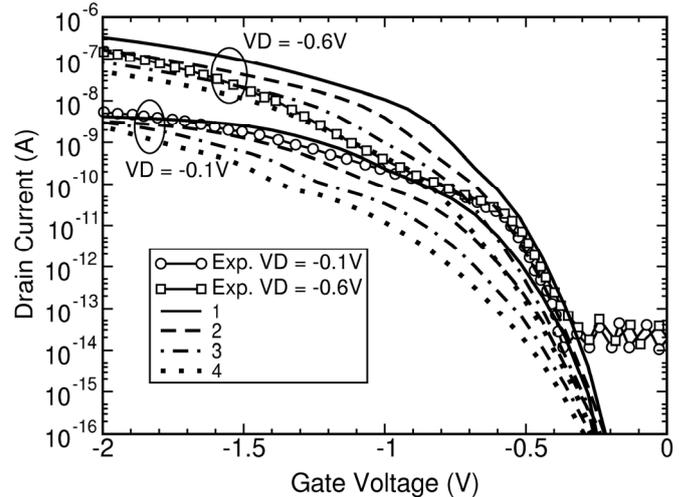


Fig. 4: Transfer characteristics of the columnar nanowire tunnel pFET simulated (1, 2, 3, 4) and measured [1] (Exp.) for drain voltages of  $-0.1 \text{ V}$  and  $-0.6 \text{ V}$ . The simulation variants 1, 2, 3, and 4 assumed 0.2 nm, 2 nm, 4 nm, and 6 nm diameter of the source contact pin, respectively.

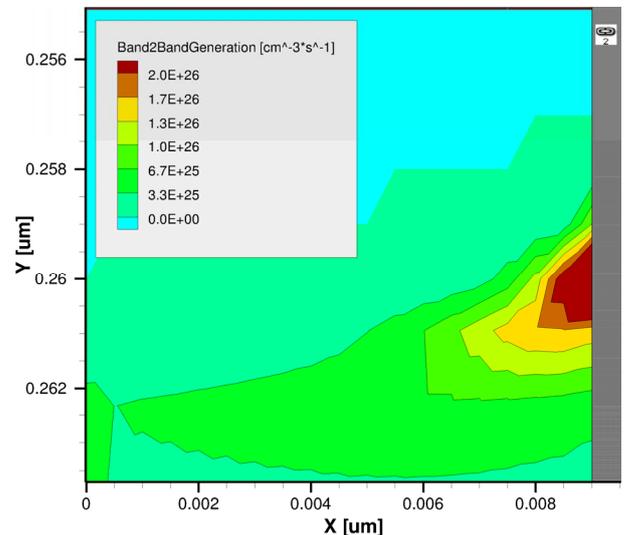


Fig. 5: Tunneling generation rate in on-state of the columnar TFET without any nanorod spike from the source electrode at a drain voltage of  $-0.6 \text{ V}$  and a gate voltage of  $-2 \text{ V}$ . The upper side of the figure coincides with metallurgical pn-junction between the source and channel.

A completely different distribution of the tunneling generation rate is observed for the columnar tunnel FET with a conducting silicide nanorod extending from the source electrode into silicon along the column axis. Fig. 6 shows the tunneling generation rate distribution for this situation. As in Fig. 5, the left-hand side of the figure coincides with the axis of the silicon column, the right-hand side is the silicon-to-gate-oxide interface. The maximum of the tunneling generation rate for this device is observed near the middle of the silicon column. The absolute value of the maximum tunneling generation rate is in excess of  $1 \cdot 10^{31} \text{ cm}^{-3} \text{ s}^{-1}$ . This tunneling generation rate is a factor of 40000 higher than in the device without the silicide nanorod in the middle of the silicon column.

As it is seen in Fig. 6, the tunneling generation distribution is concentrated around the end of the silicide nanorod that is seen in the figure as a white vertical stripe in the left side of the figure. The dark line surrounding the nanorod spike indicates the position of the metallurgical pn-junction between the source and channel doping areas. The maximum tunneling generation rate is located on the external side of pn-junction in the channel-doping region.

Since the distribution of tunneling generation rate in Fig. 6 has a limited extension not only in the radial x-direction, but also in the vertical y-direction along the column axis, the transistor on-current is expected to be not sensitive to the length of the silicide nanorod extending from the source electrode. This is because the parts of the spike that are far from the spike end do not contribute much to the integral tunneling rate that is responsible for the current in tunnel FETs.

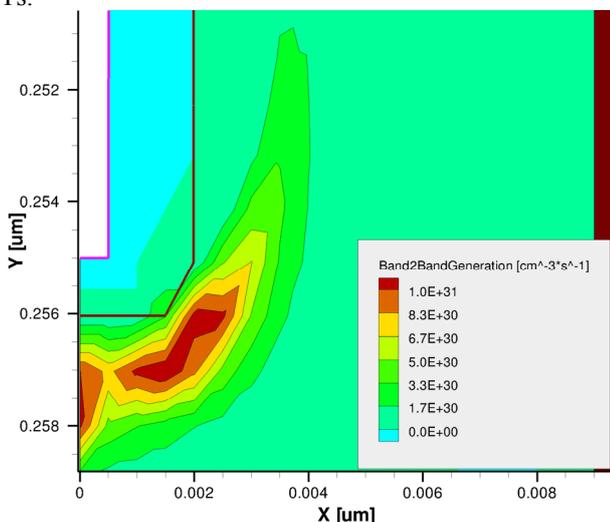


Fig. 6: Tunneling generation rate in on-state of the columnar TFET with a nanorod silicide spike in the source electrode at drain voltage of  $-0.6 \text{ V}$  and gate voltage of  $-2 \text{ V}$ .

#### IV. CONCLUSION

Columnar nanowire tunnel FETs with silicided source contacts [1–2] exhibit in measurements a record high performance both in the on-current and in the sub-threshold behavior. The high performance of the tunnel FETs with silicided source contacts experimentally observed in [1] can be

explained under the assumption that the silicide-to-silicon interface after the silicidation process is not flat, but there are silicide nanorods penetrating into the silicon wire near or in the middle of the silicon nanowire. The penetration length of the silicide nanorods under the gate was assumed to be 30 nm in the simulations of this work and the spike diameter that is needed to well reproduce the experimental performance of the considered TFETs was in the range between 0.2 nm and 2 nm. Also shorter nanorods with a penetration length of about 4 nm are expected to ensure an approximately same enhancement of the on-current in tunnel FETs as longer nanorods do.

We suggest that experimentalists should look for nanorod-shaped silicide structures near the source electrodes after the silicidation of the source contacts in silicon tunnel FETs or for possibilities to setup experimental conditions for forming source contacts with silicide nanorods penetrating into active regions of tunnel FETs.

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