AlGaN/GaN Rake-Gate HFET: A Novel Normally-Off HFET based on Stress and Layout Engineering

Hiu Yung Wong, Nelson Braga and R. V. Mickevicius
Synopsys, Inc.,
Mountain View, CA, USA
hywong@synopsys.com

***Abstract*— A novel normally-off AlGaN/GaN HFET (Rake-Gate HFET), based on stress and layout engineering without modifying typical fabrication processes is proposed. It is verified and optimized through TCAD simulation. Positive pinch off voltage is achieved by depositing compressively stressed passivation nitride surrounding gate tines, which induce significant negative piezoelectric charge under the tines. Punch through current is suppressed by including multiple tines connected as in a rake for excellent electrostatic control. It is showed that a properly designed Rake-Gate HFET has > 1000V punch-through and breakdown voltages. It also has smaller gate capacitance than regular HFETs with gates spanning similar areas. By applying the Rake-Gate HFET design to an existing normally-off HFET process (without modifying the fabrication process besides using 500nm -2GPa passivation layer), the pinch off voltage can be further increased by ~1.5V, resulting in the improvement of safe-operating margin and elimination of static energy loss in a 750V single power supply boost converter.**

Keywords*— *AlGaN/GaN HFET, Enhancement Mode, Normally-off, Stress Engineering, Layout Engineering, TCAD Simulation

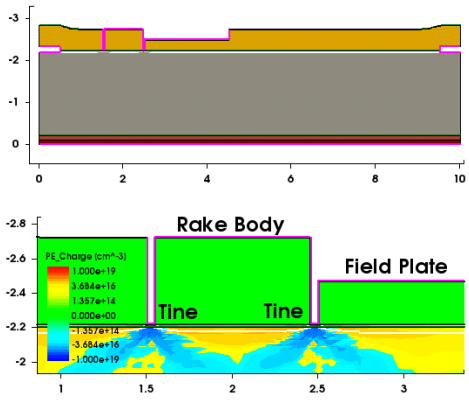

Fig. 1. Schematic showing the idea of Rake-Gate HFET (upper). Lower figure shows enlarged gate region. Pink lines represent electrodes. Design space of Rake-Gate is spanned by number of tines (N_t), tine spacing (t_S) and tine width (t_W), which can be accomplished through layout engineering alone. In this structure, N_t=2, t_S=0.9μm and t_W=50nm. Giving a total effective gate length = 1μm. The 500nm silicon nitride has -3GPa intrinsic stress. Induced negative PE Charge is found to peak under the tines. This structure has a 2μm field plate over 250nm silicon nitride.

I. Introduction

AlGaN/GaN HFETs are promising devices for power and radio frequency (RF) applications because of their excellent material characteristics, and thus better figures of merit than Silicon-based devices [1][2]. AlGaN/GaN HFETs are usually normally-on devices that conduct current when the gate is at zero bias, resulting in complex gate drive circuits for fail-safe operation [3]. However, normally-off HFETs with large enough pinch-off voltage (V_{TH}) are highly desirable in many applications such as in electric vehicles [4]. Various approaches have been proposed to form normally-off HFETs, including p-GaN gate HFET [5], fluorine plasma implantation [6], and recessed gate [7] or combination of recessed gate and AlGaN buffers [8]. However, all of them require extra processing steps and some of them have reduced process uniformity and lower carrier mobility due to implantation [6] or barrier etching in the gate region [7][8]. It has been shown via TCAD simulations that by depositing passivation nitride with intrinsic compressive stress, it is possible to shift the pinch-off voltage positively if the passivation nitride is deposited before gate opening [9][10]. However, based on the results in [10], the shift is too small to achieve a normally-off device (V_{TH}>0) for large gate lengths (e.g. 0.7μm) which is required in power devices for low punch through leakage under high drain bias. In this paper, we describe a novel normally-off device, Rake-Gate HFET, in which the gate is patterned like a rake (Fig. 1). The layout parameters, namely the number of tines, tine width and tine spacing, are controlled through layout alone. By properly engineering the layout parameters and the intrinsic stress in the passivation nitride, one can achieve normally-off devices with low punch-through currents for power applications and also substantially lower gate capacitances. Such concept can be applied to any HFETs including the aforementioned normally-off HFETs [5]-[8] to further enhance V_{TH}. We show that, without modifying the existing process, the V_{TH} of a normally-off HFET using Piezo Neutralization Technique (PNT) in [8] can be further increased by ~1.5V. This not only increases the fail-safe operation margin as required in many circuitries, but also reduces the energy consumption when used in a 750V booster converter due to smaller leakage current. This increases the design margin of normally-off HFETs such as the PNT HFET in [8] to meet the requirement of a typical commercial electric vehicle circuitry [4].

II. Device Structure and Electrical Characteristics

A Rake-Gate HFET is similar to most regular HFETs ([3]-[8]) except that the gate is patterned into an array of small gate openings, forming tines connected as a single gate as in a rake

978-1-5090-0818-6/16/$31.00 ©2016 IEEE

(Fig. 1). The design space includes layout parameter: the number of tines (N_t), tine spacing (t_S), and tine width (t_W), but involves no modification of fabrication processes. Combined with an intrinsically stressed passivation layer (silicon nitride or other appropriate materials), devices with different V_{TH} can co-exist on the same circuit without extra processing steps.

To illustrate the concept, the fabrication process of an $Al_{0.15}Ga_{0.85}N$/GaN HFET with 5nm gate oxide was simulated using TCAD software [11]. Firstly, a 2µm GaN buffer layer employing a compensation strategy [12] with $10^{18}cm^{-3}$ deep level acceptor traps was deposited, followed by epitaxial growth of a 40nm GaN channel and a 15nm $Al_{0.15}Ga_{0.85}N$ barrier. Then, after source/drain contact formation, silicon nitride with different compressive stresses and thicknesses (500nm to 2µm) was deposited. It has been shown experimentally that PECVD silicon nitride intrinsic stress can be varied by changing process conditions and compressive stress as large as -2GPa has been demonstrated [13]. We therefore chose 0, -2GPa and -3GPa as simulation splits, with -3GPa to demonstrate the potential of Rake-Gate HFET. After etching the silicon nitride using a Rake-Gate mask, 5nm gate oxide was deposited, followed by gate metal deposition. The gate metal workfunction is chosen to be 4.4eV. Because of stress relaxation in the silicon nitride after gate opening, a significant compressive stress gradient forms under the tines resulting in large negative piezoelectric (PE) charges [9][10]. Figure 1 shows the final structure of the Rake-Gate HFET. In this example, it has two tines of 50nm width separated from each other by 0.9µm. The Rake-Gate thus spans a length of 1µm. Following the same process, regular HFETs with 50nm, 100nm and 1µm in gate lengths (L_G) were also simulated for comparison.

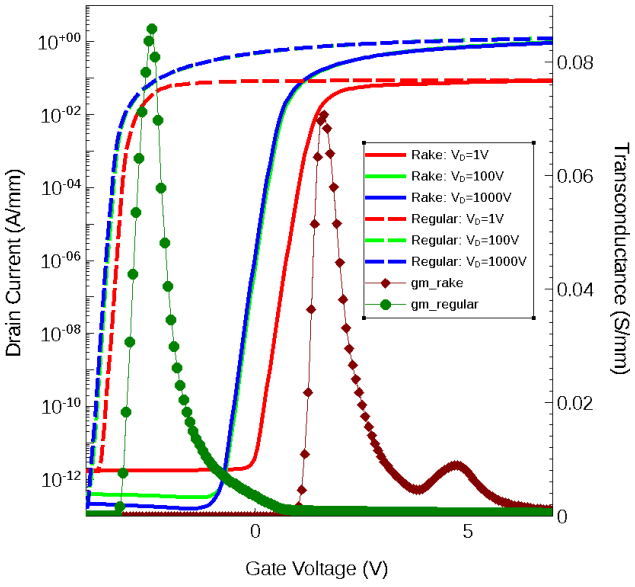

Fig. 2. I_D-V_G curves and transconductance curves (gm) of regular HFET and Rake-Gate HFET (of Fig. 1) under different drain voltages (V_D). There is more Drain-Induced-Barrier-Lowering (DIBL) in Rake-Gate compared to regular HFET. However, the V_{TH} (defined as the gate voltage at I_D=100µA/mm) still remains positive at V_D=1000V. Peak gm is reduced by about 15% in Rake-Gate but current at the same gate overdrives (V_G-V_{TH}) is similar.

The electrical performance of the Rake-Gate and a regular HFET with the same total gate length are then simulated [14] with structures including strain and stress obtained from fabrication process simulations as inputs. Essential and relevant models to III-N simulations are included as mentioned elsewhere [10][15]. Self-heating is not considered. Figure 2 shows the I_D-V_G curves and the transconductance (gm) of regular and Rake-Gate HFETs. The Rake-Gate HFET shown has a 500nm thick silicon nitride passivation with -3GPa intrinsic stress. It is found that, although the Rake-Gate HFET has worse Drain-Induced-Barrier-Lowering (DIBL), the V_{TH} (defined as the gate voltage at I_D=100µA/mm) still remains positive even at drain voltage (V_D) at 1000V. Due to the large negative PE charge inside the channel, the Rake-Gate peak transconductance is about 15% smaller than in the regular HFET. However, the ON current at the same gate voltage overdrive (V_G-V_{TH}) is similar.

Figure 3 shows the gate capacitance versus gate voltage curve at zero drain bias. The Rake-Gate exhibits substantially lower capacitance because a large portion of the gate has thick dielectric due to the additional 500nm silicon nitride passivation layer between the tines. This will reduce the energy consumption due to gate charge in a switch.

For high voltage applications, the breakdown voltage (BV) due to impact ionization and the punch through current through the buffer need to be contained. The breakdown voltage depends mostly on the gate-to-drain spacing and the field plate design. Since the Rake-Gate and the regular HFET have the same gate-to-drain spacing and field plate design, they are expected to have the same BV. Simulations indicate that both, the Rake-Gate HFET in Figure 1 and the regular HFET with L_G = 1µm, have breakdown voltages in excess of 1000 V.

On the other hand, the punch-through current through the buffer is determined by the electrostatic control of the gate. Figure 4 shows the simulated punch-through current of the Rake-Gate (of Figure 1) and regular HFETs with different values of L_G. Despite the fact that the Rake-Gate only has two 50nm tines, it has similar punch-through current as its regular gate counterpart with L_G =1µm and it is much smaller than the

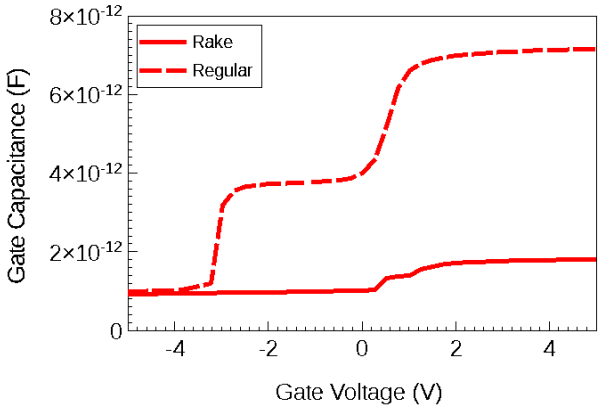

Fig. 3. CV curves (1MHz) of Rake-Gate and regular HFET (of Fig. 1) at V_D=0V. Rake-Gate shows substantially less gate capacitance.

punch-through current in regular HFETs with L_G =50nm and 100nm. Thus it is suitable for high voltage applications.

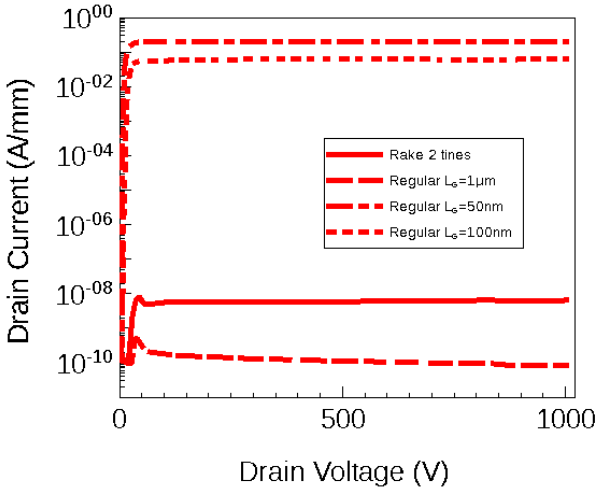

Fig. 4. Punch-through current of regular (L_G=50nm, 100nm and 1µm) and Rake-Gate HFETs at $V_G=V_{TH}$-2V. The buffer compensation trap density is reduced to $5\times10^{16}cm^{-3}$ in order to highlight the excellent gate control by the Rake-Gate.

For high voltage applications, DIBL should be minimized to avoid V_{TH} reduction at high V_D. In regular HFETs, this is usually accomplished by keeping the channel length long (curve A in Fig. 5). When L_G = 50nm, significant DIBL occurs and this is the same for the Rake-Gate HFET with 50nm tine width (curve B) when the silicon nitride thickness is 2µm. By reducing the silicon nitride thickness to 500nm, DIBL becomes comparable to that in a regular long channel HFET (curve C). On the other hand, a thicker passivation nitride stores more strain energy and thus induces more V_{TH} shift [9][10]. Therefore, there is a trade-off between V_{TH} shift and DIBL.

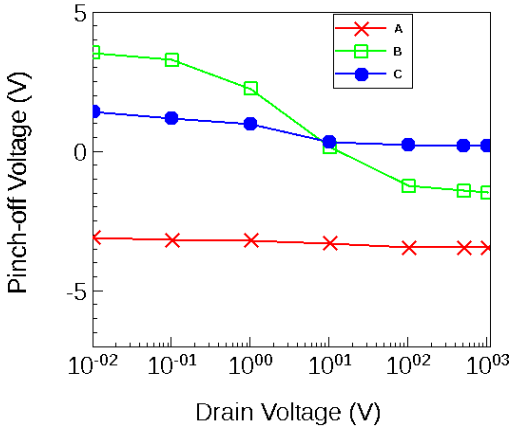

Fig. 5. V_{TH} as a function of drain bias to show the DIBL effect in Rake – Gate and regular HFET. A: regular HFET with L_G=1µm. B: Rake-Gate HFET of Fig. 1 with -2GPa 2µm silicon nitride. B: Rake-Gate HFET of Fig. 1 with -3GPa 500nm silicon nitride.

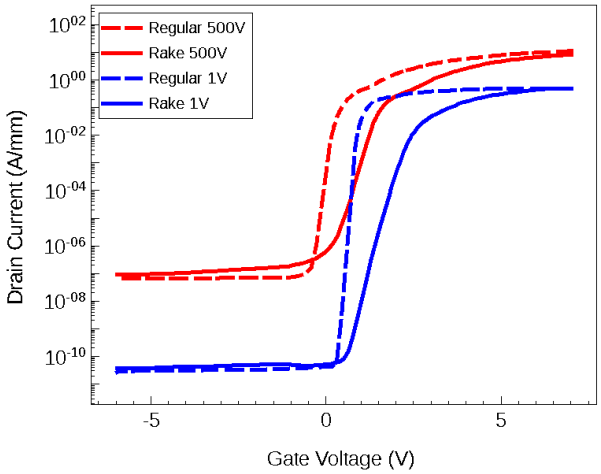

Fig. 6. I_DV_G curves of regular and Rake-Gate PNT HFETs at different drain biases.

III. Rake-Gate on PNT HFET and Booster Circuit

We then incorporate the Rake-Gate design to a PNT HFET [8] with N_t=2, t_S=0.9µm, t_W=50nm for a total L_G=1µm, and a 500 nm thick silicon nitride passivation layer intrinsically stressed with -2 GPa [13]. This is compared to a regular PNT HFET with the same L_G=1µm. The regular PNT HFET simulation was calibrated to the experimental data in [8] with similar V_{TH} and ON current and the same calibration parameters were then employed in the simulation of the Rake-Gate device. Figure 6 shows that the V_{TH} increases by about 1.5V with the Rake-Gate design. As a result, at V_G=0V and V_D=500V, the leakage is reduced by ~2-3 orders of magnitude. Figure 7 shows the punch-through current at V_G=0V. V_G=0V is used because the device will be used in a single power supply boost converter with minimum gate voltage = 0V. The Rake-Gate design has much lower punch-through current due to higher V_{TH}.

Simulations of a 750V boost converter with the schematic depicted in Figure 8 are carried out employing the Rake-Gate

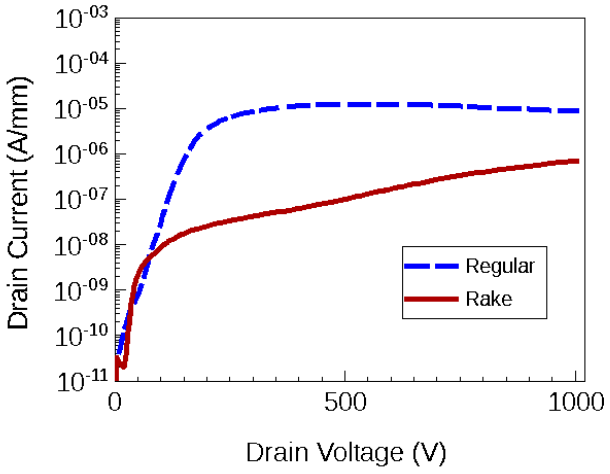

Fig. 7. Drain Leakage current of regular and Rake-Gate PNT HFETs at V_G=0V.

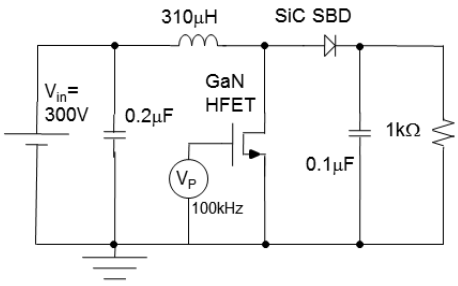

Fig. 8. Booster circuit used in TCAD Mixed-Mode simulation. V_P is 8V and 9.6V for regular and Rake-Gate design respectively due to different V_{TH}'s.

and regular HFETs of the previous section as the switching elements. As an example, a 0.5 duty cycle switching at 100kHz is chosen and a silicon carbide Schottky Barrier Diode (SBD) is used to minimize the diode recovery loss. Inductance and capacitance values are chosen so that the boost converter reaches steady state within 15 cycles while the output ripple is still reasonable.

Figure 9 shows the output voltage waveform and the current through the switch obtained in TCAD Mixed-Mode simulation, in which the electron and hole continuity equations and Poisson equation are solved self-consistently for SiC SBD and GaN PNT HFET together with SPICE circuit elements. Note that the regular PNT HFET has the V_{TH} and ON current calibrated to experimental data in [8]. The regular PNT HFET is too leaky when it is switched off due to V_{TH} being not positive enough. As a result, it has a large static energy loss, which accounts for 35% of the total energy loss. In the Rake-Gate design, with 1.5V higher V_{TH}, the leakage is much lower when the transistor is in OFF state and completely eliminates the static energy loss while the switching energy remains the same.

Therefore, the Rake-Gate design extends the design space by providing an extra knob to transistor optimization. For example, one may also reduce the mole fraction in the buffer of

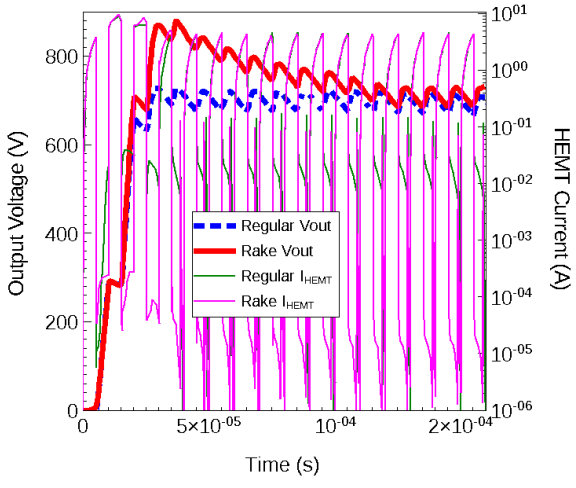

Fig. 9. Output voltage waveforms of regular and Rake-Gate PNT HFET and the current through the HFETs in the boost converter (of Fig. 8). Rake-Gate PNT HFETs has substantially lower leakage current resulting in ~35% reduction in energy loss due to elimination of static energy.

a PNT HFET with Rake-Gate to attain the same V_{TH}. As a result, the 2DEG will be increased and thus the R_{ON} of the transistor can be reduced.

Conclusion

Normally-off AlGaN/GaN Rake-Gate HFET is proposed and verified with TCAD simulations. It has much lower gate capacitance and similar electrical characteristics as regular HFETs. It requires no modification to the existing AlGaN/GaN HFET fabrication processes besides compressively stressed passivation nitride is needed. The V_{TH} can be tuned by merely layout engineering allowing multiple V_{TH} realizations in the same circuit without extra cost. It can be combined with other normally-off devices to further increase the V_{TH} to enhance the safe-operating margin and design margin. By using silicon nitride with experimentally demonstrated intrinsic stresses, a 750V, single power supply boost converter with a Rake-Gate HFET with improved design margin is demonstrated.

References

[1] A. Huang, "New unipolar switching power device figures of merit," IEEE Electron Device Letters, vol. 25, pp. 298-301, May 2004.

[2] A. Lidow, J. Strydom, M. de Rooij, D. Reusch, *GaN Transistors for Efficient Power Conversion*, 2nd Edition, 2014.

[3] R. Wang, Y. Cai, C.-W. Tang, K. M. Lau, and K. J. Chen, "Enhancement-mode Si3N4/AlGaN/GaN MISHFETs," IEEE Electron Device Lett., vol. 27, no. 10, pp. 793-795, Oct. 2006.

[4] T. Kachi, D. Kikuta and T. Uesugi, "GaN power device and reliability for automotive applications," Reliability Physics Symposium (IRPS), 2012 IEEE International, Anaheim, CA, 2012, pp. 3D.1.1-3D.1.4.

[5] X. Hu, G. Simin, J. Yang, M. A. Khan, R. Gaska, and M. S. Shur,"Enhancement mode AlGaN/GaN HFET with selectively grown pn junction gate," Electron. Lett., vol. 36, no. 8, pp. 753-754, Apr. 2000.

[6] Y. Cai, Y. G. Zhou, K. J. Chen, and K. M. Lau, "High-performance enhancement-mode AlGaN/GaN HEMTs using fluoride-based plasma treatment," IEEE Electron Device Lett., vol. 26, no. 7, pp. 435–437, Jul. 2005.

[7] V. Kumar, A. Kuliev, T. Tanaka, Y. Otoki, and I. Adesida, "High transconductance enhancement-mode AlGaN/GaN HEMTs on SiC substrate," Electron. Lett., vol. 39, no. 24, pp. 1758-1760, Nov. 2003.

[8] K. Ota, K. Endo, Y. Okamoto, Y. Ando, H. Miyamoto and H. Shimawaki, "Normally-off GaN FET with high threshold voltage uniformity using A novel piezo neutralization technique," in IEDM Technical Digest, Baltimore, MD, USA, pp. 153-156, December 2009.

[9] N. Shigekawa and S. Sugitani, "Analysis of passivation-film-induced stress effects on electrical properties in AlGaN/GaN HEMTs," IEICE Trans. Electron., Aug. 2010.

[10] H. Y. Wong, N. Braga, R. V. Mickevicius and J. Liu, "Study of the effects of barrier and passivation nitride stresses on AlGaN/GaN HEMT performance using TCAD simulation," in the 3rd IEEE WiPDA, Blacksburg, VA, 2015, T2-8025.

[11] Synopsys Inc., CA, USA, Sentaurus™ Process User Guide (2016).

[12] D. Bisi et al., "Effects of buffer compensation strategies on the electrical performance and RF reliability of AlGaN/GaN HEMTs," Microelectronics Reliability, 55, 1662–1666, 2015.

[13] M. P. Besland, M. Lapeyrade, F. Delmotte and G. Hollinger, "Interpretation of stress variation in silicon nitride films deposited by electron cyclotron resonance plasma", Journal of Vacuum Science & Technology A, 22, 1962-1970 (2004).

[14] Synopsys Inc., CA, USA, Sentaurus™ Device User Guide (2016).

[15] S. Strauss, A. Erlebach, T. Cilento, D. Marcon, S. Stoffels and B. Bakeroot, "TCAD methodology for simulation of GaN-HEMT power devices," Power Semiconductor Devices & IC's (ISPSD), 2014 IEEE 26th International Symposium on, Waikoloa, HI, 2014, pp. 257-260.