Drift-Diffusion Quantum Corrections for $In_{0.53}Ga_{0.47}As$ Double Gate Ultra-Thin-Body FETs

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***Abstract*—With the growing interest in III-V-based nano-scale transistors as potential candidates for next-generation switches there is a need for efficient simulation tools capable to predict the impact of inherent quantum effects. In this paper we show how quantum drift-diffusion (QDD) models can be used to mimic those quantum effects. The models do not only properly account for geometrical confinement in $In_{0.53}Ga_{0.47}As$ FETs with a body thickness below 12 nm, but also for source-to-drain tunneling, the main cause of rising OFF-current at gate lengths shorter than 25 nm. The parameters of the QDD models available in the commercial device simulator S-Device were calibrated with the help of the quantum transport code QT-Solver. Transfer characteristics of double-gate transistors with various gate lengths were computed. Their sub-threshold swings were extracted and used as metric for the comparison. Various QDD models, also in combination with a barrier tunneling model, were tested. The pre-factor of the density-gradient model in S-Device turned out to depend on normal electric field and body thickness. Expressions for both dependencies were implemented in the Physical Model Interface of S-Device. Good agreement for inversion layer density and sub-threshold slope obtained with the QDD models and those computed with QT-Solver was found for low and high source-drain bias.**

I. Introduction

As devices are scaled down into the nanometer range, quantum effects start to play a major role and strongly impact their performance. For instance, geometrical quantum confinement in the body of $In_{0.53}Ga_{0.47}As$ FETs with a body thickness below 12 nm leads to a shift of the threshold voltage and to a change of gate capacitance and, hence, significantly alters the transfer characteristics of the device [1]. Moreover, the thin potential barrier between source and drain in transistors with gate lengths shorter than 25 nm causes a strong leakage current known as source-to-drain tunneling (SDT) which deteriorates the sub-threshold swing (SS) [2].

Quantum transport (QT) simulators are still not mature for industrial environments and are computationally too expensive for larger and more complex 2D and 3D devices. Furthermore, not all features available in commercial TCAD packages are ready for use in QT simulators, e.g. band-to-band tunneling and certain scattering models (impurity, surface roughness, etc.). Calibration capabilities are also limited in QT solvers.

The aim of this work is, therefore, to study how so-called quantum drift-diffusion (QDD) tools, e.g. S-Device from Synopsys [3], can be used to mimic the described quantum effects by careful calibration of the implemented quantum correction models. This is demonstrated for technologically relevant $In_{0.53}Ga_{0.47}As$ double-gate ultra-thin-body (UTB) FETs.

II. Method

For the simulation of geometrical confinement perpendicular to the transport direction we used the Density Gradient (DG) model which adds a quantum potential Λ to the classical potential in the computation of the density [4]. This quantum potential depends on the carrier density n, the effective mass m_e, and a fitting parameter γ introduced in the model of Ref. [5].

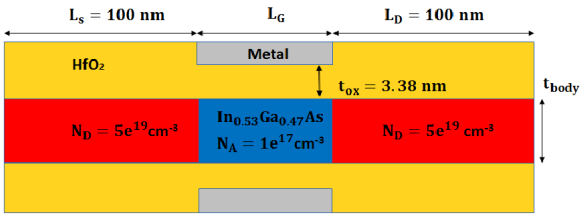

Fig. 1. Schematic of an $In_{0.53}Ga_{0.47}As$ double-gate UTB FET.

First, we simulated the 1D electron density profile along a vertical cut in the middle of the double-gate FET (see Fig. 1) and used the Schrödinger-Poisson solver S-Band [6] as reference tool. Fig. 2(a) shows a comparison of the density profiles for a body thickness of 6 nm after calibration of γ. The corresponding QV-curves (inversion charge versus gate voltage) are presented in Fig. 2(b). The same simulations and fittings were done for a number of body thicknesses ranging from 4 nm to 10 nm in the gate voltage interval $V_G = [0, 1]$ V. The used effective masses m_e and non-parabolicity parameters α depend on the channel thickness and were taken from Ref. [7].

We observed that the combination of geometrical and channel confinement makes γ a strong function of the normal electric field. Its value at the semiconductor-oxide interface was chosen as parameter to fit γ over the entire V_G-range.

Based on the QV-data we derived the following form for the dependence on normal electric field at the interface (E_{norm}):

$$\gamma_{pmi}(E_{norm}) = (1/c) + a \cdot tan(b\, E_{norm}) \qquad (1)$$

with E_{norm} measured in V/cm. This function is continuous and smooth over the entire V_G-range which assures convergence when implemented in the Physical Model Interface (PMI) of

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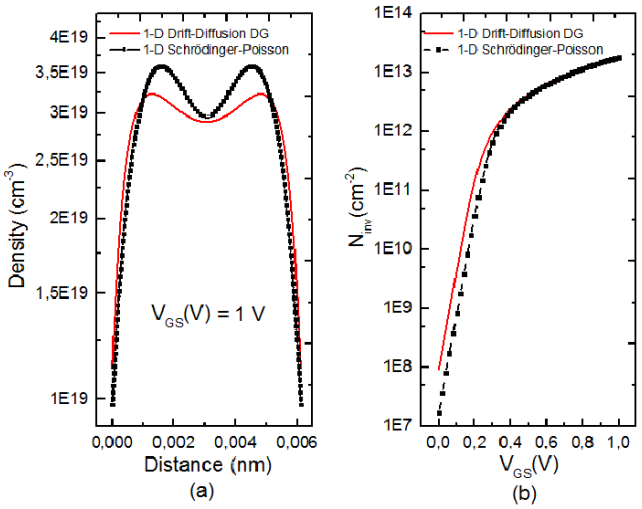

Fig. 2. (a) Comparison of the electron density and (b) inversion charge vs. gate voltage computed with the isotropic DG model (red curves) and the Schrödinger-Poisson solution from S-Band (black dashed curves). In (b) $\gamma = 0.6$ which gives the best fit for $V_{\rm GS} = 1$ V.

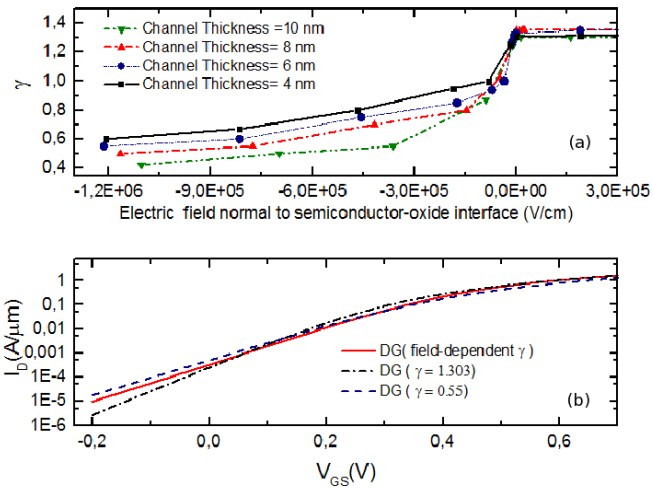

Fig. 3. (a) DG fitting parameter γ as function of normal electric field at the interface for different body thicknesses. (b) Comparison of the $I_{\rm D}V_{\rm GS}$ characteristics ($V_{\rm DS}$ = 0.05 V) of an $In_{0.53}Ga_{0.47}As$ double-gate UTB FET ($t_{\rm body}$ = 4 nm, $L_{\rm G}$ =10 nm) computed for γ = 0.55, γ = 1.303, and using a field-dependent γ (PMI model).

S-Device. The fitting parameters a, b, and c depend on the body thickness $t_{\rm body}$ and are modeled as quadratics, e.g.

$$a = a_1\, t_{\rm body}^2 + a_2\, t_{\rm body} + a_3\,, \qquad (2)$$

where $t_{\rm body}$ is measured in nm. The coefficients are $a_1 = -0.0053$, $a_2 = 0.07824$, $a_3 = 0.07824$, $b_1 = -6.566 \times 10^{-7}$, $b_2 = 8.78 \times 10^{-6}$, $b_3 = -2.007 \times 10^{-5}$, $c_1 = -0.006163$, $c_2 = 0.1065$, $c_3 = 0.5677$. For the simulation results presented in this work we used $t_{\rm body}$ = 7 nm, a = 0.499, b = 9.216×10^{-6} and c = 1.011.

To enable simulation of SDT in S-Device, the quantum transport code QT-Solver [8] was used as calibration tool. Transfer characteristics for gate lengths ranging from 10 nm to 25 nm were computed and the SS values were extracted for comparison. We extracted two sets of transfer characteristics, one for $V_{\rm DS}$ = 0.05 V and one for $V_{\rm DS}$ = 0.63 V.

We applied three S-Device models to simulate SDT: (i) the anisotropic DG model having an attenuation matrix with diagonal elements $\alpha_{\rm l}$, $\alpha_{\rm v}$ which scale Λ in longitudinal and vertical direction, respectively. We found an optimal $\alpha_{\rm l}$-value *for each gate length* that can reproduce the SS obtained from QT-Solver. The element $\alpha_{\rm v}$ serves to reproduce the effect of geometrical confinement perpendicular to the transport direction.

The other two models are (ii) the Modified Local Density Approximation (MLDA) [9] and (iii) the Nonlocal Tunneling (NLT) model [3]. To simulate SDT, the latter can be applied in combination with either MLDA or (anisotropic) DG. In this combination, geometrical confinement in the ultra-thin body is enforced by the MLDA or (anisotropic) DG model. The tunneling mass $m_{\rm c}$ of the NLT model could of course also be used to better match SS and drain-induced barrier lowering (DIBL). Calibration is in most cases necessary because the NLT model relies on a 1D WKB approach, which is not appropriate as the potential landscape in the DG UTB FET varies sharply in 2D.

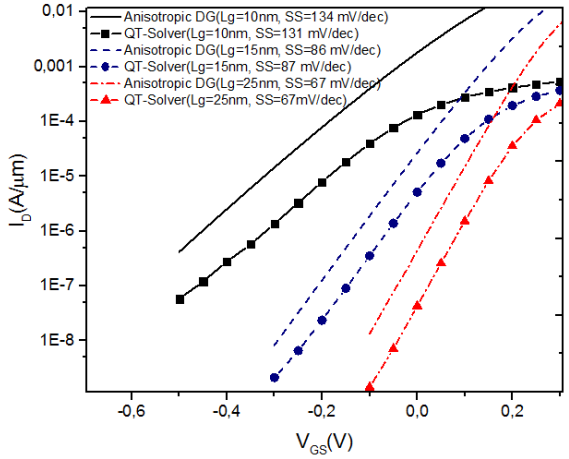

Fig. 4. $I_{\rm D}V_{\rm GS}$-characteristics from the anisotropic DG model for a 7 nm UTB FET with different gate lengths ($V_{\rm DS}$ = 0.05 V). Parameters: $\gamma = 0.6$, $\alpha_{\rm v}$ = 1, $\alpha_{\rm l}$ = 0.7 ($L_{\rm G}$ = 10 nm) , $\alpha_{\rm l}$ = 0.4 ($L_{\rm G}$ = 15 nm and $L_{\rm G}$ = 25 nm).

III. Results

Fig. 3(a) shows the field-dependence of γ for various body thicknesses. Fig. 3(b) demonstrates how the $I_{\rm D}V_{\rm GS}$-curve in the case $t_{\rm body}$ = 4 nm, $L_{\rm G}$ =10 nm changes using the extreme values of γ from Fig. 3(a) and the field-dependent γ, respectively.

The small difference in the threshold voltage between QT-Solver and S-Device ($\approx$ 60 mV) is due to different energy zeros and was not removed in Figs. 4 - 9 for better visibility.

The first model we used to simulate SDT was the anisotropic

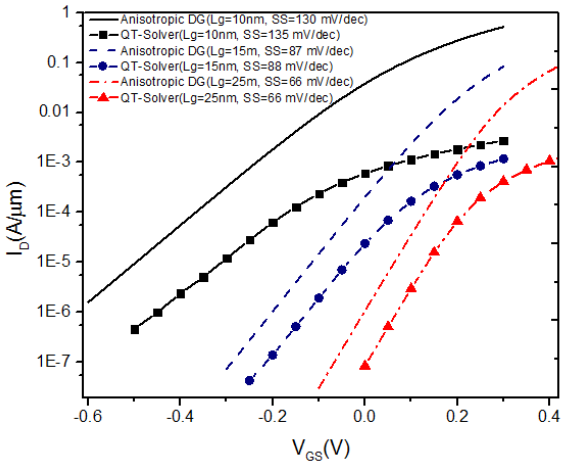

Fig. 5. $I_{\mathrm{D}}V_{\mathrm{GS}}$-characteristics from the anisotropic DG model for a 7 nm UTB FET with different gate lengths (V_{DS} = 0.63 V). Parameters: $\gamma = 0.6$, α_{v} = 1, α_{l} = 1 (L_{G} = 10 nm) , α_{l} = 0.75 (L_{G} =15 nm), α_{l} = 0.2 (L_{G} = 25 nm).

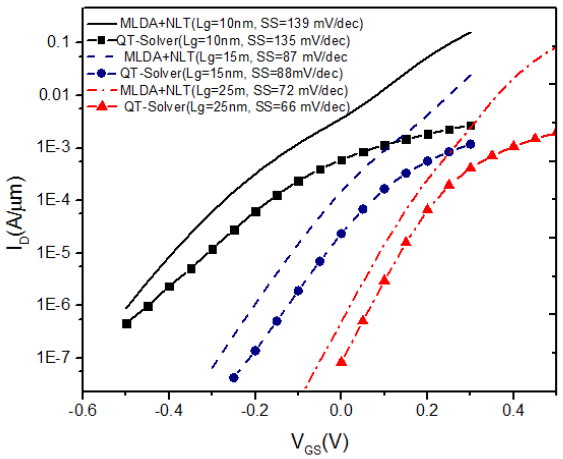

Fig. 7. $I_{\mathrm{D}}V_{\mathrm{GS}}$-characteristics obtained from the combination MLDA + NLT for a 7 nm UTB FET with different gate lengths. V_{DS} = 0.63 V, $m_{\mathrm{c}} = 0.0516\, m_0$.

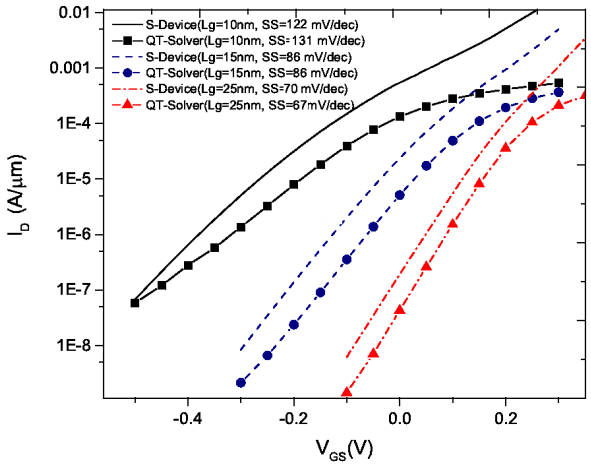

Fig. 6. $I_{\mathrm{D}}V_{\mathrm{GS}}$-characteristics obtained from the combination MLDA + NLT for a 7 nm UTB FET with different gate lengths. V_{DS} = 0.05 V, $m_{\mathrm{c}} = 0.0516\, m_0$.

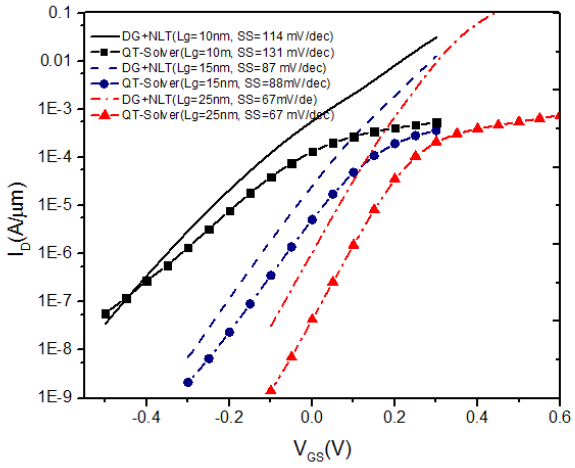

Fig. 8. $I_{\mathrm{D}}V_{\mathrm{GS}}$-characteristics obtained from the combination of DG (with field-dependent γ) + NLT for a 7 nm UTB FET with different gate lengths. V_{DS} = 0.05 V, $m_{\mathrm{c}} = 0.0516\, m_0$.

DG model. Fig. 4 presents the fitted $I_{\mathrm{D}}V_{\mathrm{GS}}$-curves for three gate lengths computed with this model for V_{DS} = 0.05 V and Fig. 5 presents the fitted $I_{\mathrm{D}}V_{\mathrm{GS}}$-curves for V_{DS} = 0.63 V. It is important to note that these curves were obtained with $\alpha_{\mathrm{v}} = 1$. This means that the quantum potential Λ was not further modified in vertical direction, i.e. we are able to accurately reproduce the confinement-induced shift of the threshold voltage. However, at the high $V_{\mathrm{DS}} = 0.63\,V$ the anisotropic DG model requires a larger α_{l} to reproduce SDT for all gate lengths.

The fitted transfer characteristics for different gate lengths computed with the combination MLDA + NLT ($m_{\mathrm{c}} = 0.0516\, m_0$) are presented in Fig. 6 for V_{DS} = 0.05 V and in Fig. 7 for V_{DS} = 0.63 V. At high source-drain voltage (V_{DS} = 0.63 V), MLDA+NLT can reproduce the leakage current due to SDT better than at low V_{DS}, in particular for the shortest gate length.

Finally, the fitted curves obtained by the combination of DG (with field-dependent γ) + NLT are presented in Fig. 8 for V_{DS} = 0.05 V and in Fig. 9 for V_{DS} = 0.63 V. For this combination, the fitted SDT currents at low and high V_{DS} are of comparable quality. Note that α_{l} = 0 by default when NLT is used [3].

Table I summarizes the results of the three models for V_{DS} = 0.05 V and Table II for V_{DS} = 0.63 V. With the parameters presented in both tables, the slope of the transistor with the shortest gate is best reproduced by the anisotropic DG model

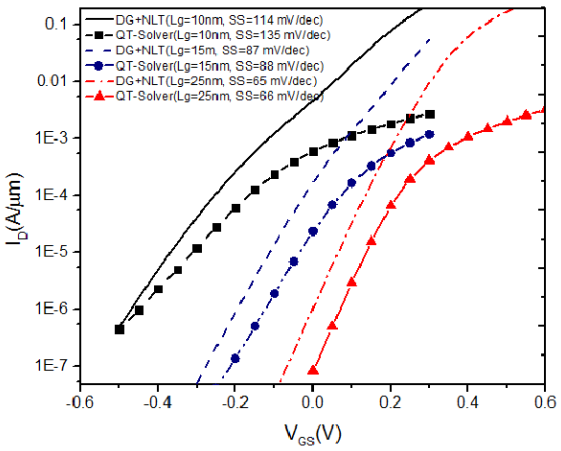

Fig. 9. $I_{\mathrm{D}}V_{\mathrm{GS}}$-characteristics obtained from the combination of DG (with field-dependent γ) + NLT for a 7 nm UTB FET with different gate lengths. V_{DS} = 0.63 V, $m_{\mathrm{c}} = 0.0516\,m_0$.

TABLE I
SUMMARY OF THE CALIBRATION PARAMETERS USED FOR EACH MODEL AT V_{DS} = 0.05 V.

Methods / L_{G}	Anisotropic DG	MLDA + NLT	DG + NLT
10 nm	α_{l} = 0.7 α_{v} = 1 γ = 0.6	$m_{\mathrm{c}} = 0.0516\,m_0$	$m_{\mathrm{c}} = 0.0516\,m_0$ $\gamma = \gamma_{\mathrm{user}}{}^{*}\cdot\gamma_{\mathrm{pmi}}$
15 nm	α_{l} = 0.4 α_{v} = 1 γ = 0.6	$m_{\mathrm{c}} = 0.0516\,m_0$	$m_{\mathrm{c}} = 0.0516\,m_0$ $\gamma = \gamma_{\mathrm{user}}{}^{*}\cdot\gamma_{\mathrm{pmi}}$
25 nm	α_{l} = 0.4 α_{v} = 1 γ = 0.6	$m_{\mathrm{c}} = 0.0516\,m_0$	$m_{\mathrm{c}} = 0.0516\,m_0$ $\gamma = \gamma_{\mathrm{user}}{}^{*}\cdot\gamma_{\mathrm{pmi}}$

* γ_{user} = 1, γ_{pmi} is evaluated according to Eq.1.

TABLE II
SUMMARY OF THE CALIBRATION PARAMETERS USED FOR EACH MODEL AT V_{DS} = 0.63 V.

Methods / L_{G}	Anisotropic DG	MLDA + NLT	DG + NLT
10 nm	α_{l} = 1 α_{v} = 1 γ = 0.6	$m_{\mathrm{c}} = 0.0516\,m_0$	$m_{\mathrm{c}} = 0.0516\,m_0$ $\gamma = \gamma_{\mathrm{user}}{}^{*}\cdot\gamma_{\mathrm{pmi}}$
15 nm	α_{l} = 0.75 α_{v} = 1 γ = 0.6	$m_{\mathrm{c}} = 0.0516\,m_0$	$m_{\mathrm{c}} = 0.0516\,m_0$ $\gamma = \gamma_{\mathrm{user}}{}^{*}\cdot\gamma_{\mathrm{pmi}}$
25 nm	α_{l} = 0.2 α_{v} = 1 γ = 0.6	$m_{\mathrm{c}} = 0.0516\,m_0$	$m_{\mathrm{c}} = 0.0516\,m_0$ $\gamma = \gamma_{\mathrm{user}}{}^{*}\cdot\gamma_{\mathrm{pmi}}$

* γ_{user} = 1, γ_{pmi} is evaluated according to Eq.1.

in the case of low V_{DS} = 0.05 V. In the case of a high V_{DS} = 0.63 V the anisotropic DG model and the combination MLDA+NLT yield comparable results. When using MLDA + NLT, an improvement could be achieved by increasing the tunneling mass for the longer gates, which was however discarded here for clarity.

For all the "ballistic" simulations with S-Device, a constant channel mobility of 2.26×10^4 cm^2/Vs was used which leads to arbitrary ON-currents. Note that in the drift-diffusion transport model the current diverges for $L_{\mathrm{G}} \to 0$. The inclusion of a ballisticity correction in the total mobility would reduce the ON-current by orders of magnitude. As the ON-current was not a subject of this paper, no attempt was made to fit it to the values obtained with QT-Solver. However, future work is necessary to understand the impact of the above-discussed quantum correction models on the ON-current, to identify possible artifacts, and to extend the criteria for the most suited variant.

IV. Conclusion

The anisotropic DG model with constant γ can fairly reproduce the SS of $In_{0.53}Ga_{0.47}As$ UTB FETs even in case of strong SDT, but has the disadvantage that the parameter α_{l} has to be fitted for each gate length. The NLT model, when used together with DG and field-dependent γ, needs less calibration of the tunneling mass m_{c} than in combination with MLDA to match the SS reference values. A drawback of this combination, is that MLDA does not allow wave penetration into the oxide [9]. As viable choice one can recommend the combination of NLT and DG with field-dependent γ, as just the same tunneling mass m_{c} (with physically correct value) can be used for all gate lengths and no further α-fitting is necessary.

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