Device Level Modeling Challenges for Circuit Design Methodology in Presence of Variability

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***Abstract*— CMOS technology scaling to decananometer range has raised the challenge to mitigate the impact of multi-scale process variations ranging from cm to atom-scale and acting as circuit yield detractors. Moreover, circuit applications in Ultra Low Power (ULP) range lead to MOSFET device operation in near threshold regime where it is well established that variability impact on DC/AC electrical characteristics dramatically increases. Variability mitigation techniques are part of process development. In addition, accurate circuit design methodologies are required to determine circuit performance margins versus specifications, and to develop circuit level variability mitigation/compensation techniques, to enable high yield and manufacturable products in presence of variability. In this context, we update device modeling requirements for circuit design, revisit device electrical characterization and compact modeling methodologies needed to support accurate circuit simulation throughout the design space. We focus on spatial variability components at local scale, including systematic layout effects and statistical variability. This approach is illustrated on UTBB FDSOI devices. Device modeling challenge for accurate circuit simulation in presence of variability is better identified.**

Keywords*— *Process Variability (PV); Local Layout Effects (LLE); Statistical Variability (SV); Variability Test Structures; Statistical Compact Modeling

I. INTRODUCTION

During past decades, CMOS technology scaling was conducted to increase integration density, improve performance and reduce power consumption; it has also required considerable development effort to mitigate the impact of process variations on circuit applications. Variability sources are classified with respect to their respective impact at circuit level [1]; both spatial and temporal variations are considered. Spatial variations alone are multi-scale, from cm to atom dimension. From circuit perspective, variations include interdie, intradie, and device to device variations. Interdie and intradie variations are of systematic nature and grouped under the label of *Global* Process Variability (PV); device to device variations combine systematic pattern-dependent proximity effects (pattern rounding, mechanical strain, ion implant unifromity,..) grouped under the label of *Local* Layout Effects (LLE), and Statistical Variability (SV) inherent to granularity of matter (fluctuations of doping, line-edge roughness, metal grain granularity…). Interdie variations include multiple contributions in which different manufacturing processes are involved that each require specific mitigation technique from technology developers. In particular, for critical dimension control [2], interdie components considered include lot to lot, wafer to wafer, intra-wafer die to die, and potentially intrafield variations (assuming multiple dies per field), in which multiple steps are involved, from mask making to lithography/etch processes. Intradie includes non-uniformities in patterning related to pattern shape, proximity and density effects, as well as those from the rapid thermal annealing (RTA) process related to non-uniform pattern density [3], without excluding other effects like Chemical Mechanical Polish (CMP) and etch micro-loading.

Mitigating variability is a multi-level approach in which dedicated solutions at process, device, and circuit level must be found. Over years, innovative materials, processes, device architectures, modeling and circuit design methodologies have been introduced so that high yield manufacturability of products can still be reached. Industry has benefited from visionary pioneer work to anticipate on limitation of CMOS scaling [4]. While new technology nodes are developed from the 65nm down to the 32nm one and below [1-6], continuous assessment of variability impact, and development of mitigation techniques at process and design level are conducted. On technology side, challenges to meet patterning process critical requirements for advanced logic nodes are well identified and addressed in their complexity [2]. Advanced Optical Proximity Correction (OPC) is to be mentioned here not only as a method to mitigate distortion of pattern shapes printed on silicon, but also as a significant contributor to help for accurate compact modeling of electrical device characteristics. At device level, adoption of architectures where electrostatic robustness against short-channel effects is improved (such as multi-gate transistor or the FDSOI technology) is also valuable for reducing impact of Variability. At circuit level, examples of variability mitigation techniques are layout regularity for better manufacturing [8-9], and power supply or back-biasing compensation techniques [10-15]. One important design requirement is that all variability effects which are not properly compensated by process mitigation techniques need to be accurately characterized in terms of deviations of electrical characteristics and accurately modeled

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in efficient variability-aware design tools. Circuit design objective are primarily twofold (i) to assess efficiency of design compensation techniques and (ii) to guarantee good agreement between circuit performance elaborated during the design phase (after post-layout circuit simulation), and circuit testing results (after Silicon processing).

In this context, the scope of this paper is to review design needs, update electrical characterization and compact modeling requirements for simulation of variability at circuit level, and to identify challenges. The paper is organized as follows. Section II discusses modeling requirements for circuit design down to the 28nm node, and considering Ultra-Low Power circuits. Section III describes the conditions for accurate nominal model in presence of variability. Section V revisits device characterization and modeling methodology for Local Layout Effects (LLE) acting as a source of local systematic variations. Section VI describes similar methodology for Statistical Variability (SV). Section VII summarizes the challenges.

II. Circuit Design

From circuit design perspective, variations can be mitigated by adapting layout and design. Improved layout reduces the risk of getting functional devices with electrical characteristics out of the expected range (e.g. with excessive leakage or poor performance) within allowed design space defined by a large range of transistor dimensions (fig.1), operating voltages and chip temperature; first, this requires preserving integrity of pattern stack for each device with respect to any combination of pattern shape and its environment allowed by Design Rules. This risk has been gradually mitigated from 90nm to 45nm nodes by adopting Design-for-Manufacturing techniques (DFM) [6-7] that adapt device layout to process and manufacturing constraints for better yield. DFM rules are technology node dependent, and are essentially driven by uniformity in lithography, e.g. by adopting unidirectional gates for SRAMs, and somehow in mechanical strain booster techniques, e.g. by applying same distance between active regions of adjacent devices. Another mitigation technique is layout regularity. At transistor level, it improves uniformity in pattern shape, mitigates impact of residual (after OPC) Gate and Active rounding effects. At circuit block level, uniformity of pattern density is reached by inserting regular dummy patterns in low density areas; layout regularity has demonstrated added-value, at the expense of some area loss, starting 40nm technology [8-9].

Beyond layout, next step of improvement is to mitigate variability by design. In the past decade, different techniques were adopted to reduce variability induced yield losses in performance and power. In Bulk CMOS technologies, examples from literature include interdie mitigation through adaptive body bias (ABB) at the expense of area overhead, adaptive supply voltage (ASV) at some expense of reliability [10], and fine-grained intradie mitigation with ABB [11]. On chip monitors and localized ABB were used for full compensation of interdie and intradie variations in 65nm node [12]. ABB was also proven effective for compensation of NBTI degradation [13]. Last, ABB technique was expanded to 28nm UTBB FDSOI technology [14], which offers a powerful knob for ABB thanks to wide-range back-gate control [15].

Recently, Design Technology Co-Optimization (DTCO) was introduced for Standard Cells design with sub-20nm devices [16]. DTCO approach extends the optimization target from manufacturability of single pattern or pattern stack in their environment to circuit cell figures (area, parasitic...), and potentially includes block level routability constraints. Recently, for SRAM design, DTCO has been further extended to account for interplay between spatial process and statistical variations [17], and to time dependent degradation [18].

Design requirements for accurate device modeling account for a broad range of application needs ranging from Logic (Standard Cells,) and IOs, to Analog-Mixed signal (Data converters,..) and Analog-RF (Amplifiers,..). Design space offers a wide range of possible transistor dimensions (Fig.1), temperature, and operating voltages.

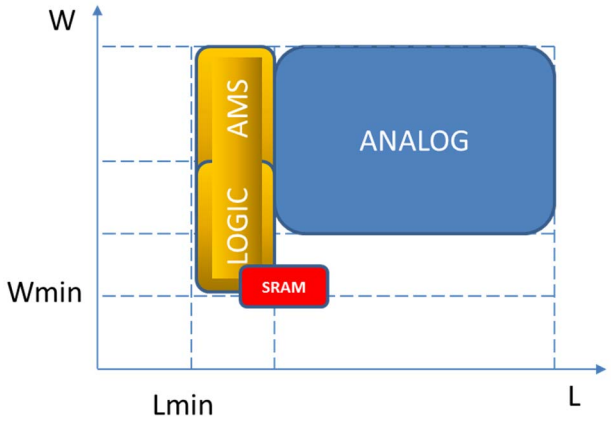

Fig. 1. Design space in terms of transistor dimensions (width W and length L). Almost 2 decades of variations in W and L design values must be supported with accurate variability-aware design tools to enable design of Logic standard cells, SRAMs, Analog-Mixed signal (AMS), and accurate Analog circuit blocks.

Circuit operation in Low Power/ Ultra Low Power (ULP) mode is critical for Internet-of-Things applications; examples are Low Voltage Digital SOC [19] featuring static and dynamic power reduction and Low Power Low Current Analog/RF design techniques where high value of short channel transit-frequency is subject to trade-off against power [20]. Indeed, MOSFET operation near threshold voltage *Vth* region is gaining in importance. It is well known that *Vth* variability impact dramatically increases in moderate inversion region, in particular due to the higher sensitivity of MOSFET channel charge to surface potential.

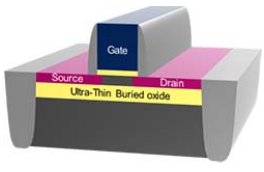

Fig. 2. UTBB FDSOI transistor structure operates as a double-gate asymmetrical transistor. Substrate region below Buried Oxide (BOX) is used as a back-gate.

We take as example UTBB FDSOI device (Fig.2). Experimental evidence of degradation of current variability at low gate voltage operation is shown in Fig.3.

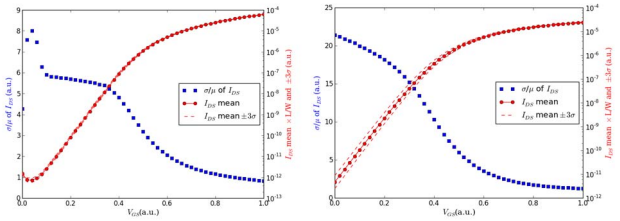

Fig. 3. Experiments of local statistical variability (σ/μ ratio, where σ is standard deviation and μ is mean value) and its dependence on *Vgs* gate voltage. SV data are for *Ids* saturation current from UTBB FDSOI transistors with long channel (left) and short channel (right). 512 samples from 1 die. σ/μ ratio increases from strong to moderate inversion., with a ratio x3/x5 respectivelly for long/short channels

While design margins versus specifications tends to reduce in particular due to combined geometry and bias scaling, the motivation for developing accurate variability models is to assess yield, to quantify the relative contributions of sources of yield loss, and to evaluate efficiency of circuit compensation techniques.

We propose a classification of variability models with respect to existing process, layout and circuit mitigation techniques (table I). In particular, variations not captured by either process or layout mitigation techniques need to be accurately modeled. This is the case for device level variations such as Local Layout Effects and Statistical Variability; those are quite influenced by device integration decisions oriented to meet Performance/Power device targets, and circuit compensation techniques are less efficient for device scale granularity. Seen from circuit design perspective, each device must be considered in the design flow as a unique instance exposed to local systematic layout effects and local statistical variations. This requirement translates into an accurate description of device electrical characteristics with a nominal model (section III), combined with a set of LLE models (section V) and SV models (section VI). With the assumption that those effects are mutually independent, each transistor parameter P is expressed in different normalized absolute or relative forms reflected in the 2 equations below:

$$P = Po + \sum \Delta P_{LLE} + \sum \Delta P_{PV} + \sum \Delta P_{SV} \quad (1)$$

$$P = Po \times \left[1 + \sum \Delta P_{LLE}/Po\right] \times \left[1 + \sum \Delta P_{PV}/Po\right] \times \left[1 + \sum \Delta P_{SV}/Po\right]$$

Where Po represents nominal value validated in well-established process, layout, and temperature conditions; ΔP_{LLE}, ΔP_{PV}, ΔP_{SV} represent corrections for LLE, PV, and SV variations respectively.

III. Nominal Model

Nominal model is used as reference and its accuracy throughout range of dimensions, temperature, and biases is a pre-requisite to elaborate accurate variability models.

We illustrate this statement with SV experiments of *Ids* and its *Vgs* dependence for different channel lengths here. For Low Voltage/Low Current application, we represent *Ids* σ/μ ratio and its dependence on *Vgs* and $\log_{10} Ids$, respectively for a long and a short channel UTBB FDSOI device. In fig.4, we put in perspective experimental values for *Ids* σ/μ ratio with *gm/Ids* ratio from the same experiments, where *gm* is defined as transconductance $gm = \partial Ids/\partial Vgs$.

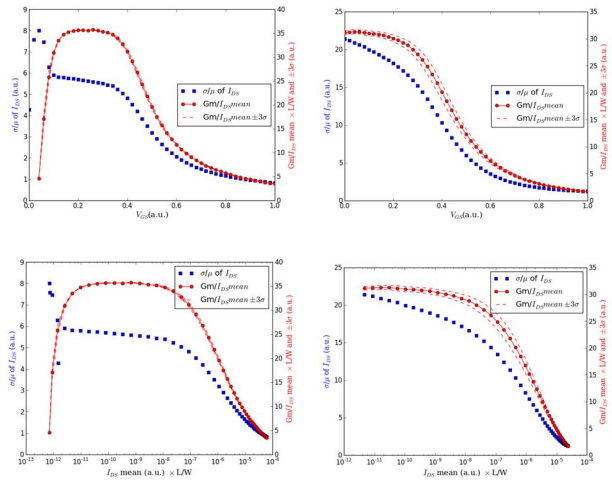

Fig. 4. Comparison of statistical variations for saturation current Ids (σ/μ ratio) with gm/Id trend (mean value +/- 3 σ,). Data are from UTBB FDSOI transistors with long channel (left) and short one (right). Same data set is represented as function of Vgs (top) and $\log_{10} Ids$ (bottom). Consistent arbitrary units are used for 4 plots.

The relationship between *Ids* σ/μ ratio and *gm/Ids* can be established using a simple power law current model applicable at the onset of strong inversion $Ids \propto \beta \times (Vgs - Vth - Dibl \times Vds)^{a}$, where β is gain factor, *Vth* is threshold voltage, *Dibl* is Drain-induced barrier lowering coefficient, *Vds* is drain-source voltage, and $a \in [1\,;2]$; we also assume that β, *Vth, and Dibl* are statistically independent as far as SV is concerned, and neglect potential SV contribution coming from series resistances at low gate voltage.

In these conditions, the dependence of long channel *Ids* σ/μ ratio on *Vgs* can be reduced to equation (2) which is similar to previous work under same assumptions [21-23]. The only difference remains in the addition of Dibl effect which we have added given its potential impact on SRAM design [24].

$$\left(\frac{\sigma_{Ids}}{Ids}\right)^2 = \left(\frac{\sigma_\beta}{\beta}\right)^2 + \left(\frac{gm}{Id}\right)^2 \times [\sigma_{Vth}^2 + Vds \times \sigma_{Dibl}^2] \quad (2)$$

In second term, gm/Ids ratio captures *Vgs* dependence; it leads to strong σ_{Ids}/Ids increase from strong inversion region (Vg > 0.6 a.u.), to weak inversion (Vg < 0.4 a.u.), where it becomes dominant. In weak inversion, gm/Ids exhibits a plateau over 4 decades of current; similarly σ/μ ratio exhibits a quasi-plateau, with a slight increase while reducing *Vgs*. For the short channel device, gm/Id shape is close to a plateau while σ/μ exhibits yet an unexplained continuous increase from weak inversion region to off-state region (Vg =0.0 a.u.). Equation (2) needs to be re-considered for weak inversion; we use a simple current model for that, $Ids \propto \beta \times \exp\left(Vgs - Vth - Dibl \times Vds\right)/\left(n \times ut\right)$, where sub-threshold slope *n,* and thermal voltage *ut* are introduced. Assuming statistical independence between β, *Vth, Dibl,* and

n, the following expression for *Ids* σ/μ ratio on *Vgs* can be derived for weak inversion

$$\left(\frac{\sigma_{Ids}}{Ids}\right)^2 = \left(\frac{\sigma_\beta}{\beta}\right)^2 + \left(\frac{gm}{Ids}\right)^2 \times \left[\sigma_{Vth}^2 + Vds^2 \times \sigma_{Dibl}^2 + (Vgs - Vth)^2 \times \left(\frac{\sigma_n}{n}\right)^2\right] \quad (3)$$

Note that equation (3) applies in weak inversion; it is similar to (2), apart from the fact of considering *n* variability. From second term of (3), 2 observations can be made: (i) σ/μ in subthreshold is controlled by gm/Ids, which confirms the importance of gm/Ids accurate nominal model for statistical modeling in low voltage, (ii) not only *Dibl* contribution is suspected to rise the plateau σ/μ, but subthreshold slope *n* needs to be considered as well as a potential contributor for SV degradation from threshold region to off-state.

To summarize, an accurate nominal model for *Ids* current and its derivatives (e.g. *gm/Ids* figure for variance estimate) is a prerequisite for reliable estimates of variability figures with circuit simulation in low voltage operation. This applies for whatever MOSFET device architecture and relies on accurate modeling of electrostatic figures (*Vth, Dibl, n*) and mobility (also detailed in [47]) at low/high electrical field induced by all terminals, including back gate for UTBB FDSOI devices.

IV. Process Variability (PV)

Process Variability includes long range variations of device dimensions, gate work function, mobility and series resistances, not excluding metal and inter-metal dielectric layers. In UTBB FDSOI transistor with low doped channel, dependence of 2D electrostatic and transport parameters on variations in front and back gate dielectric thicknesses, silicon film thickness are of prime importance, and must be valid against geometrical space of channel width and length, and full range of front and back-gate bias conditions.

Example of compact model validation of 2D electrostatics against TCAD for a wide range of process variations is shown for UTBB FDSOI in Fig.5 [25]. Compact model predictivity versus PV is must-have to enable process variations aware ULP circuit design.

V. Local Layout Effects (LLE)

LLE include all sorts of local Layout dependent systematic effects. Referring to table 1, some effects are unintentional like residual (after OPC) pattern rounding, well implants proximity [26], and STI stress [27]. Intentional effects are a consequence of strain-engineering techniques adopted to boost nominal device performance: Nmos boost by tensile contact etch stop layer (CESL) [28], Nmos and Pmos boost by dual stress liner (DSL) with tensile and compressive longitudinal stress respectively [29], compressive SiGe source/drain for Pmos [30], are techniques that lead to non-uniform stress distribution in the channel, therefore enhancements in carrier mobility and threshold voltage strongly depends on layout parameters. Last, SiGe channel has been introduced for UTBB FDSOI Pmos [31]; Ge induces compressive strain in SOi film, which tends to relax at the edges of the active area [32].

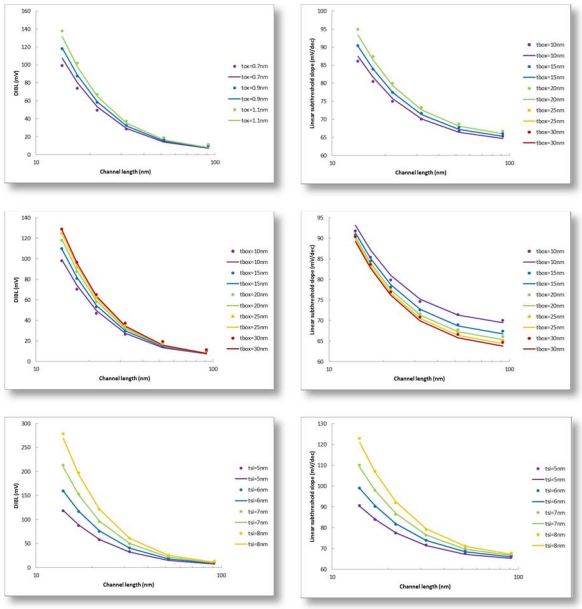

Fig. 5. Examples of compact model validation against TCAD for UTBB FDSOI 2D electrostatic parameter variations DIBL (left) and subthreshold slope (right) [25]. Impact of wide range thickness variations from front-gate and back-gate dielectrics, silicon film (respectivelly *tox, tbox, and tsi*), is reflected in a wide space of Length scaling (from 100 to 14 nm) and back-gate bias (+/-3V).

For reliable circuit design, those proximity effects must be either mitigated by layout constraints to improve uniformity in mobility enhancement, or accurately modeled after physical layout. The capabilities of post layout design tools have been greatly enhanced to analyze each device proximity and extract all critical distances (Fig.6) needed to evaluate LLE impact; post-layout extracted parameters are passed to physics-based LLE compact model extensions in order to estimate the deviation of each device characteristics

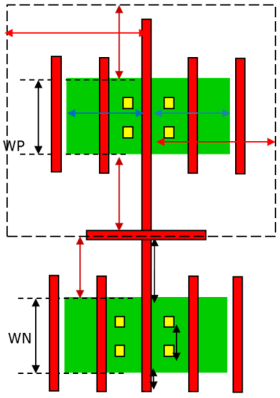

Fig. 6. Example of layout parameters extracted for post-layout circuit simulation (simple inverter case in planar CMOS)

We take UTBB FDSOI PMOS with SiGe channel as an example of LLE implementation here; measurement of strain relaxation at the edge of active region has been used to derive an analytical expression for Leti UTSOI compact model which accounts for electrical parameter dependence on active length and position of gate within active region (Fig.6) [25].

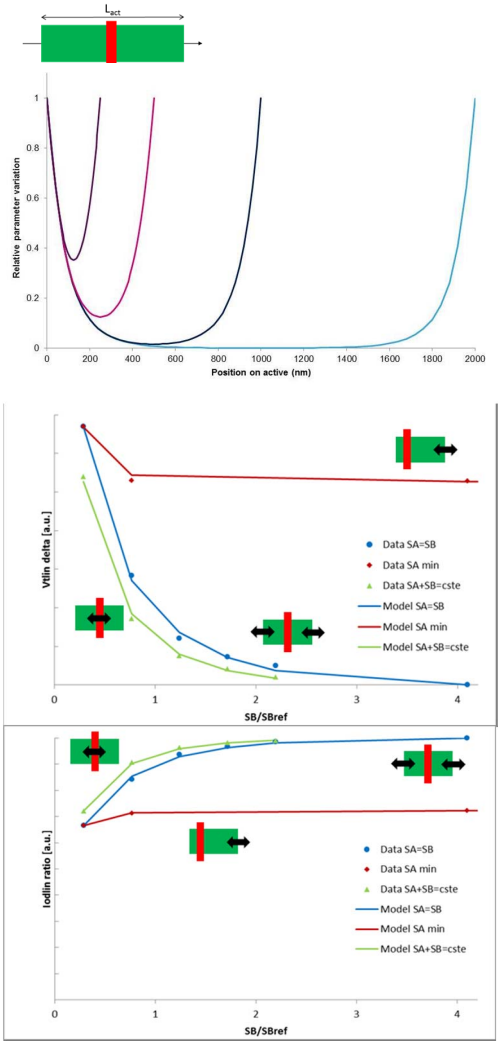

Fig. 7. LLE characteristics of UTBB FDSOI PMOS with SiGe channel strain. Model for relative electrical parameter variation along active length *Lact* (top) is inspired from shape of Strain Profile close to active edges. *Vth* shift (middle) and *Ids* shift (bottom) and their respective dependence on gate to active distance *SB*, for 3 cases of gate position vs active: nominal length centered gate, nominal gate on active edge, and centered gate with varying length. Agreement between model (lines) and experiments (symbols).

The challenge in LLE accurate modeling is to guarantee full coverage in design space [33]. First, LLE are consequences of technology decisions oriented to optimize nominal device performance; LLE behavior beyond nominal device dimensions are stabilized lately in the development process (after OPC is developed) and remain sensitive to process, equipment, or fab change. Then, unless regular layout practice is adopted, a large number of different layout situations are potentially met in real design such as logic cells, in which LLE effects interplay differently. In advanced technologies with complex design rules and wide choice of device flavors, LLE characterization and modeling is primarily focused on individual LLE effects, with some interactions accounted (LLE impact depends on W/L ratio). Considering presence of 5 sensitive LLE in a given planar CMOS technology, 20 different W/L ratios per device flavor, and test-structure design-of-experiments (DOEs) with 5 values of critical distance per LLE of interest per W/L value, up to 500 device-under-test (DUTs) with different layout need to be generated and characterized per device flavor. In the perspective of ULP design, some simplifications must be made to reduce the risk of inaccurate design in particular due to unexpected layout-induced shift of some critical parameters (*Vth, Dibl,...*) in conditions where model accuracy cannot be fully guaranteed (LLE interactions), or LLE being not subject to regular monitoring. Here again, mitigation techniques by layout (relaxation of dimensions, pattern regularity), or stringent DFM application, should be considered with high interest; those are even more valuable for ULP than for circuit application at nominal supply voltage.

VI. Local Statistical Variability

Statistical Variability (SV) has gained much importance with device scaling. Initially a limiting factor for analog signal processing (digital-to-analog converters, reference sources,..), it has been identified early as a growing concern for future digital SOCs, including read/write circuit of memories, voltage margins of SRAM cell) [34], and increased relative variations in logic delays with respect to signal path length reduction, device smaller dimensions and reduced supply [35].

Over two decades, numerical modeling has gradually permitted to investigate sources of statistical variations in view of mitigating their impact by device optimization for planar CMOS technologies [36]. Variability-aware device simulation capabilities and their applications have dramatically grown along with technology scaling, not only to identify and assess impact of individual or combined variability sources of new planar devices [37-39] down to 20nm devices, but also to become essential part of sub-20nm innovative devices design with DTCO approach [17]. In recent development, for sub-20nm devices, simulation capabilities have been extended to account for interactions between statistical variability and different classes of variations including process variations [40], reliability [41], since those have been demonstrated to be significant as well for the devices of interest.

In the same period, compact modeling of statistical variability for circuit design has been significantly developed for planar CMOS. The simple *Vth-β* mismatch variance model [21] has been extended to account for non-uniform lateral channel doping due to pocket-implants introduced in 45nm planar devices [42] and semi-empirical corrections introduced

on case-by-case to account for limited scaling of line-edge roughness [45]. Such models have the advantage of simplicity: (i) mismatch variance for *Vth-β* model is characterized using observed differences between identical layout device pairs repeated once per die, (ii) sampling from 1 wafer with less than 100 devices is enough; (iii) compact model implementation in circuit design tools is straightforward.

Nevertheless, above simplification may degrade simulation accuracy of circuits using decananometer devices, in particular in the following cases (i) assumption of small variations and normal distribution for devices close to small dimensions such as SRAM [45] or reduced supply voltage, (ii) devices where correlation between matching parameters is present (iii) second–order SV contributions in case of gate-overdrive (Rseries) or reduced supply voltage (DIBL and sub-threshold slope, see section III example), (iv) device exposure to SV/PV interactions such as innovative sub-20nm FinFet devices [40]. For those applications, statistical compact model methodology need to be reviewed; an attempt to overcome these limitations has been conducted [46] where SV compact models parameters for PSP or BSIM are directly extracted from I (V) characteristics based on 3D atomistic device simulation.

We report in Fig.8 for first time about enhancements in electrical characterization for UTBB FDSOI devices, in order to explore statistical compact modeling approach similar to [46], but starting from statistical I(V) experiments. Note that complete assessment of such methodology is beyond the scope of this paper.

To summarize, accurate statistical compact modeling is instrumental for DTCO of sub-20nm devices, as well as to assess realistic circuit design margins for low voltage circuit applications. For those applications, the challenge in accurate statistical compact modeling methodology is to overcome the limitations of conventional *Vth-β* mismatch approach based on the assumptions of relatively small variations, Gaussian distributions, low SV-induced parameter correlations, and absence of PV/SV correlations. Good news is that this challenge is well addressed by current methodology development.

VII. Challenges

Challenges in compact modeling for reliable circuit design that were highlighted in previous sections are summarized below:

- Accurate nominal model for *gm/Ids* figure down to subthreshold transistor regime, and validated throughout design space of dimensions, voltage, and temperature.
- Scalability/Predictivity of electrical characteristics with respect to process variations (PV) including vertical and lateral dimensions (*tox, tbox, tsi for UTBB FDSOI devices)*.
- LLE model accuracy, combined with improved layout regularity adoption, in particular for low voltage circuits.
- SV models validated against high-order statistics, in particular for small devices under low supply voltage
- SV, PV, and Reliability interactions, in particular for sub-20nm devices
- Efficiency and accuracy of modeling methodologies
- For UTBB FDSOI devices, these requirements are supported by Leti UTSOI model development [48], and rely on advanced TCAD development as well [47].
- Not to forget temporal variability, out of this paper scope.

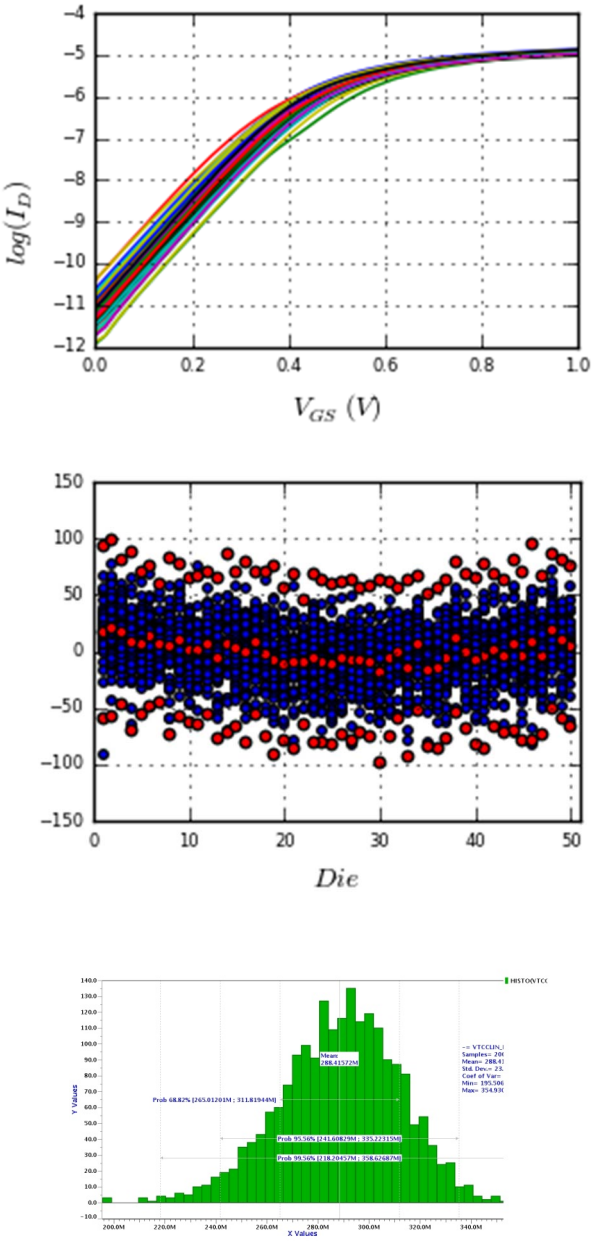

Fig. 8. Example of SV/PV experiments with a set of UTBB FDSOI identical devices with small dimensions repeated in Addressable transistors Array testchip. *Top*: I(V) data from 1 array (1 die) are exposed to SV only, and can be exploited for SV modeling . *Middle*: I(V) Data measurements are repeated per each device per die, and from die to die, from which transistor parameters are extracted. Example of 1 parameter as function of die position (blue symbols); PV presence is put in evidence (red symbols) by representing die average (PV) +/- 3 die sigma (SV). *Bottom:* Example of non-normal Vth distribution exposed to SV reflected in circuit simulation.

VIII. Conclusion

Variability has multiple contributions of different nature from technology and device. This challenge is still rising in importance both for devices scaled down to sub-20nm dimension range, and for decananometer devices exposed to supply voltage reduction for ULP applications.

In both applications, this challenge requires joint development efforts combining process and design mitigation techniques, with accurate compact modeling for assessment of design margins, in order to develop high yield products.

In this paper, the challenges for accurate modeling for circuit design have been reviewed with respect to process and design mitigation techniques, in order to be better identified.

The benefit of layout regularity is increasing with supply voltage reduction, since impact of systematic PV and LLE can be significantly mitigated, and better CAD tools accuracy can be afforded.

IX. Acknowledgment

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TABLE I. Overview of Variability Mitigation Techniques by Process, Device Modeling, and Circuit Design

Class	Variations			Technology	Device	Circuit Design	
	Components	***Sources***	***Scale***	***Process Mitigation***	***Modeling***	***Layout Mitigation***	***Circuit Mitigation***
Spatial PV Interdie	Lot/lot Wafer/Wafer Die/Die	Equipment	cm	Process trimming	Process Variations & Perf/Power Corner models		ASV ABB
Spatial PV Intradie	Pattern Density	Mask RTA CMP	mm	Smart Dummies		Smart Dummies & Common Centroid Devices	ASV fine-grain ABB fine-grain
Spatial PV Device	Pattern Proximity	Pattern shape & Environment	10 nm to um	OPC	Weff Leff corrections (Gate/Active Rounding)	DFM & Regular Layout	
	LLE	Well implants (WPE) Stress (STI, CESL, DSL, eSiGe S/D, eSiGe Channel)	10 nm to um	Smart Dummies	LLE models		
	Statistical Variability SV	RDD LER MGG	A nm nm	Implant conditions Litho/Etch Thermal Budget	Statistical models	Device dimensions Parallelization	
Temporal	Degradation	BTI, HCI	A	Gate dielectric	BTI, HCI Ageing models		ABB
	Noise	LF, RTN SN, TN	A		LF, RTN, SN, TN models	Low Noise device layout	

Variability impact on circuit design is multi-scale and requires concurrent engineering efforts to be addressed. Mitigation techniques by Process, Layout, and Design are applicable to reduce impact of Interdie and Intradie process variations (PV). Circuit mitigation techniques are more applicable at block-level. Device variability can be partly mitigated by Layout techniques, nevertheless mitigation of Local Layout effects (LLE) and Statistical Variability (SV) by Circuit techniques lacks of efficiency due to area penalty. Accurate PV, LLE and SV models are required to assess design margins versus specifications in general, as well as to optimize circuit mitigation techniques in terms of trade-off between Variability compensation and Silicon area.

Glossary: *Process Variations (PV), Rapid Thermal Anneal (RTA), Chemical Mechanical Polishing (CMP), Statistical or Stochastic Variations (SV), Random Discrete Dopant (RDD), Line-Edge Roughness (LER), Metal-Grain Granularity (MGG), Optical Proximity Correction (OPC), Local Layout Effect (LLE), WPE (Well-Proximity Effect), Shallow Trench Isolation (STI), Contact etch stop layer (CESL), Dual Stress Liner (DSL), Back-bias Temperature Instability (BTI), Hot-Carrier Injection (HCI), Low Frequency noise (LF), Random Telegraph Noise (RTN), Shot Noise (SN), Thermal Noise (TN), Design for Manufacturability (DFM), Adaptive Supply Voltage (ASV), Adaptive Body-bias (ABB).*

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