An Enhanced Specialized SiC Power MOSFET Simulation System

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Abstract—This work presents the recent progress in the development of a simulation system, CoolSPICE, specifically targeting high-power and high-temperature simulations of SiC power MOSFET devices in particular. CoolSPICE uses a subcircuit based on the conventional BSIM MOSFET model to represent SiC power MOSFETs. The BSIM equation set is modified and new parameters are added to the model set to account for the performance and behavior differences between conventional CMOS and these high power devices, while the robustness of BSIM is preserved. The parameter set is extracted by matching IV and CV curve measurements to simulations. Accuracy and robustness are verified by using this model to simulate typical power MOSFET circuit architectures.

Keywords—compact modeling; SPICE; BSIM; SiC; power MOSFET; circuit simulation

I. INTRODUCTION

We report recent work on a compact modeling system to simulate high power and high temperature circuits with specialized devices. The utility of the relatively new device material silicon carbide (SiC) ranges across power electronics applications such as converters and regulators, in areas from the automotive industry to industrial power. SiC exhibits favorable properties to be used widely in these areas, for instance a large thermal conductivity and wide bandgap. However, consequential properties such as low intrinsic carrier



This project is supported by US ARL cooperative agreement W911NF-12-2-0001 and OSD SBIR W911QX-13-C-0189.

concentration, incomplete ionization, and prevalent interface traps, which all need to be taken into account for accurate device modeling as well as circuit simulation, hamper the use of conventional circuit simulation tools [1].

The silicon CMOS world has long enjoyed the stable and robust compact MOSFET modeling system, BSIM, enabling rapid circuit prototyping and short times to market [2]. Fig. 1 shows the components for a typical SPICE simulation framework. The different power MOSFET structure, plus the demanding material properties of SiC and the wider application temperature and power ranges hinder accuracy for unmodified BSIM if used to simulate SiC power MOSFET-based circuits.

We had previously reported on the development of a CAD tool, CoolSPICE, which particularly targets SiC and high power circuits [3], extending the capabilities of a conventional SPICE-type simulator and of BSIM. Our previous work initiated some expansions to the BSIM equation set to accurately represent SiC power MOSFETs in the BSIM framework. Here we describe our recent work, including model improvements, and demonstrate the tool in operation.

II. SIC POWER MOSFET SPICE MODELS

We use subcircuits to implement the SPICE simulation of SiC power MOSFETs. Fig. 2 shows our updated subcircuit, constructed around a conventional BSIM MOSFET. Some BSIM equations have been modified to account for behavior specific to power devices. Some updates and modifications are as follows:

• Effective mobility and saturation velocity models are implemented to account for the behavior in the high voltage regime. SiC MOSFETs exhibit lower field-





simulations (solid lines) of a SiC power MOSFET and its model parameter set built by parameter matching.

effect mobilities at high bias, due to their surface roughness and large interface and oxide trap densities.

- The drain-to-gate and drain-to-source capacitance terms internal to BSIM are modified to account for the different structure of power MOSFETs, where, at high V_{DS} , C_{GD} is dominated by the capacitance of the depleted drift region, and C_{DS} by the body diode junction capacitance.
- To aid convergence, an equivalent body diode is placed between the source and drain terminals, instead of its nside connected to the far side of the drain resistance.

When implementing modifications to the BSIM framework, two important advantages for which BSIM was designed must be preserved. First, BSIM is notably robust over the common CMOS ranges of operation in terms of voltages, currents and time scales. Second, special care is taken in the BSIM equation set to yield continuous IV curves between the different modes of MOSFET operation. Our SPICE models for power MOSFETs preserve these advantages.

A. Changes to the Effective Mobility Model and Capacitive Model:

The changes in the current vs. voltage curves for SiC power MOSFETs progress differently than those for Si CMOS. For example, the increase in I_{DS} for equally-spaced changes in V_{GS} gradually decreases in a commercial SiC MOSFET. We have modified the conventional BSIM model to reflect this and other effects in simulation. One modification is the definition of a new effective mobility term:

$$\mu_{new} = \mu_{eff} \times \left[1 + \frac{\mu_{enh}}{1 + \exp[\mu_{factor} \times (V_{gseff} - \mu_{tran})]} \right]$$
(1)

Here μ_{enh} and μ_{tran} are new parameters added to the MOSFET parameter set and used in the proprietary equations we implemented within the SPICE engine in the CoolSPICE framework. V_{gseff} is based on built-in limits.

A typical power MOSFET is structurally very different from the CMOS devices BSIM was optimized to model. This requires the internal capacitance definitions of the BSIM model to be modified. To assure simulation accuracy and stability, in our implementation of CoolSPICE we have disabled the equation set describing the capacitances between the four terminals, replacing them with our own model equations. The equations describing the charge accumulation in different regions are also adjusted to keep the charge amounts consistent with the implications of the capacitance expressions.

III. SIC MODEL GENERATION AND LIBRARY CREATION

The modified BSIM equations implemented in CoolSPICE, as described in the previous section, require new parameters introduced into the MOSFET parameter sets. We have therefore developed proprietary model cards which include the common BSIM parameters as well as our modified parameter set. The parameter values must then be determined for the power MOSFETs intended for use in circuit simulations.

Our current work in progress is intended towards building a model card for every commercially available SiC power MOSFET currently in the market. At the current state of the industry this is a manageable task in terms of scale. These libraries can directly contribute to the pace of innovation in power circuit design using SiC devices, since they make rapid, accurate circuit development possible.

Our methodology is based on simulating the IV-curves of a commercial MOSFET using CoolSPICE with our proprietary model cards. We tune the parameter set by comparing simulated results to measured results at a number of temperature points. Through this process we derive the parameters and their temperature dependencies with a fair level of accuracy. We equipped the proprietary CoolSPICE engine with the ability to use the correct model card for the operation temperature, or to interpolate the parameter values between temperature points to match the operation temperature.

Fig. 3 shows example fits for the C2M0160120D device by Cree. The device characteristics at different temperatures are



(Top) C_{GD} is obtained from an internal Q_{GD} expression and matched to be consistent with the measured C_{RSS} vs. V_{DS} . (Datasheet: solid thin lines, C_{RSS} , C_{OSS} and C_{RSS} from highest to lowest; fit: dashed thick line.) (Bottom) C_{GS} and C_{LSS} curves are fit to built-in SPICE expressions. $C_{GS} \sim C_{LSS}$ since $C_{RSS} \sim C_{LSS} - C_{DS}$ is fit to match the $(C_{OSS} - C_{RSS})$ vs. V_{DS} measurement.

measured with an in-house setup which sweeps through a range of I_{DS} values at given V_{GS} values and measures the corresponding V_{DS} values. This is a pulsed measurement to ensure that heating effects are negligible, while the pulses are long to ensure that this is effectively a DC, not a transient, measurement (*i.e.* capacitive effects can be discounted). With this data, we then start out from a preliminary model card, which incorporates our modified parameter set as well, and refine its parameter values over successive simulations by CoolSPICE to match simulation to measurement. The fits are obtained at 25, 75, 125 and 200 °C respectively.

The capacitive model fits are based on data from the device data sheets. For power MOSFETs, data sheets typically provide the input capacitance (C_{ISS}), output capacitance (C_{OSS}) and reverse transfer capacitance (C_{RSS}) vs the drain-source voltage V_{DS} . The model parameters C_{GS} , C_{GD} and C_{DS} are related to these measured values as follows:

$$C_{GD} = C_{RSS}$$

$$C_{GS} = C_{ISS} - C_{RSS}$$

$$C_{DS} = C_{OSS} - C_{RSS}$$
(2)

We therefore match the parameters of our built-in proprietary expressions for C_{GS} and C_{DS} to the differences calculated according to (2) and the parameters of the same for C_{GD} to C_{RSS} , also making sure that the value for Q_{GD} calculated in the engine is consistent with this latter fit. (Naturally, C_{GD} is the derivative of Q_{GD} with respect to V_{DS} .)

Fig. 4 shows example matches of capacitance profiles for the same Cree device. The top panel shows the datasheet curves for C_{ISS} , C_{OSS} and C_{RSS} , and the fit of C_{GD} to C_{RSS} . The bottom panel shows the C_{GS} and C_{DS} values calculated from datasheet information as well as the fit to C_{DS} .



IV. MODEL FIT VERIFICATION

The model fits for the IV curves, during parameter extraction, are obtained by simulating a typical IV-curve measurement circuit (an NMOS connected to a voltage source at the drain and another at the gate and the source grounded; the gate voltage is stepped while the drain voltage is swept; a current meter records the drain current values). While we obtain reasonable matches with this approach, the model fit should be verified by circuits with varying functionality.

A. Verification by a Switching Circuit

A circuit setup used to verify the parameter set fits for both the IV and CV measurements, and therefore both the DC and transient performance of the model, is shown in Fig. 5. This single-MOSFET-switch circuit was tested at a variety of voltage levels for the gate pulse, corresponding to different V_{GS} ranges, and for the power rail voltage, corresponding to different voltage levels being blocked when the switch is off.

Fig. 6 shows the circuit used in CoolSPICE for this simulation. Additional parasitic components, e.g. a gate resistor, must be included in the simulation to match the transients accurately. Fig. 6 also shows transient matches at $V_{DD} \approx 15$ V and ≈ 500 V for the C2M0160120D device.

B. Verification of Model Stability by a Boost Converter Circuit

As mentioned in Section II, BSIM has been developed over the years to achieve a notably robust performance over the common CMOS current and voltage ranges of operation. This is an important characteristic required for reliable circuit design by simulation. However, SPICE can display convergence problems even in that range for certain circuit architectures, which have to be ameliorated by setting convergence-assisting options well-known to the community. The convergence problems can become more severe as the circuit voltage ranges and therefore the transient simulation step sizes increase.

In implementing our modified BSIM equation and parameter sets, we have to guarantee that these modifications do not damage the robustness of the framework, and that simulations using these sets are still free of convergence issues



(middle, left. V_{DS} fising edge, fight. V_{GS} fising edge) and full pulse match at VDD=500 V (bottom; the pulse with peak value ~20V is V_{GS} ; the other pulse is I_D in amps).

with the aid of standard SPICE options. To test this, we simulated a boost converter operation. Fig. 7 shows the circuit architecture and the simulation results. This circuit is not designed for optimal operation, but is meant to test simulation robustness with a 1 MHz switching frequency at kilovolt-level voltages. The simulation converges with no problems by setting tolerance levels and a minimum shunt resistance.

V. CONCLUSION

We have presented recent improvements to the capabilities of CoolSPICE, a compact modeling system targeting the simulation of high-power and high-temperature circuit operation with specialized devices. Here we focus particularly on simulating SiC power MOSFETs, whose different physical structure and performance characteristics require adaptations to the common BSIM framework which was originally intended to simulation silicon CMOS. We further demonstrate that our adaptations do not relinquish the BSIM advantages of continuous IV curves through different MOSFET regions of operation and of robust simulation in SPICE with the aid of standard convergence-assisting options.

We presently have an extensive library of commercially available SiC power MOSFETs for which we have measured



modified model and equation set during high-voltage simulations. Bottom: Simulation results: Inductor current waveform in the top panel, input and gate voltage waveforms in the lower panel (the higher and lower voltages respectively). Note that the voltage scale is in kilovolts.

the IV data at different temperature ranges. We are using the parameter extraction procedure outlined here to obtain SPICE model cards for these devices for use with the modified BSIM equation set of CoolSPICE. We are working to increase this number and keep it up to date as new devices are made available. We also intend to extend this work to SiC diodes, so as to enable the simulation of more power circuit architectures, which could use either kind of switching device.

ACKNOWLEDGMENT

This project is supported by the US ARL cooperative agreement W911NF12-2-0001 and OSD SBIR W911QX-13-C-0189. We thank OSD and ARL, and particularly Dr. Ronald Green and Dr. Aivars Lelis at ARL, for their support.

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