Design Optimal Built-in Snubber in Trench Field Plate Power MOSFET for Superior EMI and Efficiency Performance

Jingjing Chen
International Rectifier, An Infineon Technologies Company
101 N Sepulveda Blvd., El Segundo, USA
jingjing.chen@infineon.com

Abstract— **A 40V field plate trench MOSFET with optimal built-in snubber has been evaluated in Sentaurus TCAD, showing superior EMI and efficiency performance in the application of power sync-buck and power brick. We developed an advanced TCAD mixed-mode simulation to simulate switching performance of the field plate trench MOSFET with different built-in snubber resistance. Simulation demonstrates Vds damping effects through different snubber designs and an optimal range has been indicated. Physical insight has also been obtained through simulation by visualizing electrical field propagation and current distribution. In-circuit efficiency simulation demonstrates that with an optimize snubber design one can maximize the self-damping without penalization on the switching power losses or the product cost.**

Keywords-Field plate trench MOSFET, RC snubber, switching efficiency, EMI

I. INTRODUCTION

We have entered the age of limited energy resources amidst an emerging energy crisis. The fast evolutions in microprocessor and computing technology require the use of high frequency in the applications like DC-DC sync-buck or full bridge power brick, in order to achieve low cost, low profile, fast transient response and high power density. To meet the energy efficiency demand, there is a need for highly efficient, rugged and reliable power MOSFETs, capable of delivering high power without consuming much energy. However, high frequency also causes more power loss on MOSFETs. And in many applications, high amplitude current and voltage ringing appear after hard switching, being detrimental not only for electromagnetic compatibility but also for driver and FET reliability. So besides reducing the power loss, the major design considerations of a power MOSFET also include enhancement in dV/dt capability, reduction of electromagnetic interfere (EMI), and high damage immunity while switching large current in inductive loads. All these requirements make designing next generation MOSFET and optimization of the MOSFETs very challenging, as well as critical for the system performance.

Recently, field plate trench power MOSFET is gaining increasingly attention over traditional trench power MOSFET due to the much lower on-resistance (Rdson) it can achieve at the same breakdown rating [1-4]. Fig.1 shows the field plate trench MOSFET structure and equivalent circuit vs. traditional trench MOSFET. As shown in Fig.1 (a), the field plate trench structure utilizes oxide charge balance and two-dimensional depletion effect from the field plate electrode, altering the electrical field profile for higher breakdown, which enables increased doping concentration in the drift region, thereby reducing the Rdson significantly for a given chip size. In this study, the field plate in source trench enables a breakdown voltage 40V by using a 25V Epi. In addition, the field plate trench poly is shorted to source and functioning as a shield electrode beneath the gate electrode and converting most of the Cgd to Cgs. Hence the structure provides much lower Qgd by shielding the gate from the drain potential. Both low Rdson and low Qgd are essential for high system efficiency by reducing conduction loss and switching loss significantly compare with the traditional single trench structure shown in Fig.1 (b). Moreover, due to the resistance of the source trench poly, the field plate trench MOSFET inherently has a built-in RC snubber which is important for suppressing EMI. To understand the physical mechanism of RC snubber functioning in field plate structure and be able to do design optimization is critical for achieving ultra-low electromagnetic interference (EMI) noise and superior efficiency.

This paper investigates the impact of built-in snubber resistance on self-damping, power losses and system efficiency. An advanced TCAD mixed-mode simulation is developed to simulate switching performance and in-circuit efficiency of a 40V field plate trench MOSFET with different built-in snubber designs. Simulation demonstrates Vds damping effects through different snubber designs and an optimal range has been indicated. Physical insight has also been obtained through simulation by visualizing electrical field propagation and current distribution.

II. BUILT-IN SNUBBER IN FIELD PLATE TRENCH MOSFET

Snubbers are any of several simple energy absorbing circuits used to eliminate voltage spikes caused by circuit inductance when a switch opens. The object of the snubber is to eliminate the voltage transient and ringing that occurs when the switching transistor opens by providing an alternate path for the current flowing through the circuit's intrinsic leakage

978-1-4673-7860-4/15/$31.00 ©2015 IEEE

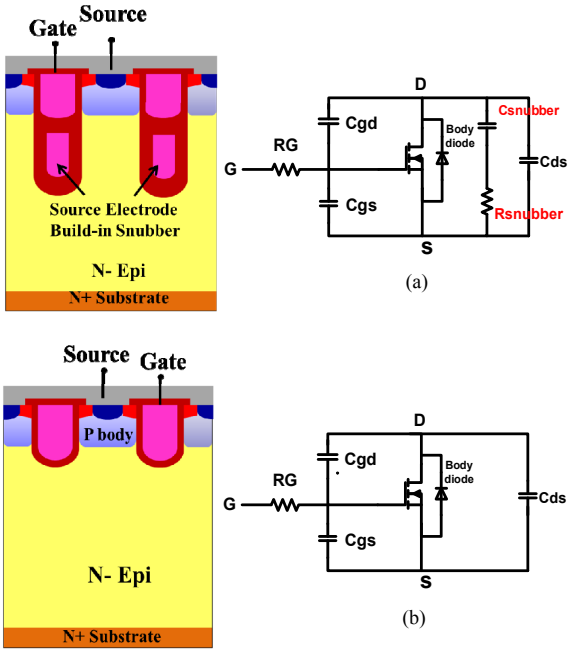


Figure 1. (a) Trench field plate structure and equivalent circuit. (b) Traditional trench MOSFET structure and equivalent circuit.

inductance. It helps to remove energy from a switching transistor and dissipate the energy in a resistor to reduce junction temperature. It reduces ringing and limits the peak voltage on the switching transistor or rectifier diode, and reduces EMI by reducing emissions and lowering their frequency. The most popular snubber circuit is a capacitor and a series resistor connected across a switch, which is also called as RC snubber.

As mentioned earlier, field plate trench MOSFET has a buried PolySilicon source electrode, which serves as a RC snubber (Fig.1 (a)). To obtain a good damping factor of the switching node, the combination of snubber capacitor (Cs) and snubber resistance (Rs) is important. The Cs of the field plate trench is defined by each technology, and can be optimized by source trench depth, field oxide thickness, cell pitch. The internal Rs is a result of the buried PolySilicon sheet resistance and die dimension. The Rs can be controlled by inserting multiple rows of source trench buses with contacts to the source metal, also by changing the contact spacing. In some situations, certain active area is sacrificed due to the source trench buses, and the maximum Rs is limited by the die dimension. Under these conditions, an intended optimized layout design provides full control on Rs. As a result of this control, Rs is tuned to damp current and voltage ringing in a similar way as with an RC snubber branch.

In the following section, a range of snubber resistance from 0.01Ω to 5Ω is simulated in TCAD switching simulation, to evaluate the impact on self-damping and power loss.

III. OPTIMUM SNUBBER DESIGN IN FIELD PLATE TRENCH

A. Optimize Snubber for Vds Ringing

Simplified circuit diagrams used in the mixed-mode circuit simulation are shown in Fig.2. All the parasitic inductors and resistors, based on the test board parameters, have not been shown here but are used in the simulation. Fig.2 (a) is a typical power sync-buck topology for reverse recovery simulation. Both ControlFET and SyncFET use the same snubber design but different die size according to the application requirement. Fig.2 (b) is the schematic used for in-circuit efficiency simulation. Q1 and Q2 are identical.

Fig.3 shows sync-FET Vds and Ids turn-off waveforms during reverse recovery for different source trench snubber resistance from 0.01Ω to 5Ω. As we can see from the waveforms, with Rs increases, Vds ringing reduces significantly. Also the voltage spikes and reverse recovery peak current are reduced accordingly. At 5Ω, a clear dynamic avalanche happens and voltage is clamped at the Epi breakdown level. An optimum range is defined between 0.5Ω to 1.5Ω for good self-damping without triggering dynamic avalanche.

Fig.4 (a) shows the transient electrical field distribution at the time when Vds first reaches 20V. With increasing snubber resistance, electrical field propagation along source trench slows down. The weakening of the field plate effect moves the high field from bottom corner of source trench to channel/epi junction, causing dynamic avalanche before breakdown. The electrical field profile along trench side wall changes from box shape to triangle shape, as shown in Fig.4 (b). With increasing snubber resistance, when dynamic avalanche happens, impact ionization also moves from source trench bottom corner to channel/epi junction, as shown in Fig.5. Therefore, more excess carriers have been generated at the channel/epi junction with higher recombination rate. The overall current density collected by contacts decreases, which significantly increases the conduction loss. The electron and hole distribution in the transient state at Vds=20V are captured in Fig.6 (a) and (b), which is different from the distribution at DC breakdown.

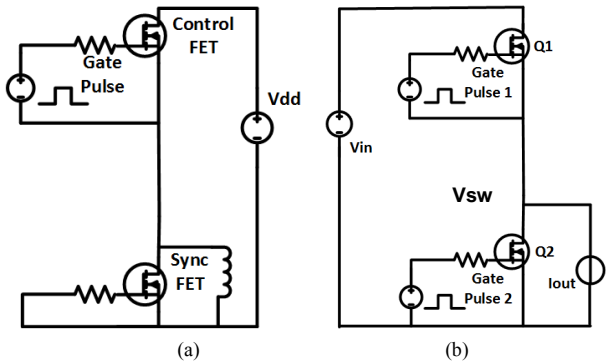


Figure 2. Simplified circuit diagrams for (a) SyncFET Vds ringing simulation. (b) In-circuit efficiency simulation.

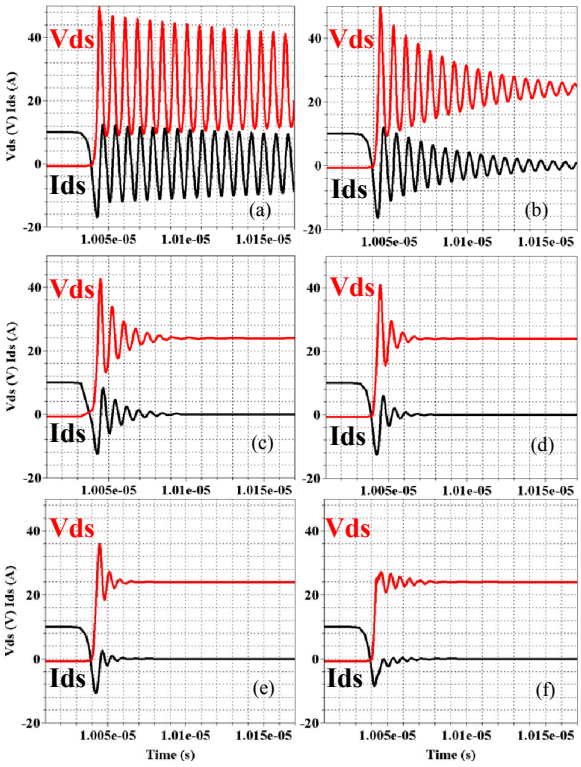
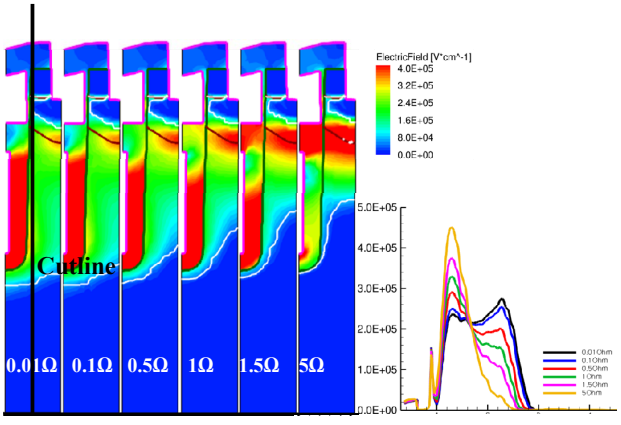


Figure 3. Simulated sync-FET turn-off waveforms during reverse recovery for different source trench snubber resistance, Vdd=12V, Iload=10A. (a) 0.01Ω. (b) 0.1Ω. (c) 0.5Ω. (d) 1.0Ω. (e) 1.5Ω. (f) 5Ω. Dynamic avalanche happens for 5Ω built-in sunbber design.



(a) (b)

Figure 4. (a) Transient electrical field distribution along the cutline captured at the first Vds=20V for different built-in snubber. (b) Electrical field profile with cutline along trench field plate side wall.

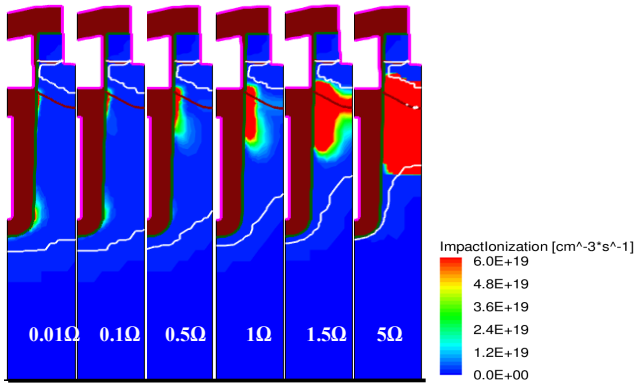
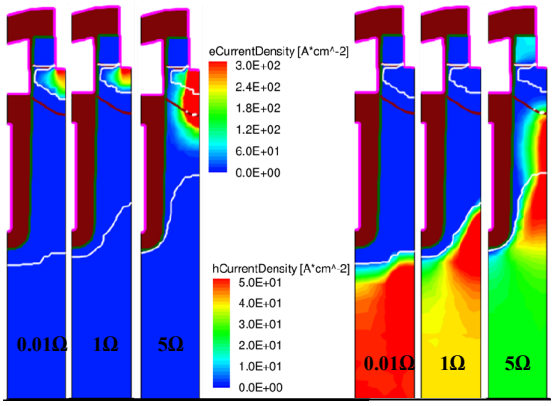


Figure 5. Transient impact ionization captured at Vds=20V for different built-in snubber.



(a) (b)

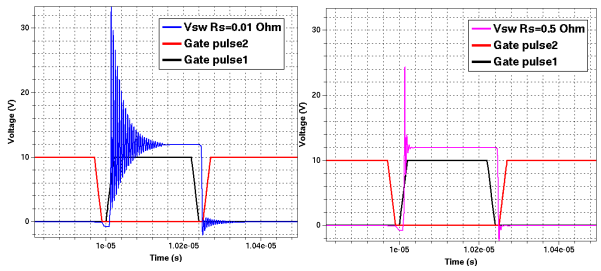
Figure 6. Simulated (a) Transient hole current density and (b) Transient electron current density distribution captured at Vds=20V for different built-in snubber.

B. Optimize Snubber for Efficiency

The efficiency is simulated at the input voltage 12V with the switching frequency of 600kHz and the dead time of 10ns, over full range of output current from 0A to 40A based on the schematic in Fig.2 (b). The efficiency is calculated from the overall power loss and the input power. From the system point of view, the overall power loss includes high side conduction loss, low side conduction loss, turn-on loss, turn-off loss, Qrr loss, gate loss and package loss. All the elements have been taken into account in the TCAD mixed-mode circuit simulation.

Fig.7 shows the switching node voltage waveforms and gate pulses waveforms for Rs 0.01Ω and 0.5Ω. The design with 0.01Ω Rs resistance shows a much higher voltage spike than the 0.5Ω Rs with ΔVsw=8V, and much more Vsw ringing during turn-on.

Fig.8 shows the simulated efficiency curves for all 6



(a) (b)

Figure 7. Simulated switching node voltage Vsw and gate pulses waveforms for (a) Rs=0.01Ω and (b) Rs=0.5Ω.

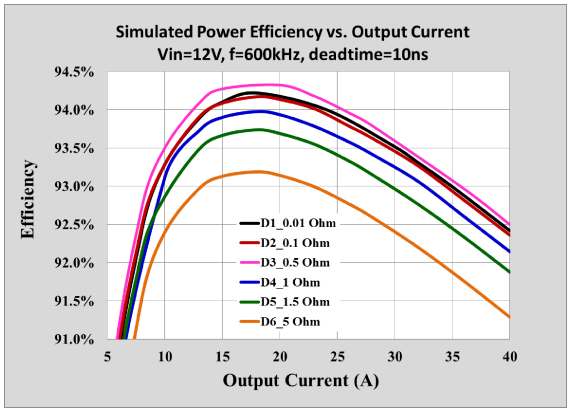


Figure 8. TCAD efficiency simulation for 6 designs with different built-in snubber resistancce.

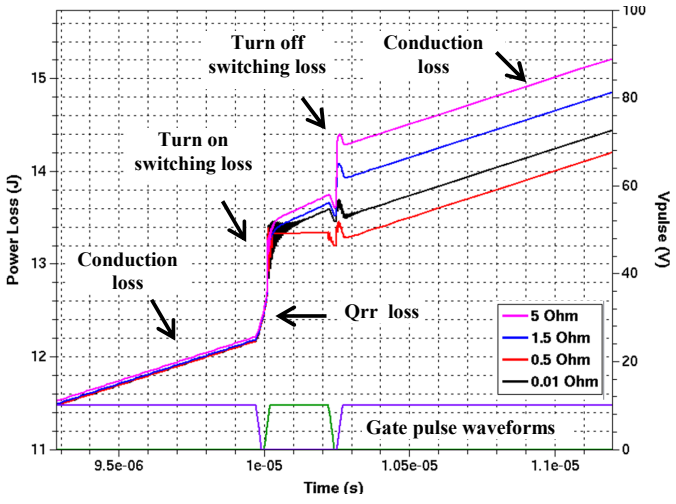


Figure 9. TCAD simulated power loss breakdown at output current 32A for different snubber designs.

snubber designs. The design with 0.5Ω Rs shows overall highest efficiency. However, further increase of Rs induces efficiency loss without much more benefit of Vsw and self-damping.

Complementary to the efficiency curves, Fig.9 shows the simulated power loss breakdown for different Rs at 32A output current as example. Using 0.01Ω Rs results in high Vds spike and ringing, contributing to more switching loss. With increase of Rs to 0.5Ω, the EMI reduces, resulting in a smaller switching loss and diode recovery loss. However, from that point, continuing the increase of Rs brings significantly increase of the conduction loss. Moreover, dynamic avalanche happens when resistance gets too high, which also induces higher switching loss. An optimal snubber value is desired to reduce ringing and voltage spike, and still maintains a superior efficiency performance. In this study, 0.5Ω is a good candidate.

IV. CONCLUSION

In summary, we have developed an advanced mixed-mode 2D circuit simulation to evaluate the impact of built-in snubber on the switching performance of a 40V field plate trench MOSFET. Results demonstrate physical mechanisms inside devices during switching. With an optimum snubber design, we not only can reduce Vds ringing and spike significantly, but also can maintain high efficiency by balancing the switching loss, conduction loss, diode reverse recovery loss and Cdv/dt effect.

.

ACKNOWLEDGMENT

The author would like to thank Jason Zhang for the valuable support and discussion in the project. The author would also like to thank Dr. Hsueh-Rong Chang and Dr. Henning Hauenstein for their support on the project.

REFERENCES

[1] Ritu Sodhi et al. "High Cell-Density, Shielded-Gate Power MOSFET for Improved DC-DC Converter Efficiency," *PCIM 2010 May*, pp. 45.

[2] T. Sarkar et al. "Enhanced Shielded-gate Trench MOSFETs for High frequency,High-efficiency Computing Power Supply Applications," *APEC 2013*, pp. 508.

[3] J. Yedinak, D. Probst, G. Dolny, A. Challa, J. Andrews, " Optimizing Oxide Charge Balanced Devices for Unclamped Inductive Switching (UIS)," *ISPSD 2010.*

[4] Jaume Roig et al. "Internal Self-Damping Optimization in Trench Power FETs for High-Frequency Conversion," *APEC 2014*, pp. 137.