

# Sandwiched-Gate Inverter: Novel Device Structure for Future Logic Gates

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**Abstract**—In this paper, we propose a novel sandwiched-gate inverter by using of an NMOS GAA together with a donut-type PMOS. The DC operation and the transient performance of the proposed inverter were investigated with 3D TCAD simulations. The proposed inverter exhibits a correct inverter operation with a high noise margin and speed.

**Keywords**—component; formatting; style; styling; insert (key words)

## I. INTRODUCTION

Over the last few decades, the size of the transistor has been reduced in order to improve its performance and to integrate more functions into a chip expedited by Moore's law. With the advancement of manufacturing technology, the transistor has been successfully scaled down to a technology node of 22-nm. However, the ability for gate to effectively control the channel diminishes due to such an aggressive reduction in size. The reduced controllability on the channel results in a significant increase in the leakage current and short channel effects (SCE). Short-channel effects such as subthreshold swing degradation, source/drain leakage current problems, larger drain-induced barrier lowering (DIBL),  $V_{th}$  roll-off, and  $V_{th}$  mismatch caused by random dopant fluctuations lead to dramatic change in the use of conventional planar devices for IC designs [1]. Therefore, the concept of multi-gate, such as double-gate or FinFET and triple-gate transistors, has been proposed and heavily investigated to overcome the bottlenecks for the continuous scaling [2]. As one of the most promising architectures for the ultimately scaled device, the gate-all-around (GAA) silicon nanowire transistor (SNWT) began to attract attention due to its excellent electrostatic capability of the channel control and efficiency of its practical design [3]. The paper is organized as follows: section II describes the proposed novel sandwiched-gate inverter. The proposed inverter can reduce circuit foot print and works properly. Section III describes the verification of the operation of proposed inverter, and Section IV concludes our works.

## II. PROPOSED NOVEL SANDWICHED-GATE INVERTER

In this study, we introduce a novel inverter structure in which the P-type GAA encloses a usual N-type GAA. Our research focuses on the proposal of novel inverter and

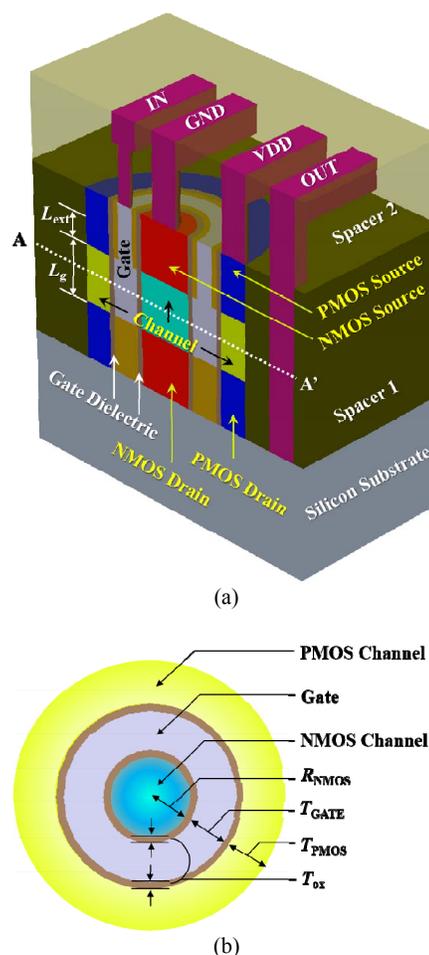


Fig. 1. Illustration of the proposed sandwiched-gate inverter. (a) 3D cross section, (b) cross section but through the channel region between point A and point A'.

verification. A sandwiched-gate inverter forms this structure as shown in Fig. 1 (a). A cross-section through the channel region between point A and point A' is illustrated in Fig. 1(b). As shown in Fig. 1(a) and (b), the NMOS silicon body is in the

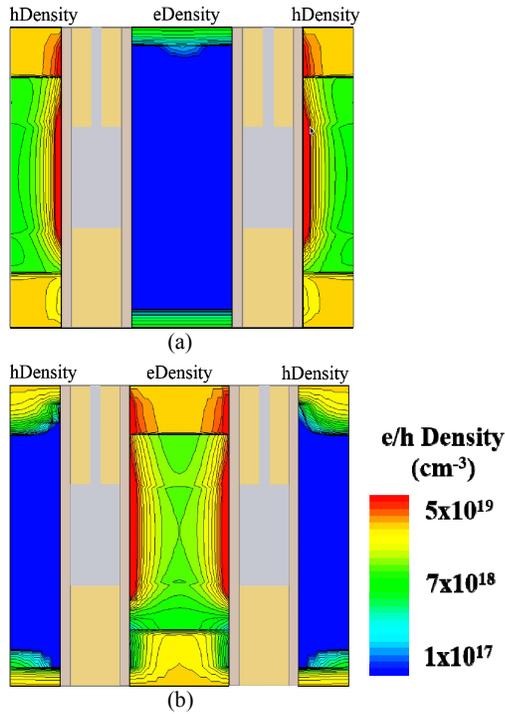


Fig. 2. The electron/hole density profile for (a)  $V_{IN} = 0$  V and (b)  $V_{IN} = 0.75$  V. The NMOS and PMOS channel are successfully turned off by an opposite gate bias.

Table I. Parameters in Simulation Setup

Parameter	Description	Value
$L_g$	Gate length	10 nm
$L_{ext}$	Source/Drain extension length	5 nm
$T_{ox}$	Gate dielectric thickness	1 nm
$T_{GATE}$	Gate metal thickness	5 nm
$T_{PMOS}$	P-type silicon thickness	5 nm
$R_{NMOS}$	N-type silicon radius	5 nm
$N_{SD}$	S/D doping	$2 \times 10^{19} \text{ cm}^{-3}$
$N_{ext}$	S/D extension doping	$2 \times 10^{17} \text{ cm}^{-3}$
$V_{DD}$	Supply voltage	0.75 V

center followed by the gate oxide. Then, the gate material is formed in the channel region surrounding the inner gate oxide to generate an N-type GAA transistor. In turn, the gate is surrounded by the outer gate oxide and, finally, the PMOS silicon body wraps around the outer gate oxide to make a sandwiched-gate structure. The regions between the sources and the drains of NMOS and PMOS are filled by spacer. To form a CMOS inverter, both the NMOS and PMOS drains are tied together at the bottom of the structure and connected to the contact (OUT) through the vertical metal. In addition, the source of NMOS is connected to the GND and the source of PMOS is connected to the VDD. The source (S) and drain (D) regions are highly doped ( $2 \times 10^{19} \text{ cm}^{-3}$ ) and the S/D extension

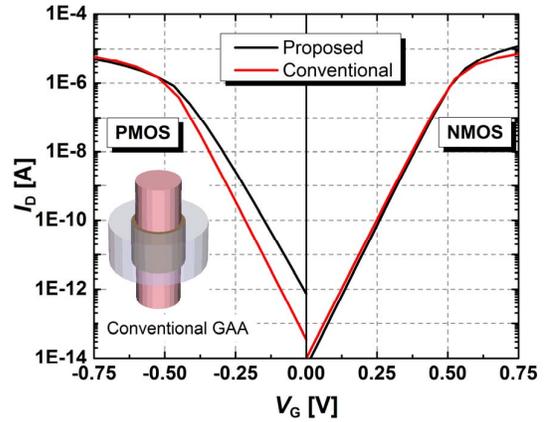


Fig. 3.  $I_D$ - $V_G$  characteristics of the PMOS/NMOS devices in the proposed inverter and individual conventional GAA SNWT (cylinder shape).

regions are lightly doped ( $2 \times 10^{17} \text{ cm}^{-3}$ ). The channel region is lightly doped ( $1 \times 10^{15} \text{ cm}^{-3}$ ) to avoid random dopant fluctuation (RDF). The structure dimension and parameter values used in this study are summarized in Table I.

### III. OPERATION OF PROPOSED INVERTER

To verify the correct operation of the proposed design as an inverter, DC simulations were conducted in a 3D-TCAD tool [4]. Fig. 2 (a) and (b) show electron and hole density profiles for  $V_{IN} = 0.0$  V and  $0.75$  V ( $V_{DD}$ ), respectively. As shown in those figures, the conduction channel is formed at the PMOS region (outer donut) when the input voltage is low (Fig. 2 (a)  $V_{IN} = 0.0$  V) and the conduction channel is formed only at the NMOS region (core) when the input voltage is high (Fig. 2 (b)  $V_{IN} = 0.75$  V). At the same time, the NMOS and PMOS channels are successfully turned off by an opposite gate bias.  $I_D$ - $V_G$  characteristics of the individual conventional GAA SNWT (cylinder shape) and the PMOS/NMOS devices in the proposed inverter are shown in Fig. 3. As shown, both NMOS and PMOS devices in our proposed inverter reveals similar electrical characteristics with the conventional cylinder shape GAA transistor. We investigated the relationship between the size of the NMOS (core radius,  $R_{NMOS}$ ) and the size of the PMOS (the outer thickness,  $T_{PMOS}$ ) so that the switching threshold ( $V_M$ ) of a proposed CMOS inverter is located in the middle between the supply rails. The voltage transfer curves of the proposed inverter for various  $T_{PMOS}$  to  $R_{NMOS}$  ratios are shown in Fig. 4 (a). The  $V_M$  values as a function of the  $T_{PMOS}$  to  $R_{NMOS}$  is plotted in Fig. 4 (b). As shown in those figures, the  $V_M$  becomes the middle of the  $V_{DD}$  (0.375 V in this study) when the ratio of the PMOS thickness to NMOS radius is 0.3:1 (e.g.,  $T_{PMOS} = 3$  nm and  $R_{NMOS} = 10$  nm). This PMOS/NMOS ratio can also be expected by considering effective channel area comparison. The switching threshold is determined by the current driving strength of PMOS and NMOS. In this way, we can calculate approximate value of ratio. As shown in Fig. 4 (a), the voltage transfer

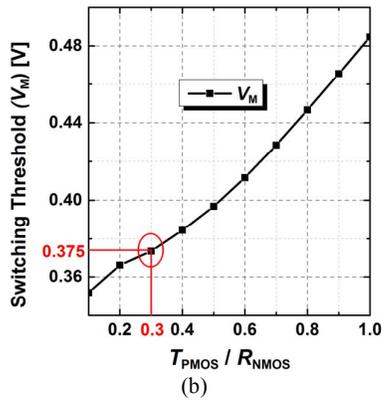
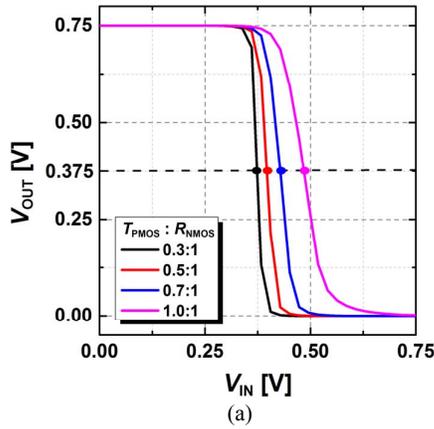


Fig. 4. (a) Voltage transfer curves (VTC) and (b) switching threshold ( $V_M$ ) as a function of the  $T_{PMOS}$  to  $R_{NMOS}$  ratio. The  $V_M$  becomes the half of the  $V_{DD}$  (0.375 V) when the ratio is 0.3:1 (e.g.,  $T_{PMOS} = 3$  nm and  $R_{NMOS} = 10$  nm).

curve with adequate sizing provides a remarkably high gain during the switching transient exhibiting a very narrow transition zone. Therefore, the proposed inverter has outstanding noise margin because of the steep slope in transition zone. Fig. 5 (a) shows the butterfly curves of the proposed inverter to estimate the static noise margins ( $NM_H$  and  $NM_L$ ) for various PMOS-to-NMOS ratios. Both low and high noise margins as a function of the ratio are plotted in Fig. 5 (b). The high noise margin ( $NM_H$ ) degrades rapidly as the  $T_{PMOS}$  gets thicker. As expected, the ratio range of between 0.3 and 1.0 provides the optimum low and high noise margin characteristics with approximately 0.345 V. As shown, the static noise margin of 92% of the half  $V_{DD}$  can be achieved by the proper sizing. Transient simulations are conducted to analyze the dynamic performance of the proposed inverter. A pulse of 10 ps rise/fall time is applied to the gate terminal and the propagation delay is measured between the input and the output of the inverter. The unloaded propagation delay of the size-matched inverter is 2.75 ps in a high-to-low transition and 2.6 ps for a low-to-high transition as shown in Fig. 6. In order to check that the proposed inverter will reduce layout area,

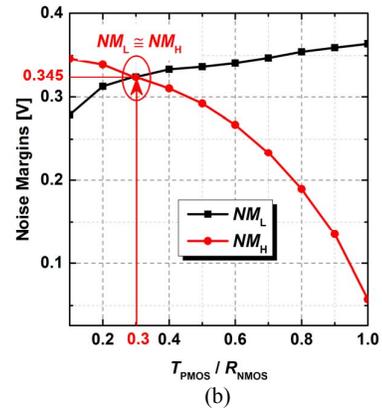
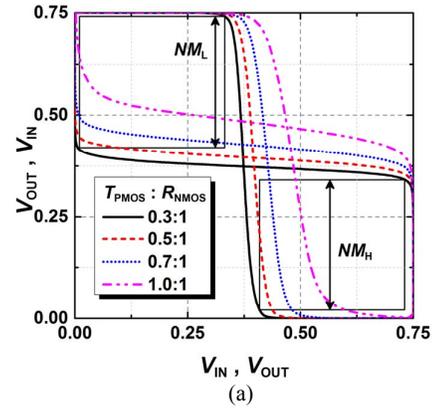


Fig. 5. (a) Butterfly curves and (b) static noise margins ( $NM_H$ ,  $NM_L$ ) for various PMOS-to-NMOS ratios. Note that, the 0.3-to-1.0 ratio provides the optimum and similar  $NM_H$  and  $NM_L$  with approximately 0.345 V.

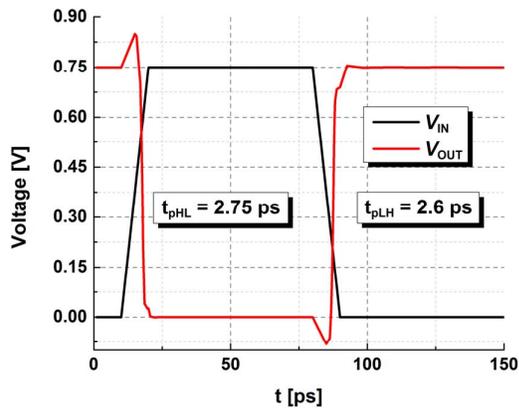
layout examples are illustrated in Fig. 7. In this example, 27% reduction in layout area can be achieved.

#### IV. RESULTS AND DISCUSSION

In this study, a novel sandwiched-gate inverter by using of an NMOS GAA together with a donut-type PMOS is proposed. The DC operation and the transient performance of the proposed inverter were investigated with 3D TCAD simulations. The proposed inverter exhibits a correct inverter operation with a high noise margin and speed. The novel inverter structure can be expanded to more complex logic gates, such as NAND and NOR gates, and will dramatically reduce the overall size of the chip when the manufacturability of the vertical GAA matures.

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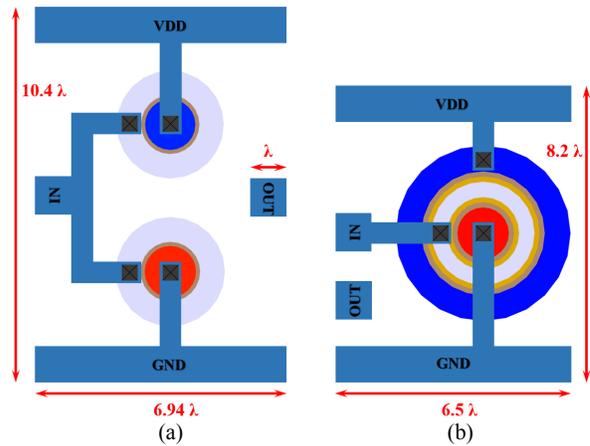
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**Fig 6.** Transient simulation of the proposed inverter for  $T_{PMOS} : R_{NMOS} = 0.3 : 1.0$  ratio. For unloaded inverter, the high-to-low ( $t_{pHL}$ ) propagation delay is  $2.75 \text{ ps}$  and the low-to-high ( $t_{pLH}$ ) propagation delay is  $2.6 \text{ ps}$ .

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**Fig 7.** General GAA inverter (a), proposed GAA inverter layout example. 27% reduction in layout area can be achieved in this example.