Simulation of thermal crosstalk of resistive switching memory in three-dimensional crossbar structure

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***Abstract*—Based on three-dimensional (3D) Fourier heat flow equation and numerical simulation, we investigated thermal crosstalk of resistive switching memory in 3D crossbar structure for the first time. Our results show that the transient thermal effect will dominate reset process. With the decrease of RS device size, the thermal crosstalk would remarkably deteriorate the retention of RS memory device and disable data storage. Some clues to improve the thermal crosstalk of RS device and RS performance in 3D crossbar structure are also provided.**

Keywords—Resistive switching memory; three-dimensional (3D) crossbar structure; thermal crosstalk; thermal effect; numerical simulation;

I. INTRODUCTION

Resistive switching (RS) memory has attracted increasing attention as potential next-generation nonvolatile memory [1-4]. To satisfy the increasing requirements for enormous data densities and nonvolatile storage, some new memory technologies are of growing interest due to their significant potential for the replacing or complementing existing memory technology (such as FLASH memory) [5-7]. High density 3-dimensional (3D) RRAM crossbar array is one of the major focuses for the new age technology [8-10]. More important, 3D integrated technology in resistive switching memory is one of the most effective methods to meet the requirement of ultra-high density and ultra-large data storage [11, 12]. To compete with the ultra-high density 3D NAND FLASH, understanding the reliability mechanisms and scaling potential in 3D RRAM crossbar array during operation is essential. Generally, Joule heating can impact on interconnect design by slowing down the current movement with increasing temperature [13]. Therefore, the thermal effect will seriously affect the stability, reliability and life of RS memory device. With increasing integration density, the RS memory device of 3D has a key challenge is how to solve the problem of thermal crosstalk. Especially, with increasing the storage cell density and decreasing the distance between adjacent cells, the thermal crosstalk will seriously restrict the development and application of RS device in 3D integration. However, it is very almost impossible so far for conventional thermal analysis method to measure the thermal effect of 3D RS device, therefore establishing a thermal effect model of 3D integration RRAM will contribute to further promote the development of 3D RS memory device. In this work, a simulation method was performed to theoretically investigate the thermal crosstalk in RS memory of three-dimensional crossbar structure.

II. THEORY MODEL

To illustrate the thermal effect and thermal crosstalk in 3D RS memory, the RRAM device of Ni/HfO_2/Pt and Ti/TiO_2/Pt diode cell based 1D1R (one diode one RRAM) structure are used as an example. The corresponding electrical parameters are the same as Ref. 14. Other inputting parameters for the simulation are shown in Table 1. Fig. 1 shows a schematic diagram of 3D RS crossbar structure. Based on 3D Fourier heat flow equation, the thermal behavior in 3D RS structure is written as

$$\nabla k_{th} \nabla T + \sigma |\nabla V|^2 - c\rho \frac{\partial T}{\partial t} = 0, \qquad (1)$$

here k_{th} is thermal conductivity, T is the temperature, c is the thermal capacity, ρ is the mass density of materials, V is the imposed voltage, t is time and σ is the electric conductivity which empirically reads as

$$\sigma = \sigma_0/(1 + \alpha(T - T_0)), \qquad (2)$$

here σ_0 is the electric conductivity at room temperature T_0, α is the resistivity temperature coefficient. Word lines (WL) or bit lines (BL) in the top and bottom layers of 3D array are assumed to be connected with ideal heat dissipation packaging structure and keep at room temperature T_0 during calculation, as

$$T - T_0|_{BC} = 0, \qquad (3)$$

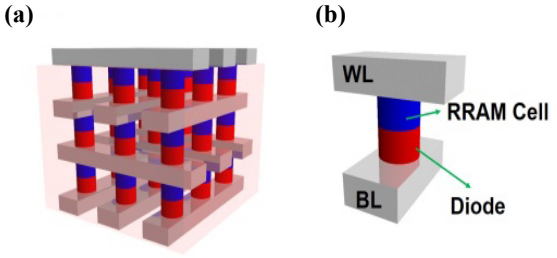

Fig. 1. Schematic diagram of 3D 1D1R crossbar structure (a) and 1D1R storage element (b).

III. RESULTS AND DISCUSSION

A. Thermal effect in 3D RS memory

To clearly understand the thermal crosstalk in 3D RS memory, we firstly investigate the dynamic temperature

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evolution in crossbar array system based on the 3D Fourier heat flow equation above by using numerical method. Figure 2 shows the simulated temperature evolution during reset operation for several cross-point arrays with different sizes. Here, all the RRAM cells are in LRS. Figure 2(a)-(d) illustrate the schematics of array structures in the simulation, including an individual RRAM cell and 3D RRAM arrays with various sizes from a 1×1×1 1D1R element to 3×3×3 block array, respectively. Figure 2(e)-(h) show simulated temperature evolution during reset process for different arrays in Fig. 2(a)-(d). The WL/BLs with the V_{reset} are marked in white and the ones being grounded are marked in black. The programmed RRAM cells are connected with on-state diodes (marked in green), and the unprogrammed RRAMs are connected with off-state diodes (marked in red).

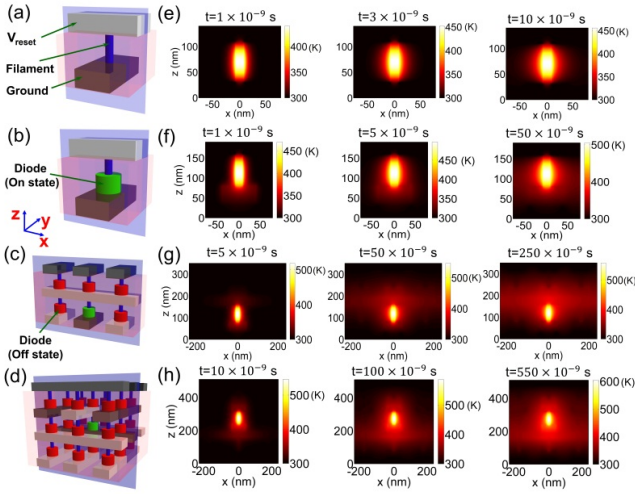

Fig. 2. Schematic diagram of the device structure: (a) an individual RRAM cell, and (b)-(d) 1D1R crossbar blocks with 1×1×1, 3×1×2, and 3×3×3 array, respectively. (e)-(f) Temperature evolution maps of the cross-sections (blue planes) in (a)-(d), respectively.

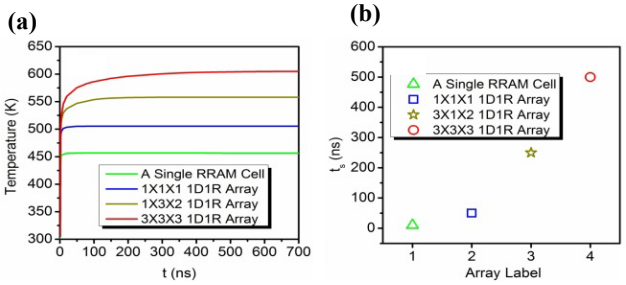

Fig. 3. Highest temperature evolution in the programmed RRAM cell with selected array structures in Fig. 2. (b) t_s (the time reaching thermal steady state) as a function of array.

Figure 3(a) shows the operated time dependence of temperature in programmed device in Fig. 2. Figure 3(b) shows the time t_s of reaching thermal steady state as a function of array. It is found that the temperature and t_s increase with increasing array, i.e., t_s is 50 ns for a 1D1R element, which is much higher than that of an individual RRAM (<10 ns), and t_s is 500 ns for a 3×3×3 block array. The peak temperature of steady state also varies remarkably with the array sizes (e.g. 500 K for a single 1D1R device, and 605 K for that in 3×3×3 array system).

B. Thermal crosstalk

To analyze the reliability of crossbar array, we simulated the 3D temperature profiles in a small 3×3×3 block array. Here, two 'worst cases' were chosen, as shown in figure 4(a)-(b). Figure 4(c)-(d) and figure (e)-(f) show the simulated potential distribution and temperature maps, respectively. It is found obviously that temperatures in the programmed RRAM devices rise much faster than those in the unprogrammed ones. In addition, temperature in the unprogrammed RRAM region passively increases with increasing time due to the thermal crosstalk effect.

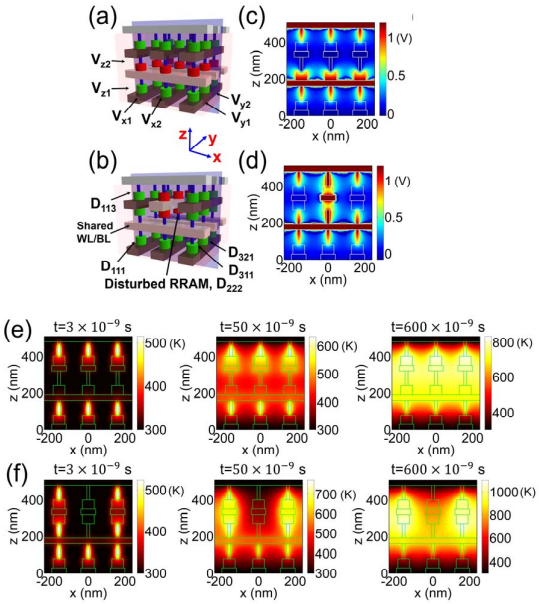

Fig. 4. (a)-(b) Schematic diagram of two selected 'worst cases' in thermal crosstalk. (c)-(d) Potential maps in the array structures in (a)-(b). (e)-(f) Temperature maps of the cross-sections (blue planes in (a)-(b)) for two array structures at different time, respectively. Disturbed RRAM device (labeled as D222) locates in the center of the array, which is surrounded by several programmed RRAM cells.

Figure 5 shows a conservative estimation of thermal crosstalk on RRAM device retention characteristic based on Arrhenius plot [16]. Arrhenius plot of the measured and simulated retention time (reference from Ref. 14 in which the conductive path of the RRAM device is simulated as metallic Ni rich filament) and the evaluation of the device reliability under thermal crosstalk. It is found that the thermal crosstalk will deteriorate the reliability, and the disturbed RRAM cell

will be failure from LRS to HRS after the programing/erasing cycles of 7×10^{11}.

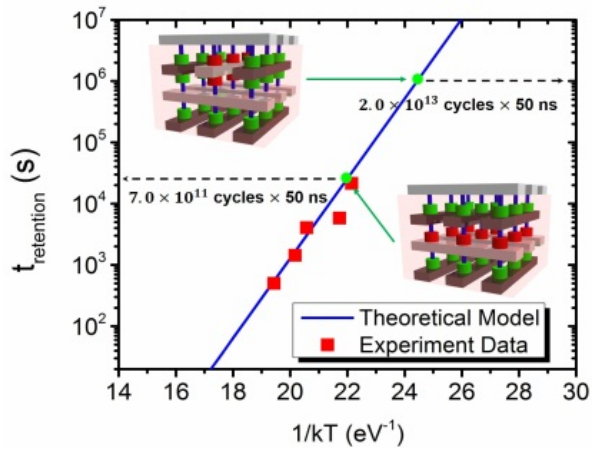

Fig. 5. Arrhenius plot of experimental [14] and simulated retention time, and the evaluation of the device reliability under thermal crosstalk. Here, assuming the reset time $t_{reset} = 100$ ns for a standalone 1D1R device, the peak temperature at $t = 50$ ns in the disturbed cell is 523 K and 475 K. Temperature could be converted into the retention time $t_{retention}$, which corresponds to $t_{retention}/(t_{reset} - 50\text{ ns}) = 7.0\times10^{11}$ and 2.0×10^{13} consecutive program/erase pulses (reasonable cycling expectations for RRAM devices).

Figure 6 shows that the different temperature dependence for a given 3D array when the programed RRAM cell locates in different layer, since the distances between thermal source (the programed RRAM cell) and the thermal dissipation boundaries (top/bottom electrodes in this work) are different. When the programmed cell is close to the top/bottom boundary, the generated Joule heat can be easily dissipated to the thermal sink boundary, and the corresponding temperature of the cell would be lower. Figure 6(d)-(f) show the temperature evolution maps for the 3 cases in Figure 6(a)-(c) while the programmed RRAM device locates in different layers.

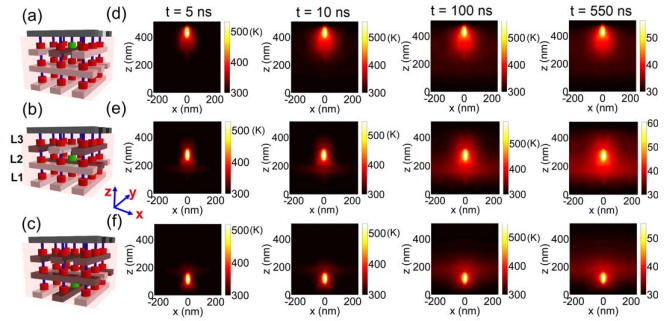

Fig. 6. (a)-(c) Schematic diagrams of the RRAM array structure selected for comparison, the programmed RRAM devices is in third layer, second layer and first layer in (a)-(c), respectively. (d)-(f) Calculated temperature evolution maps inside the arrays in (a)-(c). The WL/BLs imposed with Vreset are marked in white and the ones being grounded are marked in black. The programmed RRAM cells are connected in series with on-state diodes (marked in green), and the unprogrammed RRAMs are connected with off-state diodes (marked in red).

Figure 7 shows the highest temperature evolution in the programmed RRAM devices for the 3 cases in Figure 6(a)-(c). The highest temperatures of the programmed RRAMs could ultimately increase to 551 K, 605 K and 563 K in layer 1, layer 2 and layer 3, respectively. It can be predicted that with the growth of the layer stacks, the variation of the temperature in the programmed RRAMs in different layer would dramatically increase, which should be seriously considered during the array design and programing/erasing method optimization.

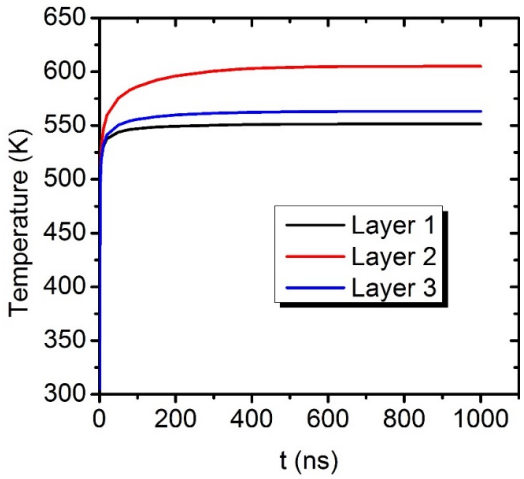

Fig. 7 Highest temperature evolution in the programmed RRAM device for the 3 selected cases in Figure S1a-S1c. Case 1-Case 3 correspond to the 3 cases in Figure S1a-S1c, respectively.

C. Improving methods

To continue miniaturization, a simple cycle-rehabilitate technique can be used: erase and reprogram the LRS of RRAM cells in the array after a certain operation cycles c_r. Using this method, the resistance of LRS in RRAM device deteriorated by thermal crosstalk could be rehabilitated by the reprogram operation, and scaling potential of arrays can be further promoted. In addition, an isolation material with higher E_a around electrode region, which could suppress the dissipation of the electrode material under Joule heating, is a possible method to increase the array endurance performance.

IV. CONLUSION

We proposed a theoretical model to study the thermal effect and thermal crosstalk of RS device in 3D crossbar structure.

Based on the proposed model, retention deterioration under thermal crosstalk and endurance degradation of RS device in 3D crossbar array were analyzed. Some methods for improving the RS device performance in 3D crossbar structure are also provided.

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Talbe 1. Paramters for simulation.

Parameter	Value
r_{ch}	8 nm
h_{cf}	80 nm
$k_{th\text{-}cf}$	22 W/(mK)
$\sigma_{0\text{-}cf}$	1.23×10^5 S/m
α_{cf}	0.0014
ρ_{cf}	8.9×10^3 kg/m^3
ρ_{im}	9.68×10^3 kg/m^3
r_{diode}	40 nm
h_{diode}	50 nm
$k_{th\text{-}diode}$	11.7 W/(mK)
c_{diode}	710 J/(kgK)
$\sigma_{0\text{-}diode}$	3.07×10^3 S/m
ρ_{diode}	4.17×10^3 kg/m^3
$k_{th\text{-}line}$	22 W/(mK)
$\sigma_{0\text{-}im}$	7×10^{-7} S/m
h_{line}	30 nm
w_{line}	80 nm
c_{line}	445 J/(kgK)
P_{line}	8.9×10^3 kg/m^3
$\sigma_{0\text{-}line}$	1.23×10^5 S/m
V	1.2 V
c_{im}	286 J/(kgK)
$K_{th\text{-}im}$	0.5 W/(mK)

Parameter describtion: r is radius, h is thickness, k_{th} is thermal conductivity, c is heat capacity, σ_0 is the reference electric conductivity and w is width. The subscripts *cf, diode, line and im* denote CF (conductive filament), diode, WL/BL component and insulating material between 1D1R cells, respectively. V is reset voltage, and $\sigma_{0\text{-}diode}$ list two values which correspond to the on-state value and off-state value of the diode device.