Power-Performance-Area Engineering of 5nm Nanowire Library Cells

Victor Moroz, Xi-Wei Lin, Lee Smith, Joanne Huang, Munkang Choi, Terry Ma, Jie Liu, Yunqiang Zhang, Jamil Kawa, and Yves Saad*
Synopsys, Mountain View, California, USA
*Synopsys, Zurich, Switzerland
Victor.Moroz@synopsys.com

***Abstract*—We benchmark planar MOSFETs, FinFETs, and nanowires in a wide range of design rules, spanning from 90nm down to 2nm. This benchmarking evaluates inverter switching speed for a load of 70 metal pitches long interconnect wire and a fan-out of one. Planar MOSFET logic slows down sharply at 14nm design rules, mainly due to short-channel effects reducing the driving strength at a fixed off-state leakage level. FinFETs take over at 14nm node and continue providing incremental gains down to 7nm design rules, but slowing down at 5nm due to the dominant parasitic middle-of-line capacitance. Vertical nanowires take over the lead at 5nm design rules and scale gracefully down to at least 5nm node. Based on these results, we perform detailed benchmarking of several design and process options for a 2-input NAND logic cell built on vertical nanowires with 5nm design rules. Benchmarking involves a holistic modeling methodology with 3D advanced carrier transport characterization of the nanowire behavior, 3D extraction of parasitic RC in the library cell, and simulation of power and delay of an 11-stage ring oscillator in HSPICE. Different cell designs and material engineering options offer cell area reduction of 33% with delay and power changing by over 2x.**

Keywords—5nm, nanowire, power-performance-area, standard library cell, transistor scaling, design rule optimization, MOL, ring oscillator, parasitic RC, holistic library cell analysis

I. INTRODUCTION

Nanowires (NW) have inherently better gate control than FinFETs which gives nanowires an advantage in off-state leakage at 5nm design rules [1]. A previous study showed that vertical nanowires exhibit considerably lower Middle-Of-Line (MOL) parasitic capacitance that makes them faster at the same power consumption energy with respect to FinFET and lateral nanowires [2].

Here, we perform two benchmarks of logic library cell performance. The first benchmark evaluates planar MOSFETs, bulk FinFETs, and nanowires in a wide range of design rules, from the 90nm node down to the 2nm node. This comparison is based on a simplified analysis of inverter switching delay for the average Back-End-Of-Line (BEOL) wire length.

The second benchmark compares several design choices for the logic library cells with vertical nanowires and 5nm design rules, based on detailed power-performance-area analysis of an 11-stage ring oscillator built with 2-input NAND library cells.

II. PLANAR VS FINFET VS NW

Historically, transistor strength per 1um layout width has been increasing steadily for planar NMOSFETs due to a combination of introducing High-K gate dielectric with Metal Gate (HKMG) and stress engineering, down to 32/28nm (Fig. 1). Further scaling to 22/20nm design rules slows down driving current improvement, whereas scaling beyond 20nm leads to a sharp performance loss, mainly due to strong Drain-Induced Barrier Lowering (DIBL) in planar MOSFETs with effective channel lengths below 25nm.

FinFETs enable scaling beyond 20nm design rules with continually improving performance, mainly due to the persistent fin pitch scaling. Nanowires exhibit a trend similar to FinFETs, extending down to at least 2nm design rules, with ~30% lower current levels than FinFETs, mainly due to the nanowire cross-section being smaller than the fin cross-section. Figure 1 depicts data for a single nanowire, whereas nanowire stacking can multiply its performance proportionally to the number of stacked layers.

For the performance of logic library cells, it is more important to characterize transistors that fit into the cell height, which scales approximately as 0.7x per technology generation. The average length of pin-to-pin BEOL wire also shrinks about 0.7x per node, whereas transistor strength reduces somewhat slower, at ~0.77x per node (Fig. 2), which is good news.

In addition to BEOL RC load, there is a MOL capacitance that became noticeable with the introduction of FinFETs and is expected to increase as 1/0.7x in the future, mainly due to the need to scale spacers separating the gate from the drain to be able to double transistor density per technology generation. FinFET MOL capacitance is expected to exceed the average BEOL load at 5nm technology node. The BEOL load here is defined for a typical pin-to-pin BEOL wire length of 70 metal pitches with 0.2 fF/um BEOL capacitance.

Lateral nanowires would have MOL capacitance close to planar MOSFET for a single nanowire layer, increasing towards FinFET level for the larger number of stacked nanowire layers. A vertical nanowire provides considerable MOL capacitance drop, due to the simultaneous reduction of capacitor area and the relaxation of the spacer width [2].

978-1-4673-7860-4/15/$31.00 ©2015 IEEE

Combining transistor strength data from Fig. 2 and inverter load data from Fig. 3, we obtain the inverter delay evolution, assuming fixed power supply voltage (Fig. 4). Planar MOSFET based logic slows down beyond 20nm. FinFET-based logic improves down to 7nm design rules and starts slowing down at the 5nm node, mainly due to the quickly increasing MOL load. Logic based on vertical nanowires exhibits noticeable performance gain over FinFETs at the 5nm node and continues improving at least down to the 2nm design rules.

III. 5NM POWER-PERFORMANCE-AREA ANALYSIS

Key design rules and assumptions for the detailed analysis of nanowire library cells with 5nm design rules are listed in Table 1. Considering that about a quarter of a typical logic chip is occupied by library cells that contain transistors connected in series, we choose a 2-input NAND logic cell that has 2 PFETs connected in parallel and 2 NFETs connected in series (Fig. 5).

A common way of building logic with vertical nanowires is to have all sources at the bottom and drains at the top [3]. That is the assumption we used to create design "A" (Fig. 6). Considering patterning requirements, this design can be built either with a combination of Extreme Ultra-Violet (EUV) lithography and Dynamic Self-Assembly (DSA) or with an octuple immersion lithography. There are 4 parallel NMOS nanowires and 4 parallel PMOS nanowires within the cell height.

Both the NMOS and PMOS nanowires are built with stress-free silicon, a channel length of 11 nm and a nanowire diameter of 5 nm. The NMOS on-state current is 702 μA/μm at 0.7 V Vdd and 1 nA/μm off-state current, assuming a 16 nm nanowire pitch. The PMOS has driving strength of 526 μA/μm, which is ~25% weaker than NMOS. The nanowire performance is characterized using 3D quantum transport analysis [4].

The 3D library cell has a footprint of 93 x 240 nm^2 and uses metal 0 (M0) through metal 2 (M2) layers, with two NFETs connected in series through an intermediate n-type island "n_i" (Figs. 7 and 8). The interconnects are made of barrier-less cobalt and have a "1D design" with M0 and M2 going North-South and M1 going West-East.

The 3D structure is created using Process Explorer [5] within 1 minute run time. A close-up cross-section of the NFET shows that an additional vertical nanowire is necessary to connect the two NFETs (Fig. 9). This increases the cell area and introduces an additional 40 kOhm resistance per nanowire. Parasitic capacitances of MOL and Back-End-Of-Line (BEOL) are calculated using Raphael [6] (Fig. 10).

An alternative approach to building logic on vertical nanowires is to swap locations of the source and drain whenever necessary to enable tighter nanowire placement. This design B shrinks the layout area by 33% and eliminates the need for metal 2 (Figs. 11 and 12). In addition, it eliminates the 40 kOhm parasitic resistance because now the drain of the first NFET connects directly to the source of the second NFET (Fig. 13).

Design B, despite smaller area, enables extending the number of parallel PMOS nanowires from 4 to 5, which improves the switching speed. In this design style, it is preferred to put the output pin z close to the middle of the cell height and input pins a and b close to the ground or power rails (Fig. 12).

Using the modeling methodology proposed in [2] that spans from quantum transport to SPICE circuit analysis, we evaluate energy per switch vs delay per switch of the 11 stage ring oscillator built with 2-input NAND cells, where design B shows clear power/performance advantage in a wide range of power supply voltages from 0.5 to 0.7 V (Fig. 14). Design C further improves the performance-energy trade-off by adding low-k spacers to design B. This improvement is mainly due to the low-k spacers enabling a reduction of the spacer width and therefore a reduction of the access resistance, which is a major factor for nanowires.

One important observation on Fig. 14 is the response to Vdd. A power supply of 0.6 V appears to be optimal, with power consumption sharply increasing for larger Vdd and switching delay sharply rising towards lower Vdd.

CONCLUSIONS

A benchmark of inverter performance with 70 metal pitches long BEOL load is performed for planar MOSFETs, FinFETs, and nanowires in a wide range of design rules, from 90nm down to the 2nm technology node. Comparative analysis shows FinFETs outperforming planar MOSFETs at 14nm and below, and then vertical nanowires taking over at 5nm design rules.

An approach for building logic library cells with 5nm design rules on vertical nanowires is proposed that provides a simultaneous 33% area shrink with either a 2x speed gain or a 2x reduction in power consumption. A holistic modeling methodology of transistor performance, MOL/BEOL parasitic resistances and capacitances, and circuit analysis enables early access to design optimization where considerable benefits are available at 5nm design rules.

REFERENCES

[1] J.-P. Collinge, "(invited) Multigate Transistors: Pushing Moore's Law to the Limit," Proc. of SISPAD, p. 313, September 2014.

[2] V. Moroz, L. Smith, J. Huang, M. Choi, T. Ma, J. Liu, Y. Zhang, X.-W. Lin, J. Kawa, and Y. Saad, "(invited) Modeling and Optimization of Group IV and III-V FinFETs and Nano-Wires," Proc. of IEDM, p. 180, December 2014.

[3] G. Larrieu and X.-L. Han, "Vertical nanowire array-based field effect transistors for ultimate scaling," Nanoscale, p. 2437, May 2013.

[4] M. Luisier and A. Schenk, "Two-Dimensional Tunneling Effects on the Leakage Current of MOSFETs With Single Dielectric and High-κ Gate Stacks," IEEE Trans. Electron Dev., v. 55, p. 1494, 2008.

[5] Process Explorer User's Manual, Synopsys, 2015.

[6] Raphael User's Manual, Synopsys, 2015.

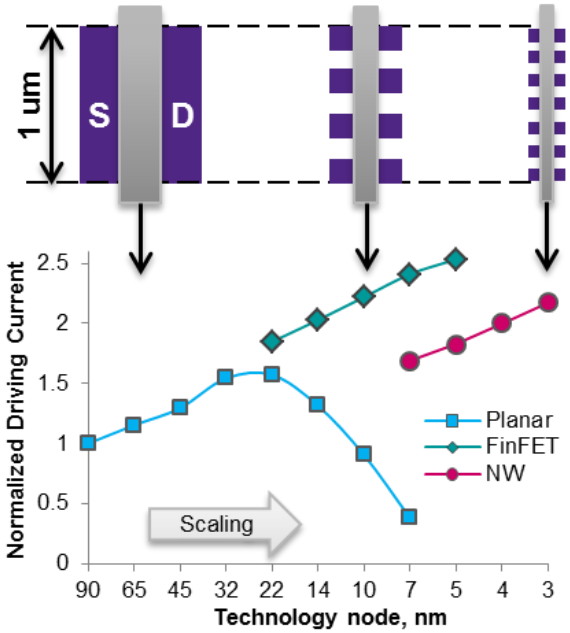


Fig. 1. Transistor strength evolution per 1um layout footprint and fixed off-state current and power supply

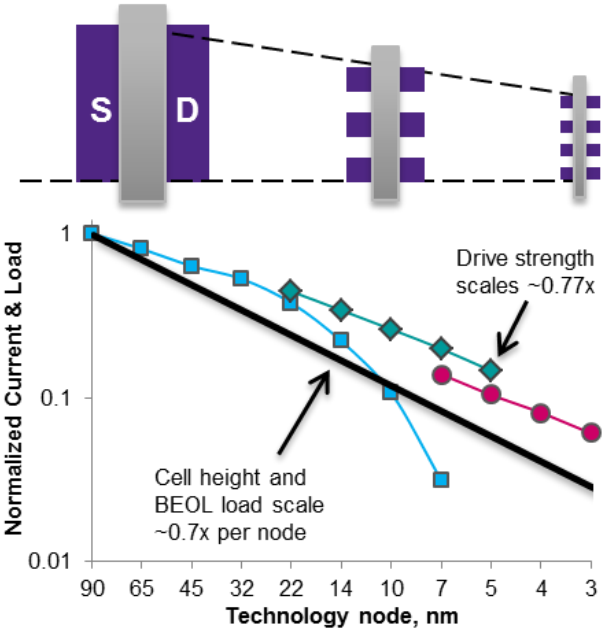


Fig. 2. Transistor strength evolution per layout footprint scaled along with library cell height scaling

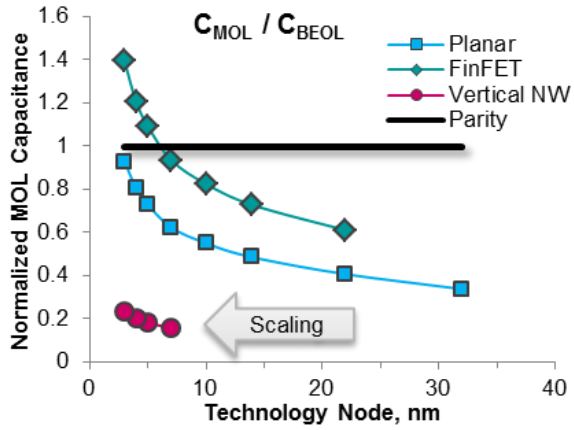


Fig. 3. Evolution of MOL capacitance w.r.t. BEOL capacitance for BEOL wire length of 70 metal pitches

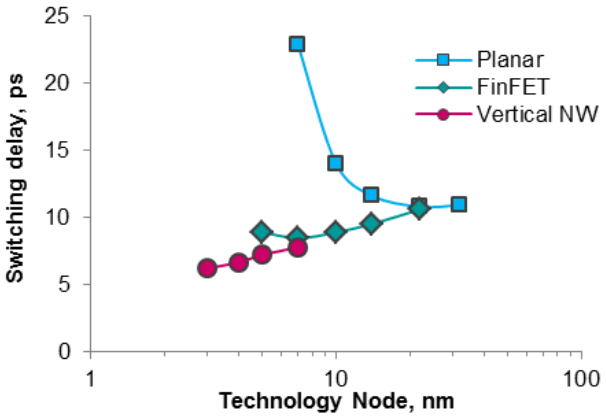


Fig. 4. Benchmarking performance of a 2x inverter built on planar, FinFET, and NW technology with fan-out of 1 and BEOL wire length of 70 metal pitches

Cell height	10 tracks
Metal 1 pitch	24 nm
Nanowire pitch	16 nm
Gate pitch	31 nm
Power supply	0.5 - 0.7 V
Channel material	Silicon
Off-state current	1 nA/um
Transistor architecture	Vertical NW

Table 1. Key design rules and assumptions

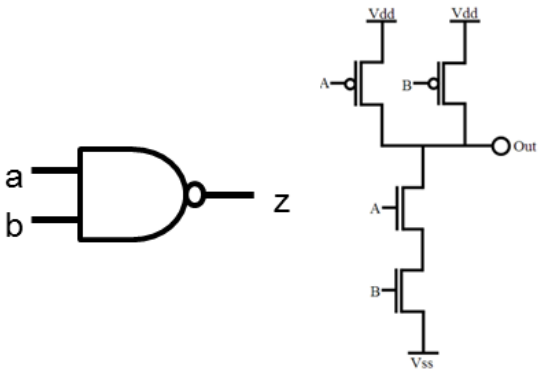
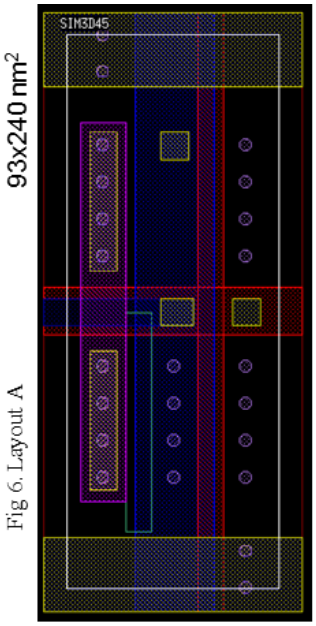


Fig 5. Two-input NAND logic cell



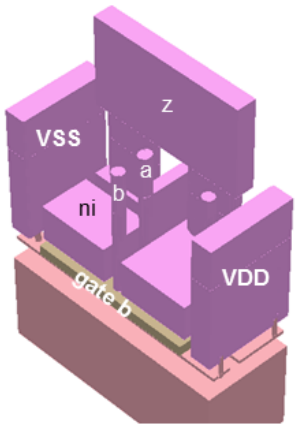


Fig. 7. 3D view of design A

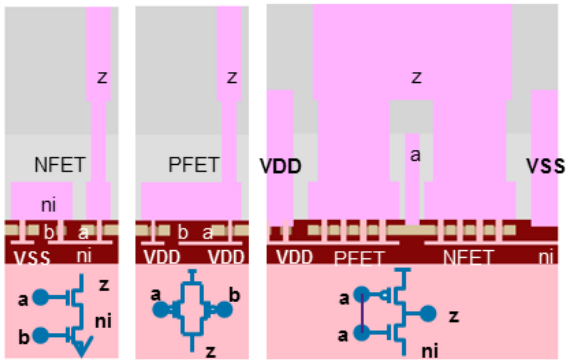


Fig. 8. 2D cross-sections of design A along cell width and cell height directions

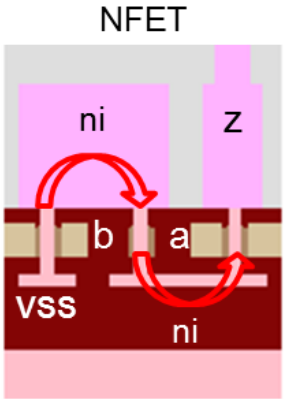


Fig. 9. Zoom-in into design A

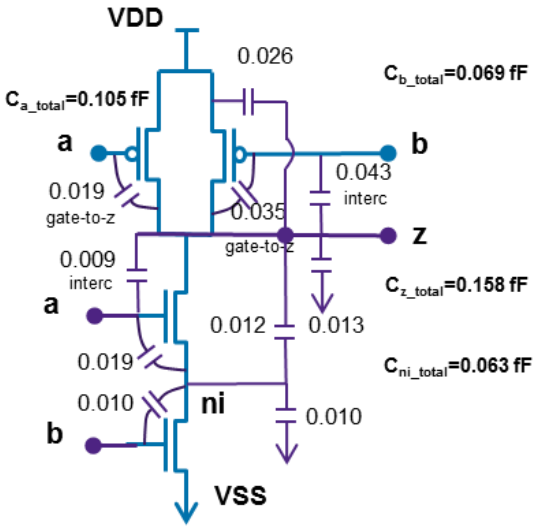


Fig. 10. Parasitic capacitances for design A

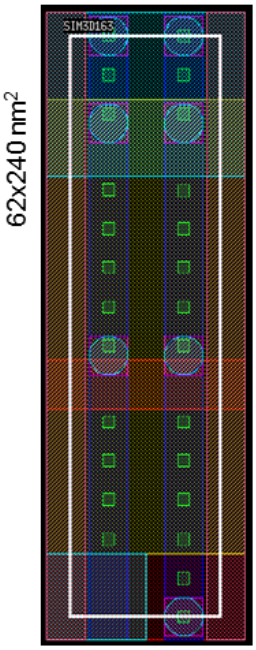


Fig 11. Layout B

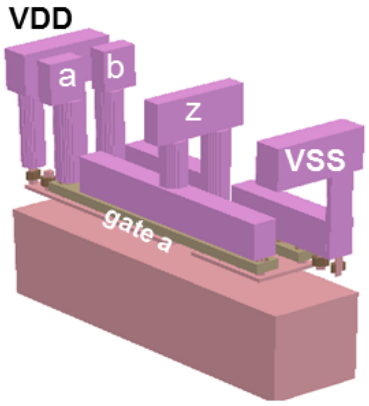


Fig. 12. 3D view of design B

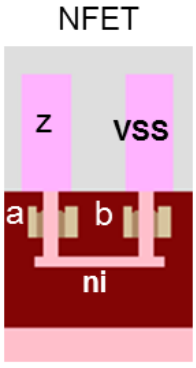


Fig. 13. NFET cross-section of design B

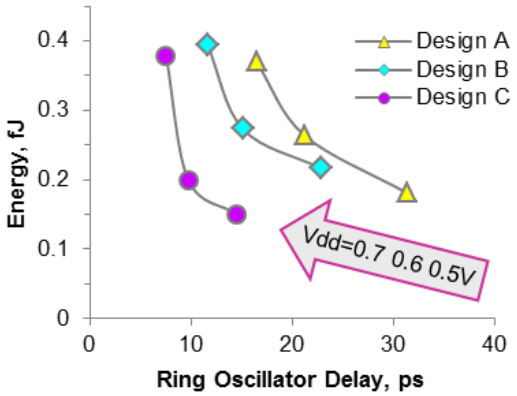


Fig. 14. Benchmarking ring oscillators built on 5nm NW's with different cell design options