Implication of Hysteretic Selector Device on the Biasing Scheme of a Cross-point Memory Array

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***Abstract*—We analyze the effect of hysteresis in the correlated material (CM) based selector devices on the choice of the word-line and bit-line voltages of a cross-point memory array. Considering a magnetic tunnel junction as the memory device, we also evaluate the dependence of array leakage and performance on the CM characteristics. While insulator-to-metal transition (IMT) in the CM plays a pivotal role in determining the voltage biases for proper functionality, we show that metal-to-insulator transition (MIT) also has an important effect on the array power-performance. If MIT switching time is large compared to the set-up time, the read/write speed may be limited by MIT, resulting in performance loss. We show that the performance can be recovered by choosing appropriate voltage biases. We define the region of operation for the voltage biases constrained by MIT to ensure no performance penalty due to metal-to-insulator transition. For the read operation, MIT constrained region of operation leads to minimal or no leakage penalty. Thus, optimal choice of bias voltages for read yields maximum performance and energy efficiency. However, for the write operation, high write voltage shrinks the region of operation, thus offering limited choices for the voltages, leading to leakage increase. The leakage penalty reduces with decreasing hysteresis of the CM. While leakage increase at iso-performance can be as large as 21X for 75mV of hysteresis, it reduces to 2.6X for hysteresis of 28mV. For hysteresis > 100 mV, the MIT constrained region of operation vanishes and the only design choice that remains is increasing the write cycle time.**

Keywords—Cross-point architecture; correlated material; metal-insulator transition; insulator-metal transition; hysteresis; magnetic tunnel junction; array leakage; half-accessed cell

I. INTRODUCTION

Increasing demand for large data storage capacity in stand-alone and embedded memories has led to the exploration of novel high density memory design solutions. The density of memories, in most cases, is governed by the number of transistors in the bit-cell [1]. For standard memory architectures based on non-volatile technologies like MRAMs [2] and resistive memories [2], at least one access transistor is required for robust array-multiplexing [2]. In order to increase the memory density further, cross-point architecture [1] is one of the most widely employed design options. A cross-point architecture eliminates the access transistor, leading to an array of closely-packed memory elements. However, the increase in density comes at the cost of higher array leakage due to sneak current paths in the un-accessed and half accessed cells (UA, HAR and HAC in Fig. 1(a), (b)). In order to mitigate this issue, a highly non-linear selector device is employed in series with a memory element [1] (Fig. 1(a), (b)). The non-linearity of the selector is utilized to minimize the sneak current with an insignificant impact on the read/write performance.

Correlated materials (CM) [3], which exhibit extreme non-linearity due to abrupt current driven metal-to-insulator and insulator-to-metal transitions (MIT and IMT - Fig. 1(c)), can potentially be used as selector devices [1]. However, these materials typically exhibit hysteretic characteristics, which can have a significant effect on the memory operation [1]. *In this paper, we analyze the implications of a hysteretic selector on the choice of the word-line (WL) and bit-line (BL) voltages in a cross-point array. While IMT plays a key role in determining the voltages for proper functionality [1], we discuss the significance of choosing the voltages considering MIT to optimize the performance. Based on this analysis, we define the desired attributes of a CM to enhance its effectiveness as a selector*.

II. SIMULATION SETUP

We model the CM by expressing its current-voltage relationship as a function of the resistivity in the insulating (ρ_{INS}) and metallic phases (ρ_{MET}) and the critical voltages (V_{CIMT}, V_{CMIT})

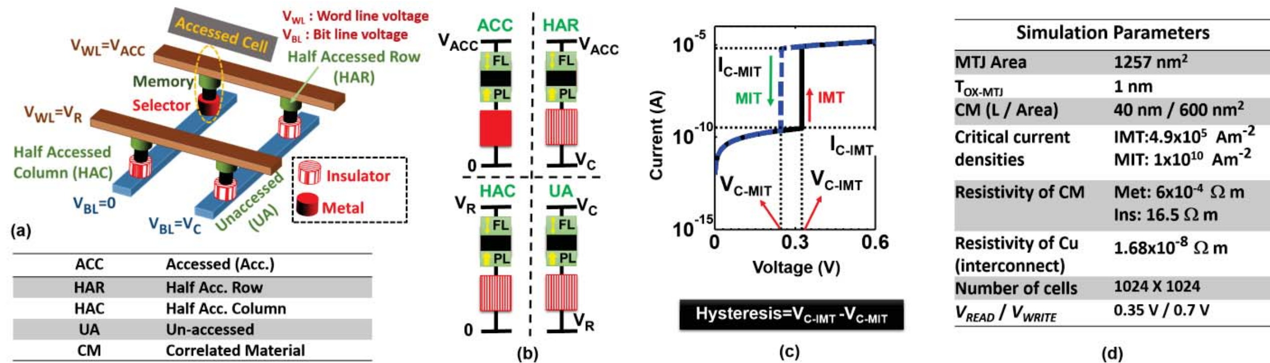

Fig. 1: (a),(b) Cross-point memory array & the voltage bias for accessed, un-accessed and half accessed cells **(c)** I-V characteristics of the correlated material (CM) illustrating critical currents and voltages associated with insulator-to-metal and metal-to-insulator transitions (IMT and MIT, respectively) and the corresponding hysteresis **(d)** simulation parameters.

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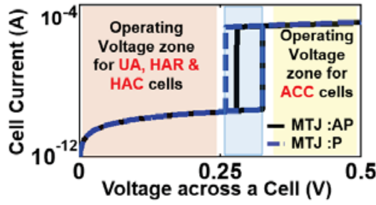


Fig. 2: Current versus voltage characteristics of a single memory cell, showing the operating voltage zone for accessed, half-accessed and unaccessed cells

and currents (I_{CIMT} and I_{CMIT}) that trigger IMT and MIT (Fig. 1(c)). The model assumes a constant resistance in the metallic and insulating phases and triggers the phase transitions by comparing the current through the resistor to a critical value, which depends on the state of the CM. If CM is in the insulating phase, the critical value is equal to I_{CIMT}, otherwise it equals I_{CMIT}. The transition times for IMT and MIT are also accounted for. The hysteresis in the current-voltage characteristics of the CM denotes the difference between the critical voltages of phase transition (V_{CIMT} - V_{CMIT}). This hysteresis translates into 'cell hysteresis' when CM is used in a memory cell. In other words, IMT and MIT trigger points are not the same in the *I-V* characteristics of the cell (i.e. cell current versus voltage across the cell - Fig. 2) due to the hysteretic characteristics of the CM.

For the memory element, we choose a magnetic tunnel junction (MTJ) [4]. MTJs are promising candidates as memory elements because of their non-volatility, compatibility with CMOS process and high integration density [5]. We use a physical model for the MTJ [6] which is governed by the coupled solution of non-equilibrium Green's function and Landau Lifshitz Gilbert Slonczewski (LLGS) equations. We set up a cross-point array simulator framework based on the CM and MTJ models for our analysis. We also capture the effect of interconnect impedance in our framework.

III. Correlated Material Properties and Selection of Bias Voltages

In a cross-point array, appropriate bit-line and word-line voltages need to be applied so that the CM of the accessed cell (ACC) operates in the metallic state while the CMs of the cells in the un-accessed (UA), half accessed row (HAR) and half accessed column (HAC) modes operate in the insulating phase. Hence, the terminal voltages for the cells need to be chosen from the voltage zones illustrated in Fig. 2. This minimizes the sneak current while achieving the desired read/write performance. Moreover, it is critical that the cumulative leakage of the HAC cells is low enough so that the read current through the accessed cell is not masked. To minimize the current in the un-accessed and half-accessed cells, CM exhibiting a large resistivity ratio

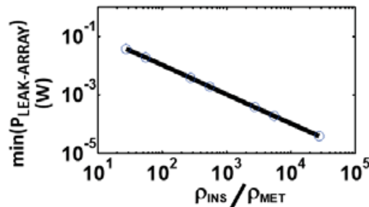


Fig.3: Array leakage ($P_{LEAK\text{-}ARRAY}$) as function of resistivity ratio (ρ_{INS}/ρ_{MET}). The leakage corresponds to the bias voltages that minimizes array leakage.

between the insulating and metallic phases must be used. To limit the array leakage below 50 μW, a resistivity ratio over 10^4 is required (Fig. 3).

The leakage in a half-accessed or unaccessed cell can also be minimized by reducing the voltage drop across it. If we apply V_{ACC} and V_R on the word-line of the access and unaccessed cells, respectively (Fig. 1(a)) and 0 and V_C on the respective bit-lines, then it is easy to deduce that V_C should be as close as V_{ACC} as possible to minimize leakage in HAR cells. On the other hand, V_R needs to be close to 0 to minimize leakage in HAC cells. While it seems possible to satisfy both individually, the unaccessed cells pose a conflict by demanding V_C and V_R to be almost equal. Typically, the last criteria turns out to be the most important since most of the cells operate in the unaccessed mode. (For instance, in an $M \times N$ array, number of unaccessed cells = $M*N+1-M-N$).

In addition to the resistivity ratio, hysteresis in the CM (V_{CIMT} - V_{CMIT}) plays a critical role in ensuring proper operation of the cross-point array. A minimum extent of hysteresis is necessary to handle the voltage snapback across the CM when state transition occurs [2]. However, as we show in this work, a large hysteresis in the *I-V* characteristics of a memory cell (originating form inherent hysteretic CM) may reduce the choice of the bias voltages. In order to explain this, we define the regions of operation for V_R and V_C for proper functionality as well as considering the leakage-performance trade-off.

A. Insulator-to-metal transition constrained region of operation for proper functionality

For proper operation of the memory array, the CM in the accessed cell should transition into the low resistive (metallic) state as the voltage across the cell is increased. At the same time, IMT must be avoided in all other types of cells (HAC, HAR, UA). This necessitates terminal voltages across HAC, HAR and UA cells to be sufficiently low to avoid a voltage greater than V_{CIMT} across the CM. This is achievable when the voltage across HAC (V_R) and HAR (V_{ACC}-V_C) are less than a critical value (V_{HA_CRIT}), which is a function of V_{CIMT}. In other words, $V_R < V_{HA_CRIT}$ (=V_{R_CRIT1} in Fig. 4(a)) and $V_C > V_{ACC}-V_{HA_CRIT}$ (=V_{C_CRIT1} in Fig. 4(a)). In addition, voltage across UA cell, ($|V_R-V_C|) < V_{HA_CRIT}$, which defines the region of operation in the V_C-V_R plane (Fig. 4(a)). Accounting for all these constraints, a common region of operation (RO) can be derived (Fig. 4(a)). Similarly, RO for proper write functionality can be derived (Fig. 4(b)). Read stability necessitates a lower read voltage across the accessed cell compared to the write voltage [5]. Because of this asymmetry in the access bias (V_{ACC}) for read and write, corresponding ROs are different. The choice of biasing is scarcer (smaller RO) for write operation since with higher V_{ACC}, it is more difficult to prevent IMT in half accessed and unaccessed cells.

B. Metal-to-insulator transition constrained region of operation for optimal performance

Operation within IMT constrained RO ensures proper functionality. However, MIT plays a crucial role in array performance especially when MIT switching time is larger than

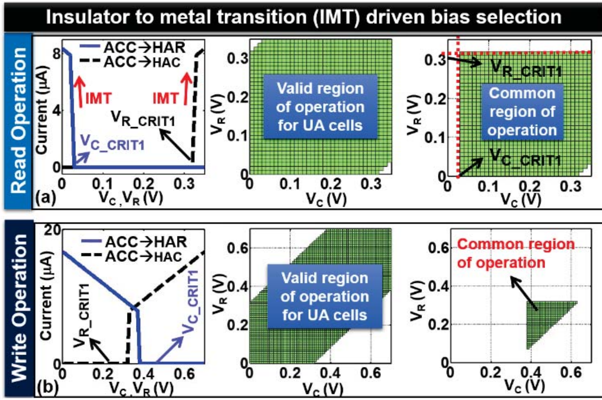


Fig. 4: IMT constrained region of operation (RO) showing the range of V_C and V_R for which CM operates in the insulating state for half accessed and unaccessed cells during (a) read and (b) write. Common region is also shown.

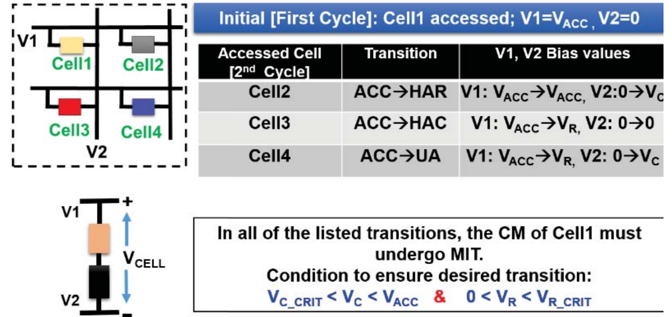
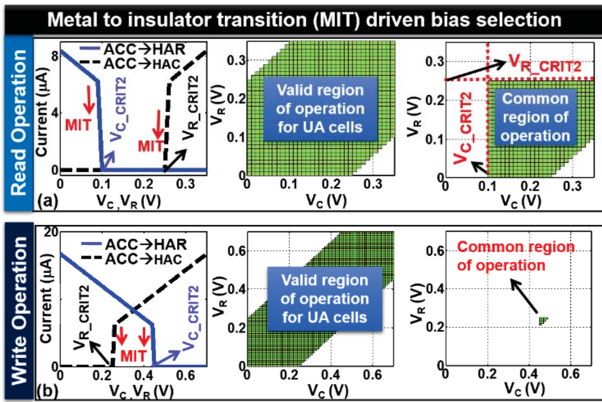


Fig. 5: Illustration of possible transitions for cell 1 (accessed during the first cycle) and the conditions for proper operation.



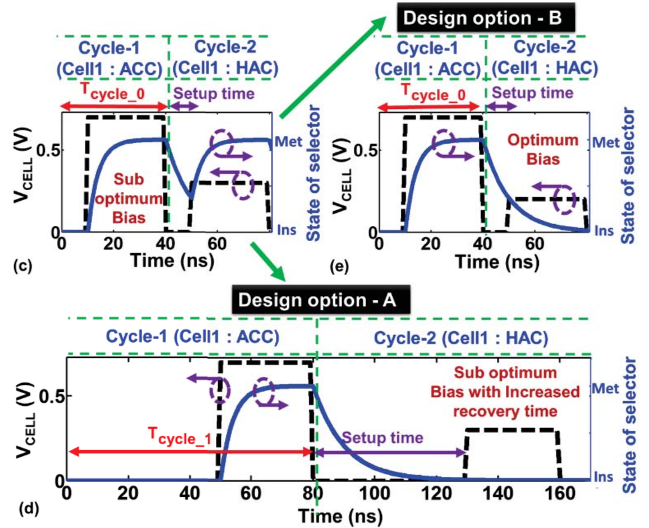


Fig. 6: MIT constrained region of operation (RO) showing the range of V_C and V_R for which CM transitions into the insulating state during (a) read and (b) write. Common region is also shown. Waveforms alongside illustrate the cases when CM of cell 1 (c) fail to undergo MIT in cycle 2 (d) undergoes MIT due to increase in the cycle time (T_{cycle}) and (e) undergoes MIT due to proper choice of bias voltages.

the setup time (determined by the delay of the peripheral circuits). This is critical in CMs in which MIT switching time is typically much larger than IMT switching time [3].

To put the things into perspective, let us consider the following scenario (Fig. 5). Cell 1 is accessed in cycle 1 and in the next cycle, cell 3 is accessed. Thus, in cycle 2, cell 1 switches to the HAC mode. Fig. 6(c) shows that even with voltages chosen from IMT constrained RO, the CM may fail to transition in the insulating state. This occurs if the metal-to-insulator transition time is larger than the setup time. Therefore, the CM gets stuck in metallic state in between consecutive transitions. This problem can be dealt with using two approaches: (A) increasing the setup time and thereby allowing the CM to complete MIT (Fig. 6(d)) and (B) choosing bias voltages from an MIT constrained RO (described subsequently). The first approach sacrifices performance and MIT acts as the bottleneck. On the contrary, the second approach makes the performance independent of metal-to-insulator transition time. In a similar manner, MIT needs to be ensured if cell 1 transitions from ACC to HAR and UA modes. The former scenario will occur if cell 2 is accessed in cycle 2 while the latter case corresponds to the access of cell 4 in cycle 2, as illustrated in Fig. 5.

The derivation of MIT constrained RO (Fig. 6 (a-b)) is similar in principle to the IMT constrained RO, described earlier. But in this case, the critical constraints are defined by V_{CMIT}. Since $V_{CMIT} < V_{CIMT}$ (hysteresis > 0), the choice of bias for each type of cells is less and the ROs for both read (Fig. 6 (a)) and write (Fig. 6(b)) are smaller than the respective IMT constrained ROs. Note that the reduction in RO for write is much more compared to read. This is due to the fact that the write voltage (V_{ACC}) is larger than read voltage (V_{ACC}), as discussed previously. Choosing bias voltage from the MIT constrained RO results in proper state switching of the CM without the need to increase the setup time and therefore no performance penalty is incurred (Fig. 6(e)). However, reduced choices for V_R and V_C may lead to leakage increase, which is discussed next.

IV. Leakage Analysis and Dependence on Hysteresis

During read, the choice of V_C and V_R is governed by (i) the array leakage (Fig. 7) and (ii) the total leakage in the HAC cells

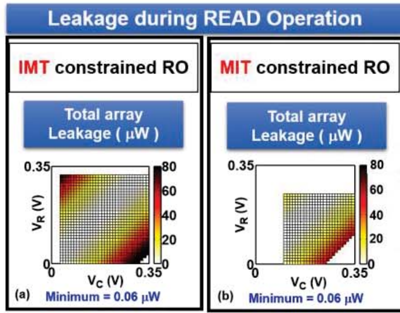


Fig. 7: Array leakage power during read calculated within (a) IMT constrained RO and (b) MIT constrained RO

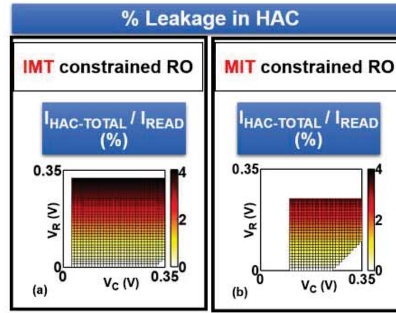


Fig. 8: Leakage of HAC cells ($I_{HAC-TOTAL}$) in comparison to the read current (I_{READ}) within (a) IMT constrained RO and (b) MIT constrained RO.

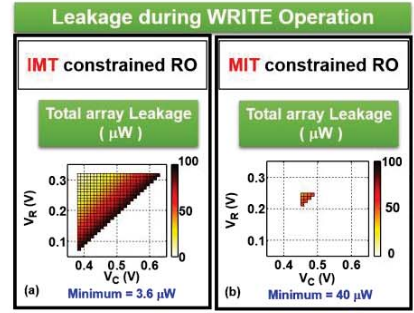


Fig. 9: Array leakage power during write considering (a) IMT constrained RO and (b) MIT constrained RO.

($I_{HAC-TOTAL}$)) (Fig. 8). The latter must be significantly less than read current of the accessed cell (I_{READ}) so that the information in I_{READ} is not sullied by I_{HAC_TOTAL}. Note that for the read operation, MIT constrained RO is sufficiently large (Figs. 7, 8) to contain the optimum voltage choices (within the range of hysteresis shown in Fig. 10(c)) and hence the minimum leakage obtained within IMT and MIT constrained ROs are same (0.06 μW) for optimal bias, $V_C = V_R = 0.17$V. Within both of the ROs, leakage current through the HAC cell is less than 3% of the read current through an accessed cell (Fig. 8), which ensures sufficient read sensitivity. Since there is no leakage penalty during read, leakage and performance during read can be optimized by considering the voltage biases constrained by MIT.

During write, V_C and V_R need to be chosen from within the region of operation to minimize the total array leakage (Fig. 9). For write, the MIT constrained RO is much smaller than the IMT constrained RO, as discussed in the previous section. Hence, the optimal bias points for IMT constrained RO ($V_C = 0.38$V, $V_R = 0.32$V) may not fall within the MIT constrained RO, leading to increase in leakage (Fig. 9). With reduced hysteresis, V_{CMIT} approaches V_{CIMT}; hence RO increases and leakage penalty reduces (Fig. 10(a), (b)). This is because, larger region of operation provides more choices for V_C and V_R for leakage minimization. The decrease in leakage with reducing hysteresis is shown in Fig. 10. It can also be observed in Fig. 10 that if hysteresis in CM exceeds 100mV, design option-A (Fig. 6(d)) becomes the only choice for write operation, since the MIT constrained RO vanishes.

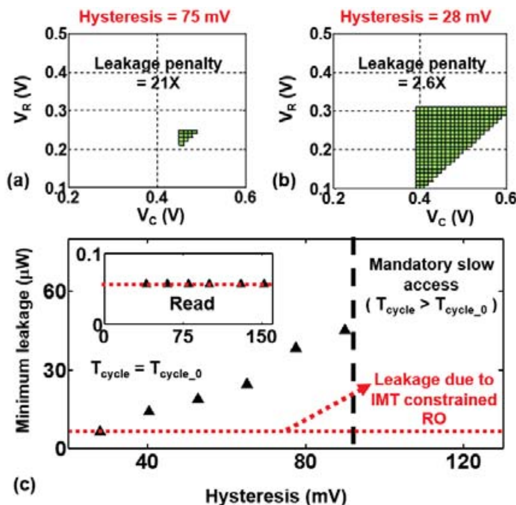


Fig. 10: (a), (b) MIT constrained region of operation for write for different hysteresis in CM. Lower hysteresis yields less leakage penalty with respect to the case when RO is constrained by IMT (c) Dependence of the minimum array leakage (at optimal bias voltages) on the hysteresis of the CM for write operation. For hysteresis > 100 mV, RO vanishes and increasing the cycle time is the only design option. Inset shows leakage versus hysteresis for read, showing no leakage increase.

V. CONCLUSION

The hysteretic behavior of the CM has an important effect on the biasing scheme of a cross-point architecture and defines a region of operation for the bias voltages (V_C and V_R). Outside this region, the accessed cell fails to transition into the un-accessed or half accessed modes properly if the metal-to-insulator transition time is larger than the setup time, resulting in performance penalty. To avoid the increase in the read/write cycle time, the choice of bias voltages need to consider MIT. This results in an increase in leakage for write but no leakage penalty for read. The leakage penalty reduces with decreasing hysteresis. Hence, CM based selector device in the cross-point array necessitates the choice of proper materials which have (a) high ratio between the resistivity of the insulating and metallic phases (for leakage minimization) (b) lower hysteresis (for a larger choice of voltage biases) and (c) low time constants associated with IMT and MIT.

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