TCAD Analysis of FinFET Stress Engineering for CMOS Technology Scaling

Amaury Gendron-Hansen[1], Konstantin Korablev[2], Ivan Chakarov[2], James Egley[1], Jin Cho[1], and Francis Benistant[3]

[1]GLOBALFOUNDRIES, 2600 Great America Way, Santa Clara, CA 95054, USA
[2]GLOBALFOUNDRIES, 400 Stone Break Extension, Malta, NY 12020, USA
[3]GLOBALFOUNDRIES, 60 Woodlands Industrial Park D, Street 2, Singapore 738406, Singapore
Email: Amaury.Gendron-Hansen@globalfoundries.com

***Abstract*— In this paper, we analyze the mechanical stress induced from source/drain embedded SiGe (eSiGe) in multiple generations of FinFET technologies. By leveraging TCAD simulations, we show that high stress over the entire fin height could be achieved with a proper design of the eSiGe cavity. We also find that the stress should not undergo any reduction as the industry continues to scale down CMOS technologies. Hence, it should still play a major role in boosting semiconductor device performance for the next generation of FinFETs.**

***Keywords*— Advanced CMOS technology, FinFET, mechanical stress, TCAD.**

I. Introduction

Over the past decade, the semiconductor industry has relied heavily on mechanical stress to boost MOSFET drive current with technology scaling [1], [2]. PFET performances were highly improved by uniaxial stress induced from eSiGe in the source and drain [3]. However, the transition from planar devices to FinFET and the reduction of the source/drain dimensions have raised some concerns about eSiGe effectiveness for upcoming technology nodes [4], [5], [6], [7].

In this paper, we present an in-depth analysis of the stress 3D distribution in bulk FinFET and its evolution with the technology scaling. This study is based on TCAD simulations of the lattice mismatch performed with Synopsys Sentaurus tools. We focus on the effects of both the new eSiGe shapes and the reduction of FinFET dimensions.

II. FinFET Process

Advanced FinFETs (Fig. 1) incorporate features from the latest planar technologies, such as high-k dielectric and replacement metal gate (RMG). RMG advantages include low equivalent oxide thickness (EOT), flexibility for work-function tuning, and stress enhancement during the poly gate removal [8]. The eSiGe is deposited by epitaxial growth after recessing the fin in the source/drain area. Diamond-shaped epitaxy allows process control and reduction of contact resistance by leveraging the slow growth along (111) crystallographic planes.

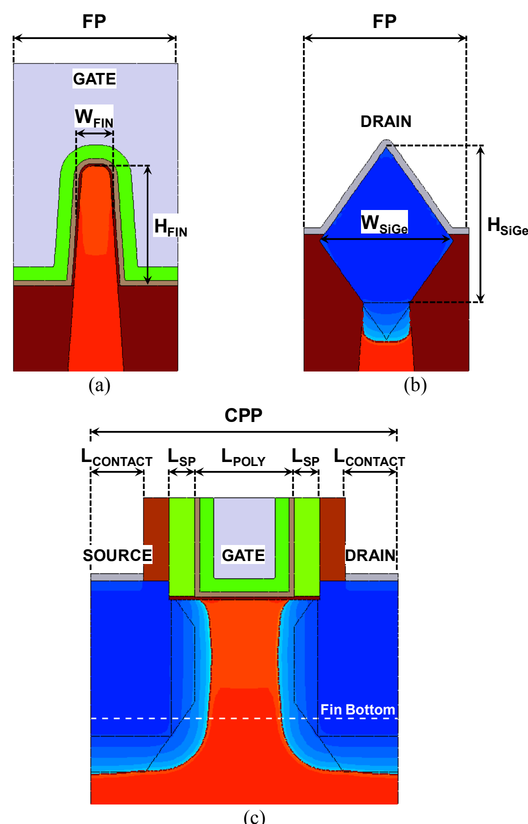


Fig. 1. FinFET cross-sections in the middle of the gate (a), through source/drain epitaxy (b), and along the channel from source to drain (c).

III. Source/Drain Cavity

Continuous stress enhancements in planar technologies led to sigma-shaped eSiGe cavities with a tip extending under the spacer to minimize the tip-to-tip distance between source and drain [9]. However, this geometry cannot be directly transferred to FinFET, and it must be optimized to achieve high stress over the entire fin height. In this paper, we compare three different cavities: U-shaped, sigma, and super sigma (Fig. 2). A U-shaped cavity can be patterned with an anisotropic etch such as a reactive ion etch (RIE), whereas preferential crystallographic directions are required for sigma and super sigma cavities. Sigma and super sigma cavities differ mainly in the shape of the tip under the spacer; the prior

978-1-4673-7860-4/15/$31.00 ©2015 IEEE

has a flat surface, and the latter is characterized by two slanted surfaces forming a sharp edge. Thus, the super sigma tip can extend in the channel while preserving the gate integrity. In all cases, the eSiGe germanium mole fraction is equal to 55%, with a 25% buffer to prevent the formation of defects.

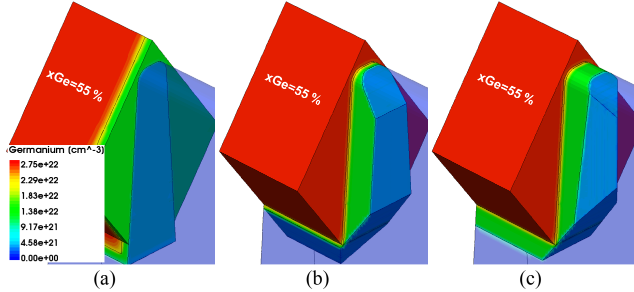
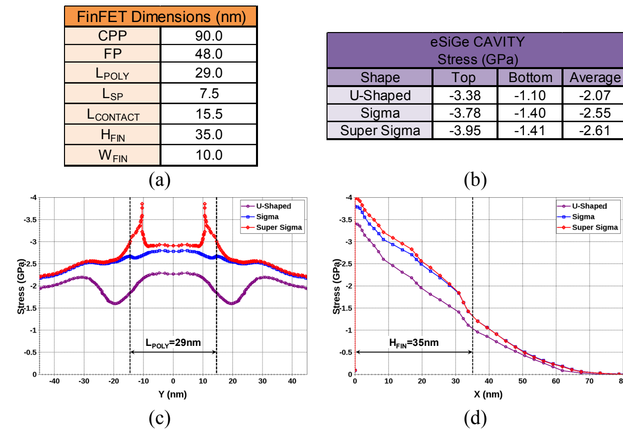


Fig. 2. U-shaped (a), sigma (b), and super sigma (c) eSiGe cavities (transparent silicon outside eSiGe and no insulator layers).

The lattice mismatch between SiGe and silicon induces a uniaxial compressive stress in the gate length direction, boosting holes mobility [10]. Simulation results (Fig. 3) show the highest stress is obtained with the super sigma cavity. Compared to the sigma cavity, the improvement is relatively small, with only a 2% increase of the average stress in the fin. Compared to the U-shaped cavity, by contrast, the increase reaches 23%. These differences in stress come from the effects of different SiGe volumes and tip to tip distances.



FinFET Dimensions (nm)	
CPP	90.0
FP	48.0
L_{POLY}	29.0
L_{SP}	7.5
$L_{CONTACT}$	15.5
H_{FIN}	35.0
W_{FIN}	10.0

(a)

	eSiGe CAVITY Stress (GPa)		
Shape	Top	Bottom	Average
U-Shaped	-3.38	-1.10	-2.07
Sigma	-3.78	-1.40	-2.55
Super Sigma	-3.95	-1.41	-2.61

(b)

Fig. 3. FinFET dimensions (a), stress extraction in the fin (b), lateral stress profile from source to drain at mid-fin height (c), and vertical stress profile in the middle of the channel (d).

Importantly, the lateral stress profiles (Fig. 3 c) do not have the same shapes for the three cavities. The super sigma reaches two maxima near the gate edges, whereas the sigma remains almost flat and the U-shaped drops. For advanced CMOS technologies with a high fraction of ballistic current, the stress maximum near the source junction brings extra benefits by enhancing the injection velocity [11].

The vertical profiles (Fig. 3 d) show a stress reduction from the top to the bottom of the fin. The stress decreases by 67%, 63%, and 64% for the U-shaped, sigma, and super sigma cavities, respectively. Variations along the fin height are unavoidable with eSiGe stressors. The lattice constant at the bottom of the eSiGe is set by the silicon substrate; thus, the lattice mismatch with the silicon fin is small. The mismatch increases only as the eSiGe relaxes away from the substrate. This effect is reinforced by the stress rebalancing during a RMG process. After the dummy poly removal, the top of the fin is prone to deformation, allowing a high stress transfer from the eSiGe (Fig. 4).

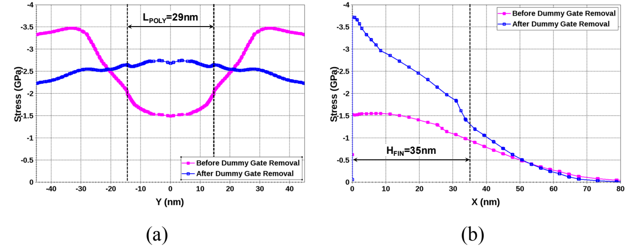


Fig. 4. Lateral (a) and vertical (b) stress profiles for sigma cavity FinFET before and after polysilicon removal.

IV. Dimensions Scaling

We performed TCAD simulations to understand how the technology scaling affects the stress in a FinFET, varying only one FinFET dimension at a time. The trends were not expected to depend strongly on the cavity geometry, so the analysis was limited to the sigma cavity. For these simulations, we kept diamond-shaped eSiGe even if the epitaxy would merge, and the eSiGe cavity tip proximity to the channel stayed constant. Lattice mismatch and defect formation between two adjacent merged eSiGe are outside the scope of this study.

First, we consider the dimensions along the device length (Fig. 5). The contacted polysilicon pitch CPP variations correspond to eSiGe volume variations, the fin dimensions remaining constant. The stress tends to saturate at high CPP but decreases sharply in the range suitable for advanced CMOS technologies (below 100 nm). However, the gate length L_{POLY} and spacer length L_{SP} scaling reduce the fin volume, allowing the stress to increase.

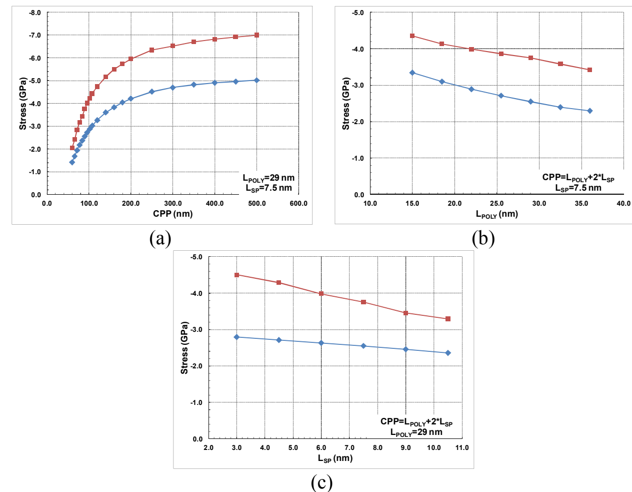
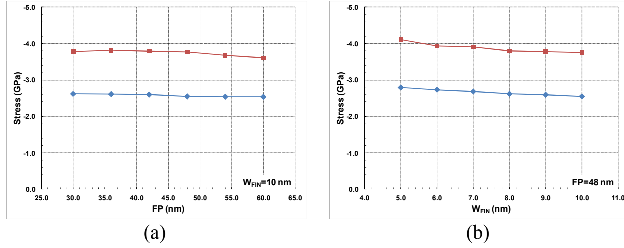


Fig. 5. Stress at the top of the fin (red squares) and average stress in the fin (blue sigmas) for CPP (a), L_{POLY} (b), and L_{SP} (c) variations.

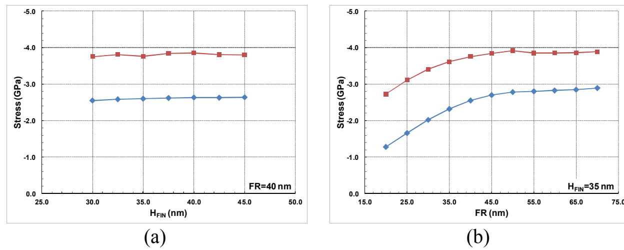
Along the device width (Fig. 6), the effect of the fin pitch FP is negligible. Even the transition from unmerged to merged epitaxies (at approximately 40 nm) does not affect the stress. As the fins become narrower to keep the short channel effects under control, we expect some stress gain from the fin volume reduction.



(a) (b)

Fig. 6. Stress at the top of the fin (red squares) and average stress in the fin (blue sigmas) for FP (a) and the fin width W_{FIN} (b) variations.

FinFET technology scaling might lead to taller fins to increase the current per footprint. However, as shown in Fig. 7, both the stress at the top of the fin and the average stress are fairly insensitive to the fin height H_{FIN}. In contrast, the fin recess FR before the eSiGe epitaxy is an important knob for stress optimization. The highest stress values are achieved for a recess at least 10 nm below the bottom of the fin.



(a) (b)

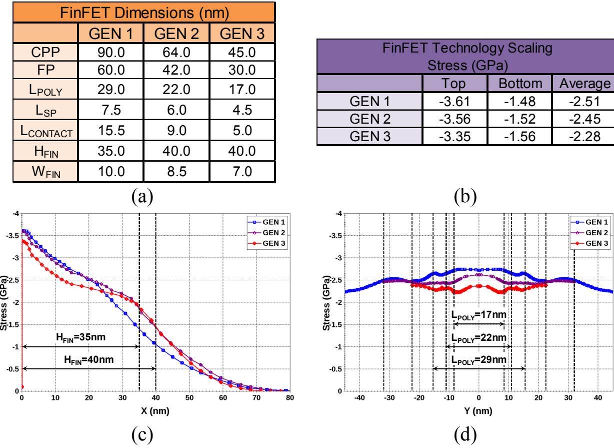
Fig. 7. Stress at the top of the fin (red squares) and average stress in the fin (blue sigmas) for H_{FIN} (a) and the FR (b) variations.

To get the overall effects, we performed simulations for three FinFET generations (Fig. 8). The results show a moderate stress reduction with the technology scaling. The average values decrease by 2% from generation 1 to generation 2 and by 7% from generation 2 to generation 3. To compensate this reduction and achieve the same stress levels in all three generations, the eSiGe germanium content needs only to increase from 55% to 57% in generation 2 and to 62% in generation 3.

To gain additional insight into the impact of technology scaling, the dimensions were adjusted along either the device length (CPP, L_{POLY}, and L_{SP}) or the device width (FP and W_{FIN}) (Fig. 9). Along the device length, L_{POLY} and L_{SP} reduction do not compensate for the stress degradation at smaller CPP because L_{POLY} is not scaled as aggressively as CPP to mitigate short channel effects. Along the device width, the scaling tends to increase the stress, as expected from its dependence with the fin width.

V. Conclusion

A thorough analysis of the mechanical stress distribution in FinFET was performed by leveraging TCAD simulations. We found that effective stressors can be designed if the fin etch before eSiGe epitaxy is properly optimized. And, as CMOS technologies continue to be scaled, an increase in the eSiGe germanium content by only a few percent is sufficient to keep the stress level constant. Therefore, we expect eSiGe stress engineering to remain critical in optimizing FinFET performance.



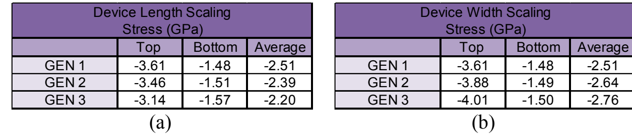
FinFET Dimensions (nm)			
	GEN 1	GEN 2	GEN 3
CPP	90.0	64.0	45.0
FP	60.0	42.0	30.0
L_{POLY}	29.0	22.0	17.0
L_{SP}	7.5	6.0	4.5
$L_{CONTACT}$	15.5	9.0	5.0
H_{FIN}	35.0	40.0	40.0
W_{FIN}	10.0	8.5	7.0

FinFET Technology Scaling Stress (GPa)			
	Top	Bottom	Average
GEN 1	-3.61	-1.48	-2.51
GEN 2	-3.56	-1.52	-2.45
GEN 3	-3.35	-1.56	-2.28

(a) (b)

(c) (d)

Fig. 8. Dimensions for three FinFET generations (a), stress extraction in the fin (b), lateral stress profile at mid-fin height (c), and vertical stress profile in the middle of the channel (d). Generations 1, 2, and 3 corresponds to GEN1, GEN2, and GEN3, respectively.



Device Length Scaling Stress (GPa)			
	Top	Bottom	Average
GEN 1	-3.61	-1.48	-2.51
GEN 2	-3.46	-1.51	-2.39
GEN 3	-3.14	-1.57	-2.20

Device Width Scaling Stress (GPa)			
	Top	Bottom	Average
GEN 1	-3.61	-1.48	-2.51
GEN 2	-3.88	-1.49	-2.64
GEN 3	-4.01	-1.50	-2.76

(a) (b)

Fig. 9. Stress extraction for scaling along the device length (a) and width (b). Generations 1, 2, and 3 corresponds to GEN1, GEN2, and GEN3, respectively.

References

[1] K.J. Khun, "Considerations for Ultimate CMOS Scaling," IEEE Tans. Electron Devices, vol. 59, no. 7, pp. 1813-1828, July 2012.

[2] S. Natarajan, M. Agostinelli, S. Akbar, M. Bost, et. al., "A 14nm Logic Technology Featuring 2nd-Generation FinFET Transistors, Air-Gapped Interconnects, Self-Aligned Double Patterning and a 0.0588µm^2 SRAM Cell Size," in IEDM Tech. Dig., pp. 71-73, Dec. 2014.

[3] S.E. Thompson, M. Armstrong, C. Auth, M. Alavi, et. al., "A 90-nm Logic Technology Featuring Strained-Silicon," IEEE Tans. Electron Devices, vol. 51, no. 11, pp. 1790-1797, Nov. 2004.

[4] S. Maeda, Y. Ko, J. Jeong, H. Fukutome, et. al., "3 Dimensional Scaling Extensibility on Epitaxial Source Drain Strain Technology Toward Fin FET and Beyond," in VLSI Tech. Dig., pp. 88-89, June 2013.

[5] C. Auth, C. Allen, A. Blattner, D. Bergstrom, et. al., "A 22 nm High Performance and Low-Power CMOS Technology Featuring Fully-Depleted Tri-Gate Transistors, Self-Aligned Contacts and High Density MIM Capacitors," in VLSI Tech. Dig., pp. 131-132, June 2012.

[6] A. Keshavarzi, D. Somasekhar, M. Rashed, S. Ahmed, et. al., "Architecting Advanced Technologies for 14nm and Beyond with 3D FinFET Transistors for the Future SoC Applications," in IEDM Tech. Dig., pp. 67-70, Dec. 2011.

[7] A. Nainani, S. Gupta, V. Moroz, M. Choi, et. al., "Is strain engineering scalable in FinFET era? : teaching the old dog some new tricks," in IEDM Tech. Dig., pp. 427-430, Dec. 2013.

[8] J. Wang, Y. Tateshita, S. Yamakawa, K. Nagano, et. al., "Novel Channel-Stress Enhancement Technology with eSiGe S/D and Recessed Channel on Damascene Gate Process," in VLSI Tech. Dig., pp. 46-47, June 2007.

[9] K. Mistry, C. Allen, C. Auth, B. Beattie, et. al., "A 45nm Logic Technology with High-k+Metal Gate Transistors, Strained Silicon, 9 Cu Interconnect Layers, 193nm Dry Patterning, and 100% Pb-free Packaging," in IEDM Tech. Dig., pp. 247-250, Dec. 2007.
[10] P. Packan, S. Cea, H. Deshpande, T. Ghani, et. al., "High Performance Hi-K + Metal Gate Strain Enhanced Transistors on (110) Silicon," in IEDM Tech. Dig., pp. 1-4, Dec. 2008.
[11] L. Lucci, P. Palestri, D. Esseni, L. Bergagnini, et. al., "Multisubband Monte Carlo Study of Transport, Quantization, and Electron-Gas Degeneration in Ultrathin SOI n-MOSFETs," IEEE Tans. Electron Devices, vol. 54, no. 5, pp. 1156-1164, May 2007.