Integrated Modeling Platform for High-k/Alternate Channel Material Heterostructure Stacks

Dhirendra Vaidya, Arjun Hegde, Saurabh Lodha, Swaroop Ganguly
Electrical Engineering Department
Indian Institute of Technology Bombay
Mumbai, India
swaroop.ganguly@gmail.com

Aneesh Nainani, Naomi Yoshida, Theresa Guarini
Applied Materials Inc.
Santa Clara, CA, USA

***Abstract*—To study the High-k dielectrics on alternate semiconductor materials for transistors a modeling platform has been developed which implements a faster 1D Schrodinger-Poisson along with trap models. A fitting algorithm is used for the extraction of trap profiles which fits the model capacitance/admittance to the measurements in the least square sense. The extraction is illustrated on a subnanometer EOT HfO_2/SiGe/Si heterostructure stack.**

Keywords—heterostructures; gate stacks; interface traps

I. Introduction

With advances in epitaxial growth and high-k dielectric deposition technics, combinations of alternate channel material and high-k dielectric have emerged as plausible options for next-generation logic transistors. However such a combination can only be adopted if the high-k/alternate channel semiconductor interface quality is excellent, i.e. comparable to the best Si/SiO_2 interface. Capacitance (and conductance) measurements on metal-oxide-semiconductor (MOS) capacitors are ubiquitously used for quick and economical evaluation of the high-k/alternate channel semiconductor interface. However, the extraction of interface state density over the entire bandgap from MOS capacitor measurements still remains a challenge. We have developed an integrated simulation platform to aid the characterization of high-k/alternate channel semiconductor interfaces. An efficient self-consistent Schrödinger-Poisson solver yields the band bending, carrier densities and the (ideal) capacitance-voltage (C-V) characteristics of these complex stacks; equivalent circuit based trap models are then used to study their frequency dispersion. Finally, a novel interface trap extraction methodology has been developed and illustrated on ultrathin effective oxide thickness (EOT) MOS capacitors.

II. Ideal CV of Heterostructure stacks

The implementation of the simulator follows Wang et al.[1] and makes use of Accelerated Anderson Mixing for faster convergence. The Poisson-only C-V simulations, performed using a Newton-Raphson loop, are expectedly the fastest (see Table 1). The unavailability of an exact Jacobian in the Schrodinger-Poisson case necessitates Accelerated Anderson Mixing to reduce the number of iterations. Table 1 provides the timing information of the solver on Intel® Xeon® 2.6GHz processor.

In the SiGe channel gate stacks where a thin layer of SiGe is epitaxially grown, a built in potential is developed across the isotype SiGe/Si heterojunction. This built in potential is evaluated by applying the Neumann boundary conditions, i.e. making external electric field zero at the device boundaries. This allows the semiconductor side of the capacitor to be charge neutral; we have defined this as the flat-band condition. When the metal-Si work function difference is zero, this condition appears at zero gate voltage.

TABLE I. Timing considerations of the simulator

	Poisson only	Schrodinger Poisson
Iterations at flat-band	3-4	11
Iterations at accumulation	4-5	22
Time per iteration (sec)	0.022	0.33-0.41

III. Interface Trap Extraction

We adopt the interface trap model from Nicollian and Brews [2] and the border trap model of Yuan et al. [3]. Though our platform incorporates the border trap model, it is not discussed in the rest of this paper since the SiGe/Si MOS capacitor data that we have modeled here does not seem to require it.

Interface state density is the critical parameter in the evaluation of the dielectric/semiconductor interface quality, and the capture cross section is an important auxiliary parameter in its extraction. Both these parameters are material and process dependent and may be extracted from MOS capacitor characterization. Temperature-dependent admittance measurements, proposed by Martens et al. [4] are slow and require specialized characterization equipment. In our methodology we try to illustrate extraction over the entire semiconductor bandgap at room temperature.

978-1-4673-7860-4/15/$31.00 ©2015 IEEE

Figure 1 summarizes our interface trap density extraction methodology. The ideal high frequency C-V (HFCV) is first calculated by turning off the minority carrier response completely – this is achieved by modifying the Schrodinger-Poisson loop. The ideal HFCV is matched to the maximum and minimum capacitance measured at the highest frequencies (> 1MHz) through tuning of the high-k and interlayer (IL) thickness and permittivity, and doping densities in the semiconductor layers. The material parameters for SiGe are taken from Sant et al. [5].

Next, the band-bending and carrier densities are obtained by mapping high-frequency (1MHz) CV to the ideal HFCV; these will give identical capacitance for the same band-bending since the traps in the former only result in a dc stretch-out, with no contribution to the ac capacitance. This assumes that the 1MHz C-V is free of ac trap response; if not, this would be one of the sources of errors in the extraction of interface state density and capture cross section (to be discussed in detail later).

The interface states density and capture cross section are parameterized as:

$$D_{it} = D_{it0} + \sum A_i^{D_{it}} \exp(-(E - m_i^{D_{it}})^2 / C_i^{D_{it}})$$

$$\sigma_{maj} = \sigma_0 + \exp(-\alpha E/kT) \text{ or}$$

$$\sigma_{maj} = \sigma_0 + \sum A_i^{\sigma_{maj}} \exp(-(E - m_i^{\sigma_{maj}})^2 / C_i^{\sigma_{maj}})$$

where $A_i^{D_{it},\sigma}, m_i^{D_{it},\sigma}, C_i^{D_{it},\sigma}, D_{it0}, \alpha, \sigma_0$ are fitting parameters.

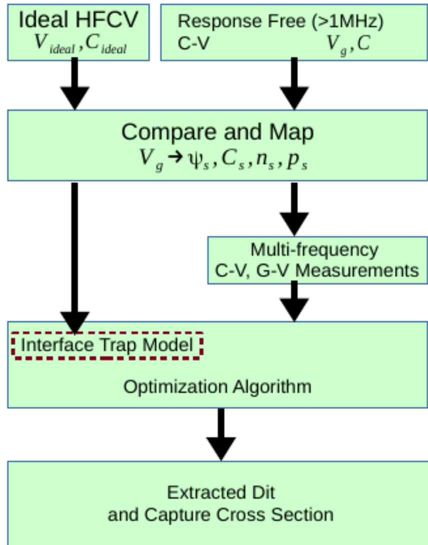

Fig. 1. Interface trap extraction methodology

The number of Gaussians used for fitting may be varied if required. We find that multiple Gaussians are adequate to parameterize any arbitrary profile for interface state density and capture cross section, though the exponential profile may be convenient in some cases for the capture cross section. We have obtained the $D_{it}(E)$ and $\sigma(E)$ profiles from least squares fitting to the admittance data - or possibly to capacitance (conductance) data alone, referred to later in this paper as 'capacitance-only' ('conductance-only') fitting.

IV. Results and Discussion

Fig. 2(a) shows the ideal HFCV compared with capacitance measurements. For multi-frequency C-V we did observe some dispersion in the accumulation; this suggests a series resistance contribution, which we corrected for. The capacitor stack comprises: HfO_2/SiO_2 (High-k/IL dielectric) on $Si_{0.55}Ge_{0.45}/Si$ with a Si cap near the IL-SiGe interface. The non-saturating behaviour observed in accumulation for MOS capacitors with very thin insulators is captured by our Schrodinger-Poisson simulator. As mentioned earlier the tuning of parameters suggest that $\epsilon_{IL} = 5.7$ instead of the 3.9 expected for SiO_2 and this may be attributed to the formation of some hafnium silicate. Fig. 2(b) shows, for comparison, an InGaAs MOSCAP CV matched to the simulated CV reported by Yuan et al. [3]. As non-parabolicity was not included in the Schrodinger-Poisson, the EOT was estimated to be 3nm rather than reported value of 3.3nm. However, the simulation platform can be extended at present to carry out C-V modelling and extraction of interface traps on III-V heterostructure MOS capacitors.

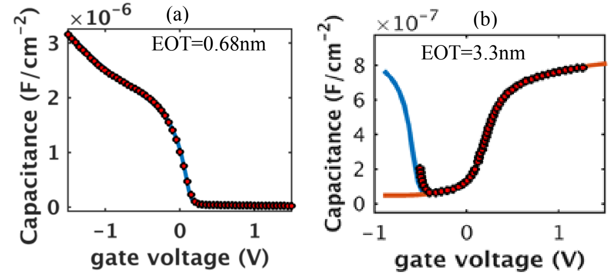

Fig. 2(a). Ideal HFCV (solid blue) simulation of SiGe/Si MOSCAP with 1.75nm Si cap, correctly modeling the non-saturating behavior of capacitance in accumulation, as seen from 1MHz CV data (circles). (b). Ideal LFCV (solid blue) and HFCV (solid red) of InGaAs MOSCAP, compared against reported simulation data (circles) [3].

We now illustrate the extraction of interface states for a multi-layered gate stack on a SiGe/Si MOS capacitor shown in Fig. 3(a). The parameters for the SiGe layer are obtained from Sant et al. [5] and from Rieger and Vogl [6]. The Ge content in SiGe is known a priori to be 30%; its doping of $10^{18} cm^{-3}$ and that of the Si substrate – a moderate level of $1.15 \times 10^{16} cm^{-3}$ – are obtained from the minimum capacitance. The measured C-V and G-V characteristics are shown in Fig. 3(b) and 3(c) respectively. Significant frequency dispersion is observed in the depletion region of the C-V and smaller but substantial frequency dispersion is also seen in the accumulation C-V. It may be noted that 1MHz C-V exhibits an anomalous behavior. For accumulation bias more negative than -0.15V, the capacitance at 1MHz is seen to be slightly larger than that at smaller frequency. This behavior cannot be explained by the series resistance or border traps and needs further investigation.

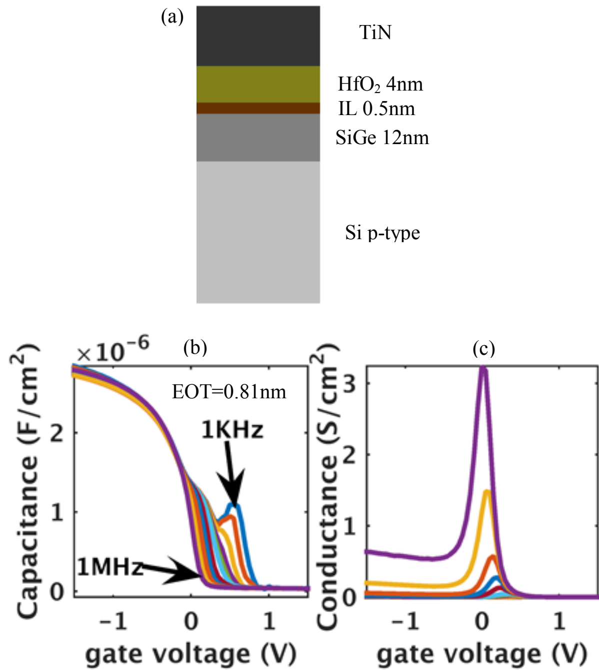

Fig. 3 (a). MOS capacitor stack, SiGe layer contains 30% Ge. (b). Measured CV showing larger frequency dispersion in the depletion and smaller frequency dispersion in accumulation (c). Measured GV.

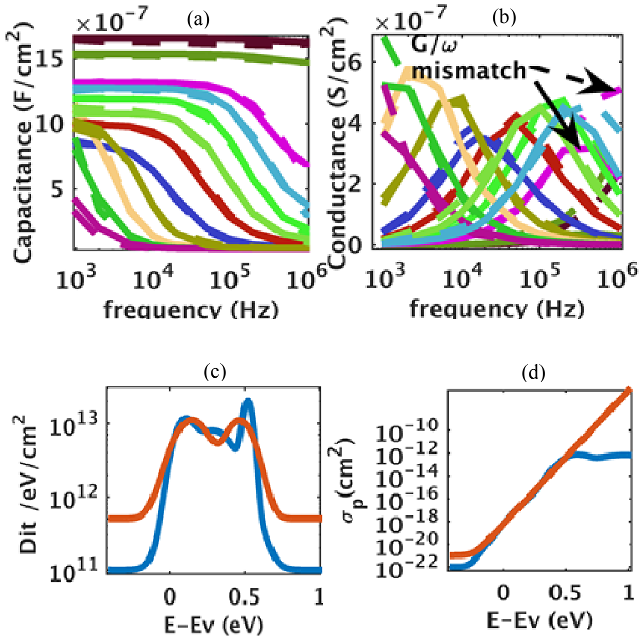

Fig. 4 (a). Fitting of capacitance using 4 Gaussians for density of interface states and capture cross section, showing the measured (dashed) and fitted (solid) curves. (b). Consistent conductance match is obtained even if only the capacitance is explicitly fitted, indicating that the interface state model is sufficient to explain the frequency dispersion in depletion even at ultrathin EOTs. G/ω whose peaks appear at higher frequencies show some mismatch at higher frequencies. (c). Extracted $\mathbf{D_{it}}$ profile using 4 Gaussians (blue) and 2 Gaussians (red). (d) Extracted capture cross section using 4 Gaussians (blue) and an Exponential (red).

Fig. 4(a) shows the capacitance-only fitting from -0.15V to 0.75V using the method shown in Fig. 1. We observe from Fig. 4(b) that the G/ω characteristics are also reasonably well-matched using the parameters obtained from the capacitance-only fitting, even though the G/ω are not intentionally fitted. This consistency is due to the fact that the frequency dispersion is completely explicable using the interface trap model we have used. In Fig. 4(b) it is seen that G_m/ω is not well-matched at higher frequencies (500KHz and 1MHz). We have verified that, conversely, conductance-only fitting leads to a mismatch at higher frequency when it comes to capacitance.

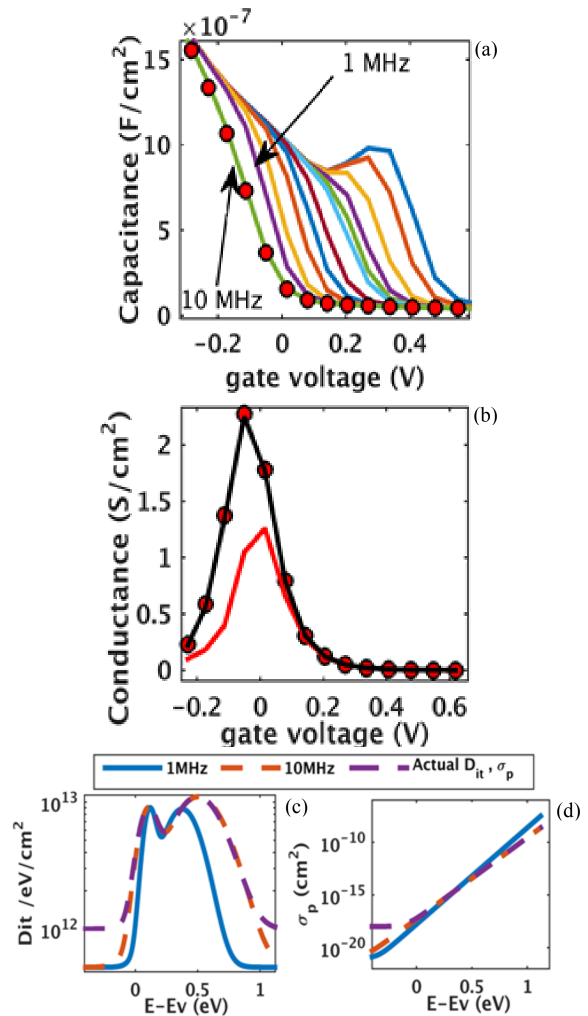

Fig. 5 (a). C-V for the stack of Fig. 3(a) assuming synthetic $\mathbf{D_{it}}, \boldsymbol{\sigma_p}$ profiles. The red circles represent C-V data assuming dc stretch-out only, i.e. no ac trap response, matched much better by a 10MHz C-V than 1MHz. (b). G-V characteristics for $\mathbf{D_{it}}, \boldsymbol{\sigma_p}$ profiles extracted from ac response free C-V (red circles) – again, matched much better by C-V extracted from 10MHz C-V (solid black) than from 1MHz C-V (solid red). (c). $\mathbf{D_{it}}$, and (d). $\boldsymbol{\sigma_p}$ profiles extracted from the 10MHz and 1MHz C-V are compared to the actual (synthetic) profiles

To understand the mismatch in conductance at higher frequencies, we first simulate the multi-frequency C-V on the same stack using a synthetic interface state density – the result

is shown in Fig. 5(a). Next, we treat this multi-frequency C-V as measured data and perform D_{it} extraction as laid out in Sec. III. Two cases are studied here: at the comparison step in the extraction methodology (c.f. Fig. 1), the high-frequency C-V that is assumed to be free of ac trap response is 1MHz in the first case, and, 10MHz in the second. From Fig. 5(c), it is seen that the second accurately recovers D_{it} and σ_p whereas the first is only accurate in the lower half of the bandgap; we may note that this is also what one gets with the conventional conductance method of Nicollian and Brews [2] for p-type capacitors. This suggests that high frequency measurement (10 MHz) could extend the room-temperature extraction of D_{it} and σ_p over the entire bandgap.

V. CONCLUSION

We have developed a MOS capacitor modelling platform that integrates a Schrödinger-Poisson solver with trap models. It is seen to capture physico-chemical effects essential to high-k on heterostructure capacitors, enable extraction of trap density profiles, and suggest limitations of prevailing characterization techniques. While this platform has been largely calibrated using Group-IV heterostructure capacitors so far, it can be applied similarly to III-V heterostructure capacitors. A friendly user-interface has also been developed and will be provided online.

REFERENCES

[1] H. Wang, G. Wang, S. Chang and Q. Huang, “Accelerated solution of Poisson-Schrodinger equations in nanoscale devices by Anderson mixing scheme,” Micro Nano Lett., vol. 4, pp. 122–127, 2009.

[2] E. H. Nicollian and J. R. Brews, “MOS (metal oxide semiconductor) physics and technology,” NY: Wiley, 1982.

[3] Y. Yuan, B. Yu, J. Ahn, P. C. McIntyre, P. M. Asbeck, M. J. W. Rodwell and Y. Taur, “A Distributed Bulk-Oxide Trap Model for Al_2O_3 InGaAs MOS Devices,” IEEE Trans. Electron Devices, vol. 59, no. 8, pp. 2100-2106, Aug 2012.

[4] K. Martens, C. O. Chui, G. Brammertz, B. D. Jaeger, D. Kuzum, M. Meuris, M. M. Heyns, T. Krishnamohan, K. Saraswat, H. E. Maes and G. Groeseneken, “On the Correct Extraction of Interface Trap Density of MOS Devices With High-Mobility Semiconductor Substrates,” IEEE Trans. Electron Devices, vol. 55, no. 2, pp. 547-556, Feb 2008.

[5] S. Sant, S. Lodha, U. Ganguly, S. Mahapatra, F. O. Heinz, L. Smith, V. Moroz and S. Ganguly, “Band gap bowing and band offsets in relaxed and strained $Si_{1-x}Ge_x$ alloys by employing a new nonlinear interpolation scheme,” J. Appl. Phy., vol. 113, no. 3, 2013.

[6] M. M. Rieger and P. Vogl, “Electronic-band parameters in strained $Si_{1-x}Ge_x$ alloys on $Si_{1-y}Ge_y$ substrates,” Phys. Rev. B, vol. 48, no. 19, 1993.