Physical Simulation of Si-Based Resistive Random-Access Memory Devices

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***Abstract*— We present a newly-developed three-dimensional (3D) physical simulator suitable for the study of resistive random-access memory (RRAM) devices. We explore the switching behavior of Si-rich silica (SiO_x) RRAM structures, whose operation has been successfully demonstrated experimentally at ambient conditions [1]. The simulator couples self-consistently a simulation of oxygen ion and electron transport to a self-heating model and the 'atomistic' simulator GARAND. The electro-thermal simulation model provides many advantages compared to the classical phenomenological models based on the resistor breaker network. The simulator is validated with respect to experimental data and captures successfully the memristive behavior of the simulated SiO_x RRAMs, by reconstructing the conductive filament formation and destruction phenomena in the 3D space. The simulation framework is useful for exploring the little-known physics of SiO_x RRAMs, and providing efficient designs, in terms of performance, variability and reliability, for both memory devices and circuits.**

Keywords*— *Si-rich silica (SiO_x) memristors; resistive switching; charge transport; self-heating; physical simulations;

I. INTRODUCTION

Resistive random-access memory (RRAM) devices are a special case of a general class of memory devices that exhibit a resistance that depends on the past history of the device (memristance) [2]. These nonvolatile memory based devices (also known as memristors) have attracted substantial attention in the last few years [1]-[14], as they offer improved controllability of resistance switching in semiconductor memories at small sizes. Moreover, and as highlighted by the ITRS report of 2010 on emerging research devices [12], there are many incentives for developing RRAM technologies, including their low cost-per-bit, low power dissipation, high endurance, and last but not least their suitability for integration in crossbar arrays in the three-dimensional (3D) space. Potential applications of memristors range from high-density memories and novel processor architectures to neuromorphic computing and neural networks.

Memristors have been suggested in the 70's [15], but it was only until 2008 that the first practical demonstration of the devices, using titanium dioxide (TiO_2), was reported [13]. Several RRAM technologies are currently under consideration, including phase-change materials (chalcogenides, perovskites, Ge sulphide and selenide) [10], silicon oxides [1] and metal oxides (NiO, TiO_x, HfO_2) [13], in which resistance is switched through the formation and destruction of conductive filaments (CFs), by exploiting field- and temperature-driven redistribution of oxygen ions. Other exotic types of memristors, in which switching is due to purely electronic phenomena, also exist such as ferroelectric memristors [7]. While memristors based on metal oxides are currently considered most promising, they face a serious challenge related to on-chip integration on silicon. The development of SiO_x-based RRAM devices (x<2), as explored in this work, could result in a breakthrough in low-cost on-chip integration with silicon microelectronics.

We introduce a self-consistent physical simulator of intrinsic switching in silicon-rich silica RRAM devices. Physical switching in these devices has been demonstrated experimentally under ambient conditions [1]. In Ref. [1], Kenyon and co-workers reported devices that can be cycled between high resistance 'OFF' and low resistance 'ON' states with a resistance contrast of 10,000 or more, for a relatively long period. Most theoretical and experimental work on resistive switching focuses on devices based on metal oxides (e.g. TiO_2 or HfO_2). Moreover, previous modeling work has relied mostly on classical phenomenological models based on the resistor breaker network [14]. These models do not calculate self-consistently the electric fields and do not consider accurately the heat dissipation and diffusion phenomena. Our simulator uses a powerful combination of tools, to correctly reconstruct the conductive filament formation and destruction in 3D, by coupling self-consistently oxygen ion and electron transport simulations to the local electric field and temperature distributions determined from physical and atomistic models.

II. SIMULATION MODEL

We have developed a physical simulation framework to capture the switching behavior of the SiO*x*-based RRAM structure shown in Fig. 1 [1]. The full structure usually consists of a thin (10-120nm) layer of SiO_x between *n*-type electrodes (poly-Si) and a *p*-Si substrate with a Cr/Au electrode at its base. The poly-Si plates typically have an area of 125µm×125µm. In the 3D space, we couple a stochastic kinetic Monte Carlo (KMC) simulation of ion and electron transport to the 'atomistic' simulator GARAND [16] and a time-dependent heat diffusion equation (HDE) solver to capture switching in these Si-based RRAMs. The positions of oxygen ions and vacancies, and trap occupancies are tracked in time, and the electric field **E** is updated self-consistently, according to the resulting charge distribution using GARAND; GARAND accurately evaluates the electric field and potential distributions

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in a nano-device, by coupling the solutions of Poisson's equation and density-gradient equations. The local heat generation is then determined by the dot product of the field and current density vectors **J**•**E**, assuming Joule heating is the dominant mechanism for dissipation. Temperature rise due to self-heating is calculated by the resolution of the time-dependent HDE

$$\nabla \bullet \left[\kappa(\vec{r},T)\nabla T(\vec{r},t)\right] + g(\vec{r},t) = \rho C \frac{\partial T(\vec{r},t)}{\partial t}, \qquad (1)$$

using a more advanced in-house solver, as compared to time-independent HDE solvers employed for example in [18], [19]. In equation (1), $T(\vec{r}, t)$ and $g(\vec{r}, t)$= **J**•**E** are the temperature and heat generation, respectively, at a given position $\vec{r}$ and time t, $\kappa(\vec{r},T)$ is the temperature-dependent thermal conductivity, ρ is the material density and C is the specific heat capacity. The field and temperature distributions are updated regularly, and are used to calculate (see Ref. [9]): (i) the attempt-to-escape rate for oxygen to jump over its barrier, (ii) the probability of vacancy recombination, and (iii) the velocity of the field and temperature-assisted ion hopping. The distributions are also used to update the traps' electron occupancy by calculating the hopping rate between the traps (Mott hopping), and the tunneling rates between the traps and the electrodes using the Wentzel-Kramers-Brillouin (WKB) approximation. The occupancies and tunneling rates are used to evaluate the steady-state electric current through the device using a solver similar to that proposed in [9]. The flowchart shown in Fig. 2 illustrates the simulation procedure. The simulator is validated against experimental trends of Si RRAM structures [1]. One important aspect of the simulator is the use of an advanced structure editor, which allows the generation of a simulation structure of arbitrary geometry and material profile. This is particularly useful when studying realistic SiO_x RRAM structures incorporating silicon-rich areas (with Si nano-inclusions) in the oxide.

III. Results and Discussion

A. Memristive switching processes

We demonstrate the capabilities of our simulator by modeling a 3D section under one of the *n*-type poly-Si plates shown in Fig. 1. We use an oxide thickness (T_{ox}) of 10nm and a simulation contact area of 100nm long and 100nm wide. We reconstruct the memristive behavior of the Si RRAM by studying the conductive filament formation and rupture processes. Fig. 3 shows the *I–V* characteristics of the device. Fig. 4 illustrates the filament formation process by plotting the vacancy distribution in the oxide. The simulation starts with an initial vacancy distribution in a given volume of the oxide (corresponding to a grain boundary), which results in a small 'OFF' current at low bias voltages. Indeed, at low electric fields, very few (if any) oxygen vacancies are generated, which is reflected by the very low device current [point (a) of Fig. 3 and Fig. 4(a)]. As the bias voltage is increased, more vacancies are generated, as the rate of oxygen ions jumping over their barrier increases exponentially as $\exp\left[-e(E_a - aE)/k_bT\right]$, where E_a is the formation energy, a is the lattice constant, E is the electric field, T is the lattice temperature, e is the electronic charge, and k_b is the Boltzmann constant. At around 10V, filament seeds start to appear [point (b) of Fig. 3 and Fig. 4(b)]. These seeds start growing in a visible fashion as the voltage is increased [point (c) of Fig. 3 and Fig. 4(c) at bias 14V]. At approximately 16V, an accelerated generation of oxygen vacancies occurs and starts to form a complete conductive filament, bridging the poly-Si plates to the *p*-Si substrate [point (d) of Fig. 3 and Fig. 4(d)]. This gives rise to percolation paths in the 3D space, through which current flows directly from the substrate to the poly-Si plates [17]. This makes the device current abruptly jump to a very high value, switching the resistance of the two-terminal device from a high value (corresponding to the high resistance state – HRS) to a low value (corresponding to the low resistance state – LRS). Fig. 4 highlights the 3D nature of percolation paths in real devices.

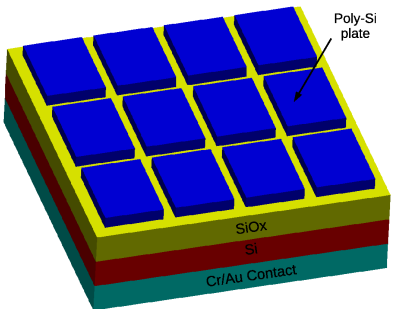

Fig. 1. A 3D schematic diagram of the experimental structure from Ref. [1]. The test devices considered in [1], as developed by Kenyon and co-workers, consist of a 10-120nm layer of silica between *n*-type contacts (poly-Si) and a *p*-Si substrate. The poly-Si plates typically have an area of 125μm×125μm.

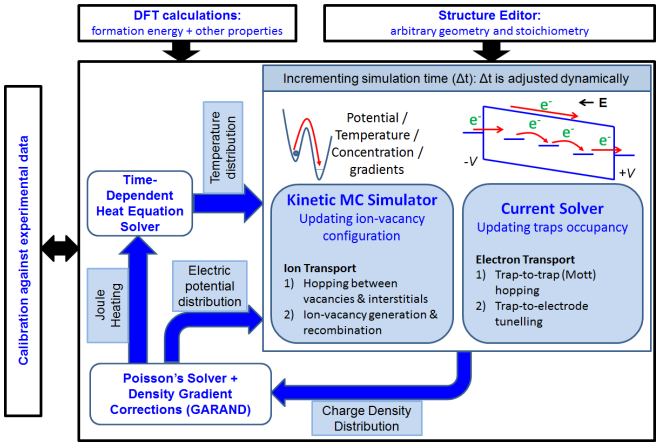

Fig. 2: The simulation framework, coupling self-consistently oxygen ion and electron transport to the local electric field and temperature distributions.

Once the conductive filament is formed, we impose a current compliance limit. As the bias is gradually reduced after

filament formation, the oxygen ions in the contact with the high bias (poly-Si) and elsewhere can migrate back to/through the oxide, hop through vacancies and eventually recombine with other vacancies; the device is maintained at the LRS for a large bias range before the device switches back to a HRS at low biases, as the filament is ruptured. Therefore, considering the aforementioned behavior, the two-terminal device is characterized by a variable resistor, whose effective resistance value depends on the current flowing through it, giving rise to its memristive characteristics.

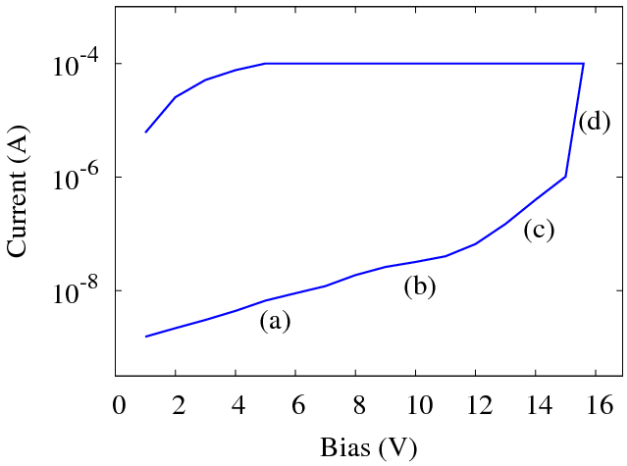

Fig. 3. The *I–V* characteristics of the device.

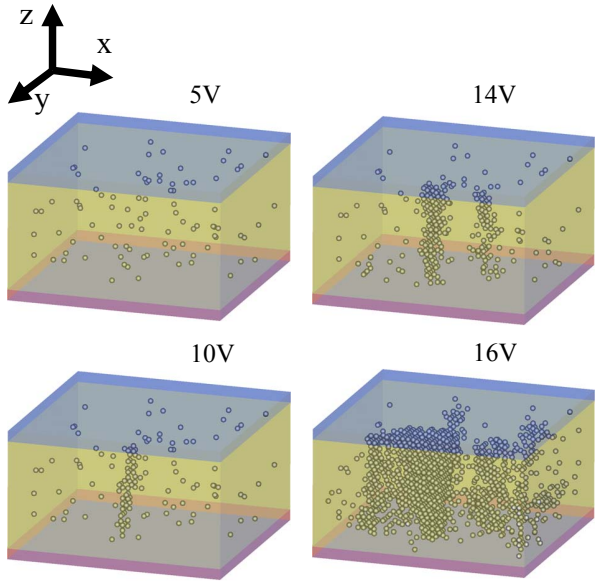

Fig. 4. The vacancy distribution through the filament formation process in the oxide (yellow volume). The Poly-Si electrode starts at z=10nm (blue volume) while the *p*-Si substrate ends at 0nm (red volume). The shown volume has an area of 20nm×20nm. (a) At low biases (5V in this case), only a small number of oxygen vacancies are generated. (b) As the bias voltage is increased (10V in this example), more vacancies are generated and filament seeds start to appear. (c) The seeds start to grow in a visible fashion as the voltage is increased (a 14V applied bias in the subfigure). (d) At approximately 16V, an accelerated generation of oxygen vacancies occurs and forms a complete conductive filament, bridging the poly-Si plates to the *p*-Si substrate. Percolation paths are created, which is translated by the abrupt jump in device current.

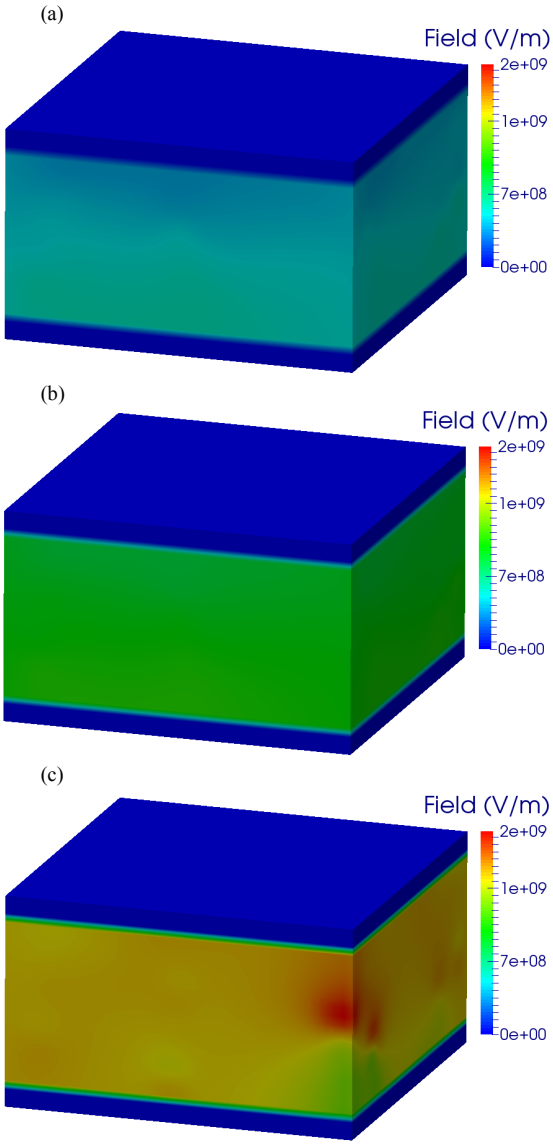

Fig. 5. The 3D distribution of the electric field magnitude (in V/m) at a given instant, and a bias of (a) 5V, (b) 10V, and (c) 16V, in the oxide volume (10nm thick, 20nm long and 20nm wide), and its poly-Si and *p*-Si substrate boundaries. The x, y and z axes scale ranges are the same as those defined in the caption of Fig. 4.

B. Microscopic characteristics

Fig. 5 shows the electric field magnitude as calculated from GARAND at a given instant, for three biases (5V, 10V and 16V), in the oxide. Fig. 6 shows a typical temperature map, at a given instant, just before the conductive filament formation. Clearly, the temperature maps are much less localized than the electric field [and hence power density (Joule heating)] maps. Just before the complete filament formation, the temperature can reach values as high as 470K, as illustrated in Fig. 6 (and in general even higher – up to 550K at some conditions),

suggesting the important role of self-heating in the operation of resistive switching memory devices. Local temperature rise due to self-heating affects seriously the device behavior, as it boosts the probability of vacancy generation and ion hopping.

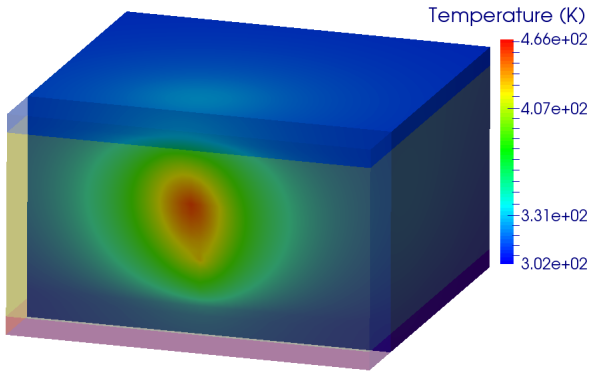

Fig. 6. A typical temperature distribution, at a given instant, during the CF formation. The *x*, *y*, and *z* axes scale ranges are the same as those defined in the caption of Fig. 4.

IV. Conclusion

We have developed a physics-based 3D simulator for resistive switches and presented results from its application to silicon-rich silica (SiO_x) devices. The simulator couples a stochastic simulation of ion transport and electron transport to the 'atomistic' simulator GARAND and a time-dependent heat flow equation solver to capture the switching behavior of the devices. We have illustrated the efficiency of our simulator by studying the forming and rupture of the conductive filament. Interesting future work includes investigating the effect of the excess Si percentage and Si nano-inclusions in the oxide layer. The simulator represents a very predictive tool for exploring the little-known physics of SiO_x RRAMs, and providing efficient designs, in terms of performance, variability and reliability, for both devices and highly-packed memory circuits.

Acknowledgment

We would like to thank the EPSRC (UK) for funding under the grant EP/K016776/1.

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