Layout-induced stress effects on the performance and variation of FinFETs

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***Abstract*—Recently, LLEs(Local Layout Effects) and their impact on performance due to STI stressor and eSiGe S/D have been reported in FinFETs[1]. However, the impacts of gate and contact stress are rarely demonstrated. In this paper, we extended the LLE factors to the gate and contact and analyzed their impact on the electrical parameters of mobility, IdSat and VtSat via TCAD simulation study. This work shows that 5(20)% of n(p)FET performance enhancement and only 1(2)% of IdSat variation can be obtained through optimal stress components aligned with LLE factors.**

Keywords—variation; LLE; FinFET; stress simulation; STI, TCAD, layout;

I. Introduction

With the down-scaling of devices, the stress from the surrounding trench oxide structures, gate, contact, and other stressors – used for performance boosting – has aggravated LLE. The LLE impact on the FinFET performance due to the STI (Shallow Trench Isolation), DTI (Deep Trench Isolation), and eSiGe S/D (embedded SiGe Source/Drain) has been reported by various researchers. Their approaches, however, are limited to the trench insulators and the impact was only described by the variation of mobility [1].

We included the stressors of metal gate and contact as well as STI, S/D stressor and analyzed the influence of the whole LLE factors on the electrical parameters such as on-current and threshold voltage, which are known to be critical for the LLE evaluation of actual chip-level products. Based on the analysis, we proposed the optimal combination of various stressors, besides, obtained more insensitive condition to variation.

II. Simulation Methology

Stress induced LLEs were analyzed using device and process simulations. The simulations were done with cell-level layouts. All the simulations in this work, as shown in the Fig. 1, were performed using the in-house tool, which is capable of three-dimensional device and process simulations including dopant diffusion and mechanical stress calculation. The dopant and stress profile were obtained from the process simulations, and then used in the device simulations for evaluation of their impact on the electric parameters. [2, 3].

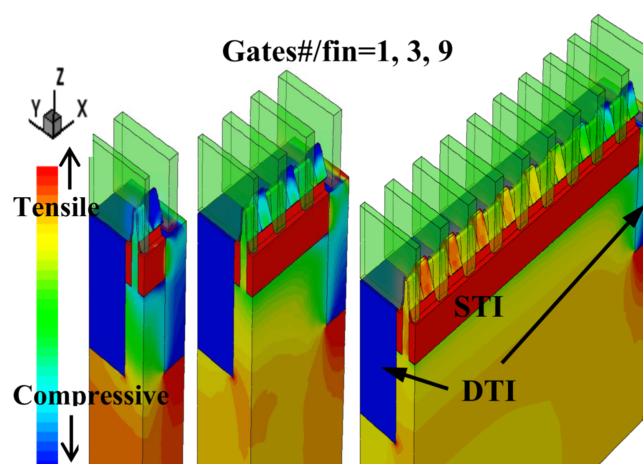

Fig. 1 : Schematic of original dual trench scheme for enhancement of drive current and small LLE. Note that stress distribution is different depending upon the layout.

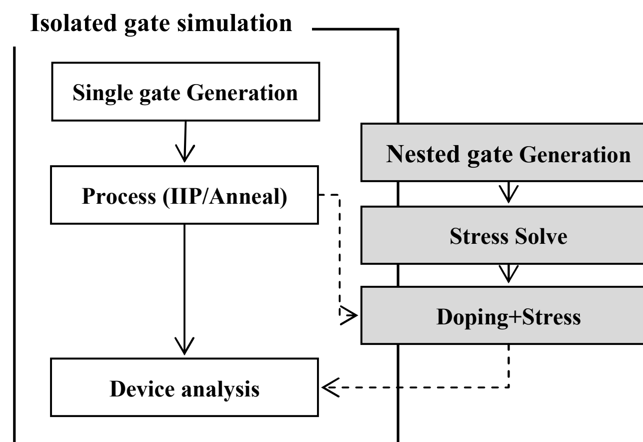

Fig. 2 : Simulation flow for evaluation of stress impact on the electrical parameters of device.

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III. RESULTS AND DISCUSSION

The impact of each stress source on LLE was investigated for the dual trench architecture (shown in Fig. 1). The optimal stress combination of those stress factors has been proposed for LLE minimization.

A. DTI stress impact on LLE

Fig. 3 shows the IdSat behavior with the number of gates (NG) under various stress polarity of DTI and fully relaxed STI. The simulated IdSat and VtSat values in this paper are all in percentage and are normalized by the current level under condition of single gate per fin and no DTI stress.

As shown in Fig. 3(a), the variation of IdSat in NFET between single gate and 9-NG – with 1[GPa] tensile stress from DTI – is around 14%. Unlike nFET, the variation is more in case of pFETs (~26%), which is due additional eSiGe S/D stress. Under compressive stress condition, the variation of IdSat in nFET is suppressed to 1%, but it's large for pFETs (~31%)

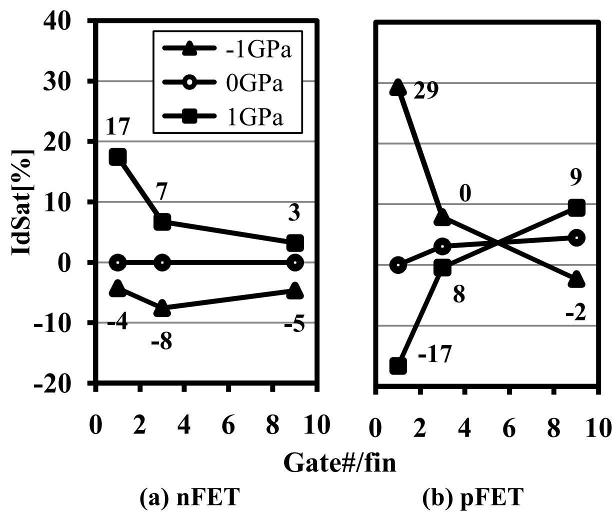

Fig. 3 : IdSat versus number of gates (NG) behavior for various DTI stress polarity when in neutral STI stress, STI=0 GPa, where IdSat(%)=100x[IdSat-IdSat(Gate#/fin=1)@DTI=0GPa]/ IdSat(Gate#/fin=1)@DTI=0GPa.

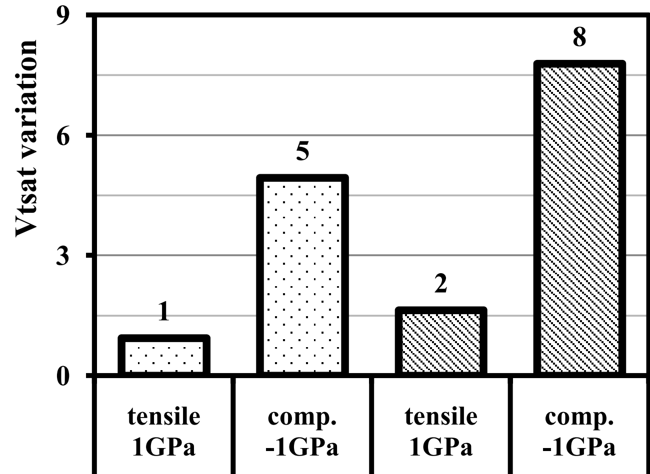

Fig. 4 : DTI stress dependency of VtSat variation when STI=0GPa, where Vtsat variation=|VtSat(1gate/fin)-VtSat(9gates/fin)|.

Fig. 4 shows the stress impact on VtSat variation. Both the compressive and tensile stress affect VtSat level. However, irrespective of device polarity, compressive stress generates larger VtSat variation as compared to the tensile stress.

The mobility variation with the total channel stress – tensile and compressive – is illustrated in Fig. 5. The change in IdSat is affected by both VtSat and mobility variation. As the amalgamation of these effects make the IdSat behavior quite complicated, the DTI stress should be neutralized to suppress the DTI-induced LLE. it is known that the stress value of trench insulators can be controlled by changing the trench gap-fill material [4].

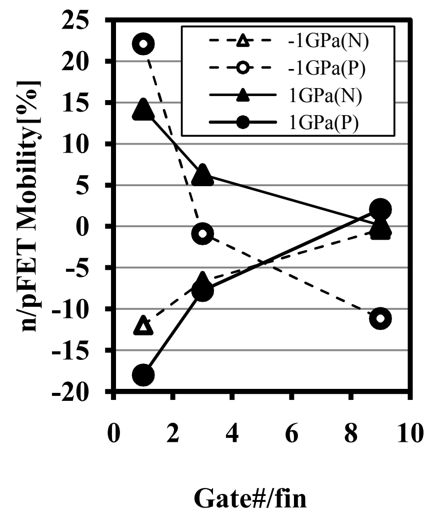

Fig. 5 : n(p)FET mobility versus number of gates (NG) behavior for various DTI stress polarity when in STI=0 GPa, where mobility is normalized by each type of device's mobility when in gate#/fin=1.

Fig. 6 shows the IdSat variation of nFET under compressive stress in terms of Sxx, Syy, where Sxx is the stress in transport or channel direction, and Syy is in transverse direction.

The contours are the set of Sxx and Syy values causing 10[mV] and 30[mV] of VtSat shift. Under condition of negative Sxx and Syy, the IdSat variation is lower than the ΔIdSat under tensile stress. For the same VtSat shift, about 40% higher level of stress value is required when tensile stress is applied in channel direction.

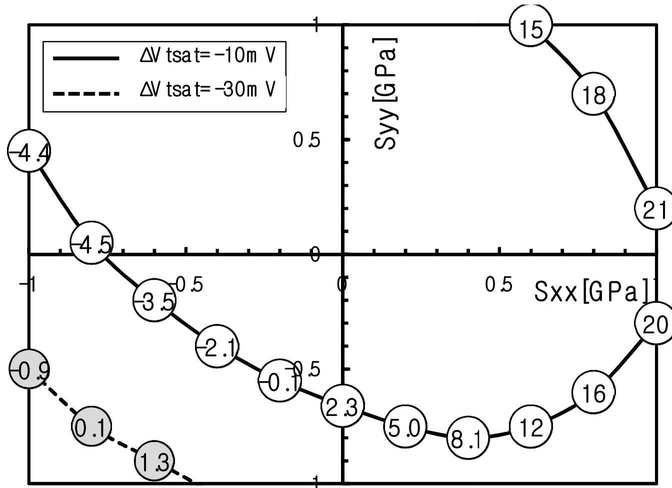

Fig. 6 : Channel stress dependency of VtSat(IdSat) variation for nFET. Vtsat variation is prone to compressive stress as compared to tensile.
Values in the circle : % ratio of IdSat(Sxx,Syy)/IdSat(0,0) .
∆VtSat = VtSat(0,0) – VtSat(Sxx,Syy).

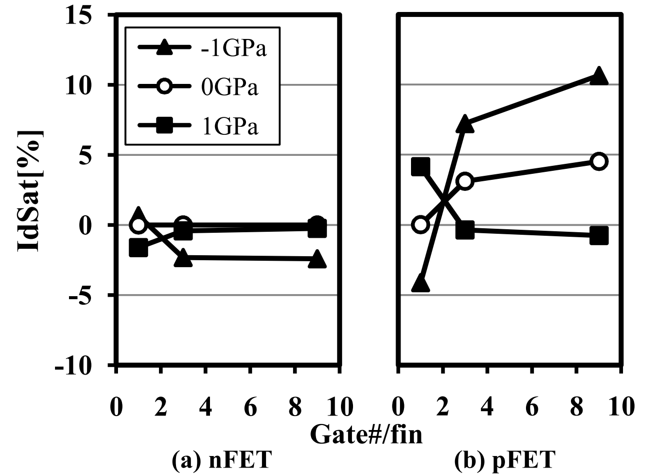

Fig. 7 : IdSat and VtSat versus NG behavior for various STI stress polarity when neutral DTI stress, DTI=0 GPa

B. *STI stress impact on LLE*

Fig. 7(a) and 7(b) illustrates IdSat and VtSat variation along NG for various STI stress polarity under relaxed DTI. It is clear from Fig.8 that the impact of STI stress on LLE is relatively weaker than of DTI stress. This is due to the local impact of STI. Contrary to DTI, STI isolates each device so that it is periodically arranged, which means the stress profile due to STI is nonlocal and limited. Therefore, STI does not contribute to the layout effect seriously, and acts as a performance booster due to its stress level. However, the local impact should be considered when the stress level is high.

The impact of tensile stress STI on LLE is smaller than the compressive STI, and the tensile STI stress makes IdSat of pFET increased as shown in Fig. 7(b). This is contrary to the negligible impact of STI stress on nFET's IdSat. Both the compressive and tensile stress of STI contribute to the IdSat variation of nFETs. In aspect of VtSat, as shown in Fig. 4 and 6, the VtSat variation is more serious under compressive stress in channel. Therefore, the tensile STI can contribute to reduction of LLE. We can also expect some performance gain from well optimized stress of STI.

In Fig. 8, the stress impact of DTI and STI on nFET's IdSat level is illustrated. The variation is defined by the gap between single-gate and 9-NG results. It is clearly shown that both the IdSat and VtSat variation are strongly affected by the DTI stress, which means the layout dependent variation is mainly generated by the DTI. Fig. 8 also shows that both the IdSat and VtSat variation can be reduced under relaxed DTI condition. When the DTI stress is almost targeted in aspect of LLE, a small increase of tensile DTI stress can be neutralized by some small increase of the STI stress.

We also included the stress impact of the metal gate (MG) and contact. It is observed that resulting stress induced by MG array is distributed uniformly in space, leading to no LLE. Therefore, we used MG and contact stress to boost drive current.

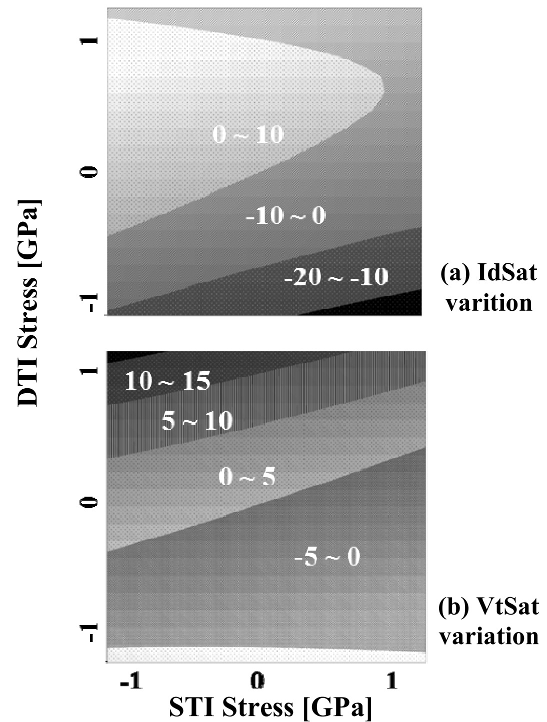

Fig. 8 : Contour view of (a)IdSat and (b)VtSat variation of nFET to various STI/DTI values, where numbers indicate IdSat(or VtSat) variation = #(1gate/fin) - # (9gates/fin)

Fig. 9 indicates that the performance increases with the stress enhancement of the STI, MG and contact while the variation is reduced with smaller stress of DTI. In this simulation, the gate and contact stress are regarded as spatially uniform so that only contribute to the performance gain. The STI stress shows spatial variation, but the influence on the LLE is quite limited due to its periodicity along the fin length.

Therefore, the STI, gate and contact stressors are effective for performance boosting without serious impact on LLE.

Under the device architecture of this work, we optimized the stress levels of the stressors. In nFET, the combination of fully relaxed DTI, tensile STI, tensile gate and compressive contact demonstrated 5% performance gain and 1% of IdSat lift, which is 6% higher performance and 0.5% lower variation compared with the 1[GPa] tensile STI case shown in Fig. 9. The optimized condition was more effecitive in pFET, so 20% of performance gain and 2% of IdSat variation were achieved under this combination. Comparing with the 1[GPa] STI case, the performance gain is 19% higher and the IdSat variation is 3% lower.

IV. CONCLUSION

We have analyzed the stress impact of DTI, STI, gate and contact on the transistor variability and the performance. The DTI stress mainly determines the variability aspect of the LLE while the STI, Gate and contact stress strongly influence the performance gain.

For the variability-performance optimization, the DTI stress should be relaxed while the stress levels of other LLE factors are adjusted for better performance. The combination of the fully relaxed DTI, tensile STI, tensile gate and compressive contact could reduce the variation and boost the performance.

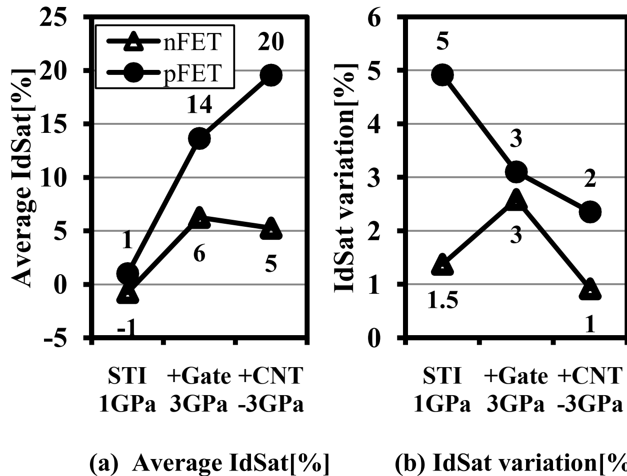

Fig.9 : Results of the best stress combination for boosting the performance (IdSat) and suppressing the LLE under condition of fully relaxed DTI, tensile STI and gate, and compressive contact, where (a) Average IdSat = sum(IdSat of gates#/fin 1,3,9) /3 (b) IdSat variation = IdSat (1gate/fin) - IdSat (9gates/fin).

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