Electrical Characteristic of InGaAs Multiple-Gate MOSFET Devices

Cheng-Hao Huang
Parallel and Scientific Computing Laboratory and
Institute of Communications Engineering
National Chiao Tung University
Hsinchu, Taiwan

Yiming Li
Parallel and Scientific Computing Laboratory and
Department of Electrical and Computer Engineering
National Chiao Tung University
Hsinchu, Taiwan
ymli@faculty.nctu.edu.tw

***Abstract*—In this work, we study the impact of channel fin width (W_{fin}) and fin height (H_{fin}) on III-V multiple-gate metal-oxide-semiconductor field-effect transistors (MOSFETs). We numerically simulated the output and transfer characteristics and the short-channel effect (SCE) of 14-nm InGaAs triple-gate MOSFETs by using an experimentally validated simulation. The engineering findings of this study indicate that devices with W_{fin} = 10 nm and H_{fin} between 14 and 21 nm possess optimal characteristic owing to a tradeoff between the drain-induced barrier lowing and subthreshld property. The effects of channel resistance, effective width, and quantum confinement resulting from the H_{fin}-dependent small energy band gap channel film on device characteristic are further estimated and discussed.**

Keywords—III-V, InGaAs, multiple-gate, fin width* (*W_{fin}*), *fin height* (*H_{fin}*), *metal-oxide-semiconductor field-effect transistor* (*MOSFET*), *quantum confinement, short-channel effects* (*SCEs*).

I. INTRODUCTION

Silicon-based MOS device has faced various challenges on such as material replacement, structure innovation, and process improvement. Diverse InGaAs MOSFET devices have drawn attention owing to fascinating device performance [1]. Such high electron mobility device is now considered as a promising candidate to replace silicon-based complementary metal oxide semiconductor (CMOS) devices at sub-14-nm nodes [2-4]. Among different channel films, InGaAs/InAlAs stacking layer is one of highly attractive III-V materials due to little lattice mismatch [5] and superior heterojunction transport property [6].

Recent studies have focused on the interface engineering between high-κ dielectric and III-V channel to reduce the interface trap density (D_{it}), which is critical for realizing steep sub-threshold swing (SS) at off state as well as large current drive at on state [7]. To suppress the short channel effect, both the non-planar and ultra-thin body devices [8-10] have been reported for dimension scaling. Researches about channel films or source/drain layers deposition were studied [11,12]. However, optimal electrical characteristic of III-V devices has not been computationally investigated yet. Therefore, in this work, we study the DC characteristic of 14-nm-gate InGaAs tri-gate MOSFET devices with respect to different W_{fin} and H_{fin} of the device channel.

This work was supported in part by the Ministry of Science and Technology, Taiwan, under Contract No. MOST 103-2221-E-009-180.

II. THE COMPUTATIONAL DEVICE MODEL

Figure 1(a) briefly lists the process simulation flow of the explored device. By following the process flow, we can form the proposed device structure. Figure 1(b) shows the entire 3D device structure, where the channel length (L_g), W_{fin}, and H_{fin} are marked on it, and Figs. 1(c)-(d) are the cross-sectional views along the cutting lines AA' and BB' in Fig. 1(b), respectively. The simulated device is numerically fabricated on silicon substrate. InP, $In_{0.52}Al_{0.48}As$ buffer layer, $In_{0.53}Ga_{0.47}As$ channel layer, and N+ doped InGaAs source/drain layer are sequentially grown on the substrate. All the layers are undoped except the source/drain, which is heavily doped with silicon as the n-type impurities. The adopted device structural parameters are listed in Table I, where W_{fin} varies from 7 to 14 nm and H_{fin} ranges from 7 to 35 nm.

The DC characteristic of the explored device is simulated by solving a set of 3D density-gradient drift-diffusion equation numerically [13,14]. The band gaps of the relevant binary compounds are functions of temperature, as shown in

$$E_g(\mathrm{InAs}) = 0.36 - 2.760 \times 10^{-4}\, T^2 / (T + 93)\,, \qquad (1)$$

$$E_g(\mathrm{GaAs}) = 1.42 - 5.405 \times 10^{-4}\, T^2 / (T + 204)\,, \qquad (2)$$

and the band gap of ternary compound depending on the composition fraction (x) is given by [15]

$$E_g(\mathrm{In}_{1-x}\mathrm{Ga}_x\mathrm{As}) = 0.36 + 0.629x + 0.436x^2\,. \qquad (3)$$

The traps placed at the high-κ gate oxide-InGaAs interface are distributed within a narrow gap near the conduction band edge. They are acceptor type and negatively charged when occupied, where the density of interface traps is $4\times10^{11}\mathrm{eV}^{-1}\,\mathrm{cm}^{-2}$ [16]. The mobility of surface roughness scattering and the acoustic mobility due to acoustic phonon scattering are included by enhanced Lombardi model [17]. These mobility are then combined with material's bulk mobility through the Matthiessen's rule [18], $1/\mu = 1/\mu_b + D/\mu_{ac} + D/\mu_{sr}$, where D is used to describe the damping that switches off the inversion layer from the interface. The mobility degradation due to the

978-1-4673-7860-4/15/$31.00 ©2015 IEEE

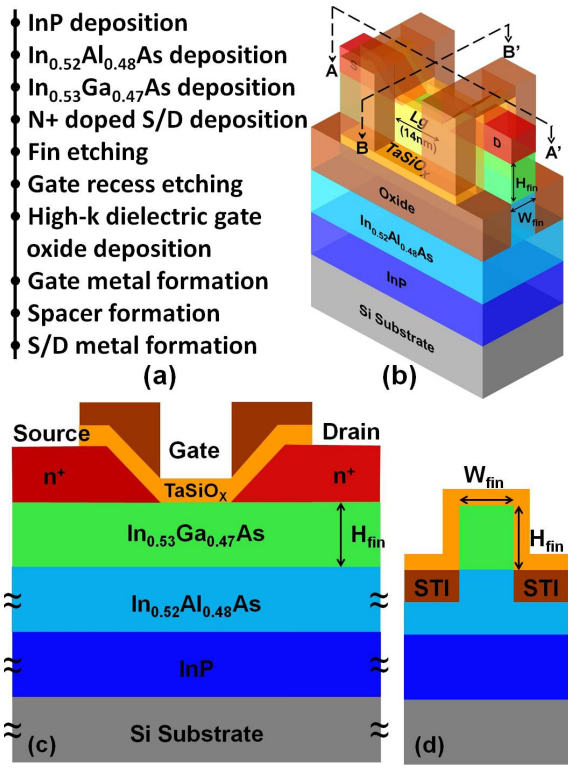

Fig. 1. (a) The summarized process simulation flow. We first simulate the device structure by running process simulation. (b) An illustration of 3D InGaAs tri-gate MOSFET. (c) Cross-sectional view of the device, along the cutting line AA' in (b). (d) Cross-sectional view of the device, along the cutting line BB' in (b). The L_g, W_{fin}, and H_{fin} are marked there

TABLE I. LIST OF STRUCTURAL AND PROCESS PARAMETERS

Parameters	Value
Effective oxide thickness	0.52 (nm)
Gate work function	4.76 (eV)
$In_{0.53}Ga_{0.47}As$ (S/D layer)	$1x10^{19}$ (cm^{-3})
$In_{0.53}Ga_{0.47}As$ (channel layer)	Undoped
$In_{0.52}Al_{0.48}As$ (buffer layer)	Undoped
InP	Undoped
Channel length (L_g)	14 (nm)
Fin width (W_{fin})	7, 10, and 14 (nm)
Fin height (H_{fin})	7, 14, 21, 28, and 35 (nm)

high-field velocity saturation model [19] is further considered. To validate the accuracy of our device simulation, we first calibrate the 3D device simulation to the experimental data [16], as shown in Fig. 2. The channel length of the calibrated device is 40 nm, which is relatively longer than this work.

III. RESULT AND DISCUSSION

Firstly, we fix the H_{fin} and examine the characteristic variation by changing W_{fin}. As shown in Fig. 3, the off-state electron density of the device channel increases with widening W_{fin} due to the smaller channel resistance. As W_{fin} widens, the

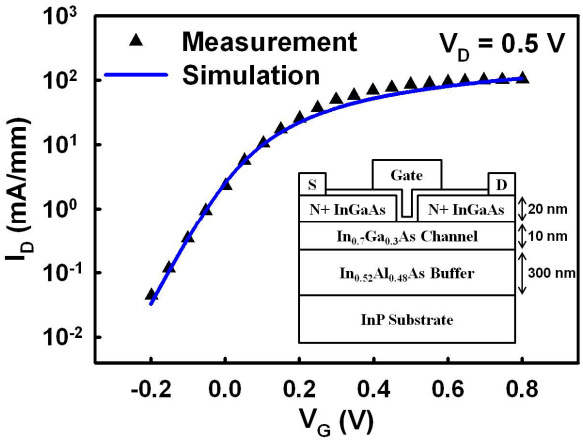

Fig. 2. Plot of I_D-V_G curve. Our device simulation is first calibrated to the experimental data. The inset shows the device structure and parameters.

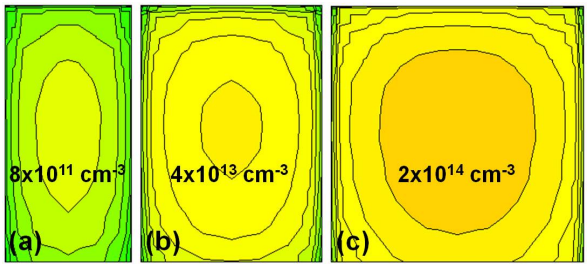

Fig. 3. Off-state electron density of the device channel with the same H_{fin} = 14 nm and W_{fin} = (a) 7 nm, (b) 10 nm, and (c) 14 nm. The Off-state electron density increases with widening W_{fin} due to the smaller channel resistance, where the resistance is reversely proportional to the cross-sectional area.

cross-sectional area of the channel will increase. The cross-sectional area is reversely proportional to resistance, as a result, the channel resistance decreases. I_{ON} and I_{OFF} versus W_{fin} is plotted in Fig. 4, and both I_{ON} and I_{OFF} increase when W_{fin} widens owing to the wide effective width (W_{eff}) and decrease of resistance, where W_{eff} is equal to W_{fin} + $2H_{fin}$. The device current is proportional to W_{eff}/L_g, consequently, I_{ON} increases with widening W_{fin}. However, the variation degree caused by changing W_{fin} for I_{ON} and I_{OFF} are different, so the device with W_{fin} = 10 nm has the largest on-/off-state current ratio.

To observe the variation of tuning H_{fin}, we plot the energy band diagrams of the off and on states from the insulator surface to the substrate, as shown in Fig. 5. The energy band gap of the $In_{0.53}Ga_{0.47}As$ channel layer is smaller than that of the $In_{0.52}Al_{0.48}As$ buffer layer, so the portion of low conduction band energy increases with heightening H_{fin}. For the off state, as shown in Fig. 5(a), device with short H_{fin} can confine more electrons than that with tall H_{fin}, which also means that carriers have the less leakage path to go through. For the on state, as shown in Fig. 5(b), the Fermi level is above conduction band, so the region between Fermi level and conduction band are filled with electrons. We can estimate the total electron concentration per unit volume in the conduction band by integrating the density of quantum states times the probability that a state is occupied by an electron over the conduction band

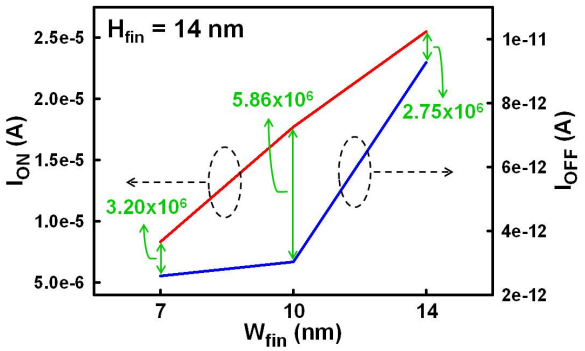

Fig. 4. Plot of I_{ON} (left Y axis) and I_{OFF} (right Y axis) versus the W_{fin} with a fixed H_{fin} = 14 nm. Both I_{ON} and I_{OFF} increase with widening W_{fin} due to the large effective width and the small channel resistance. The device with W_{fin} = 10 nm has the largest on-/off-state current ratio.

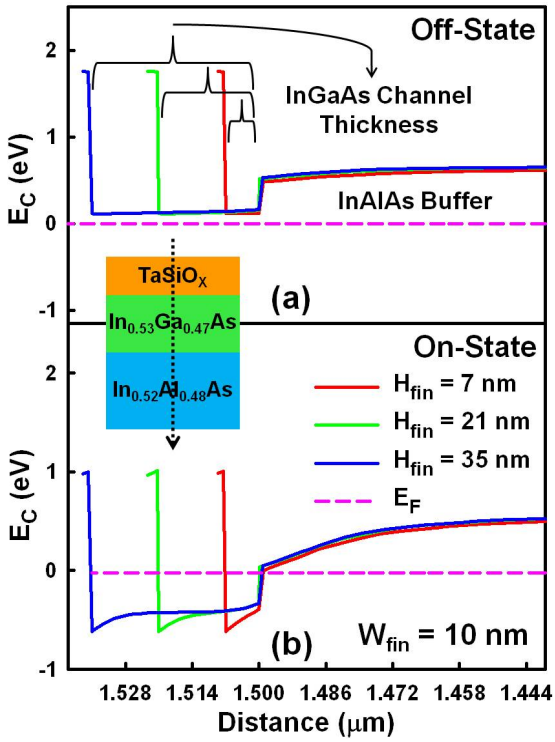

Fig. 5. (a) Off-state and (b) on-state energy band diagrams of the device with the same W_{fin} = 10 nm and H_{fin} = 7, 21, and 35 nm. As H_{fin} heightens, the portion of low conduction band energy increases. Device with short H_{fin} can confine more electrons, but device with tall H_{fin} can accommodate more electrons.

energy. Hence, the device with tall H_{fin} can accommodate more electrons through the channel and have the larger electron concentrations.

After that, we plot the I_D-V_G curves, as shown in Fig. 6, and both I_{ON} and I_{OFF} decrease with shortening H_{fin}. The performance of transport current is not only governed by W_{eff} and channel resistance but also the magnitude of quantum confinement resulting from the H_{fin}-dependent small energy

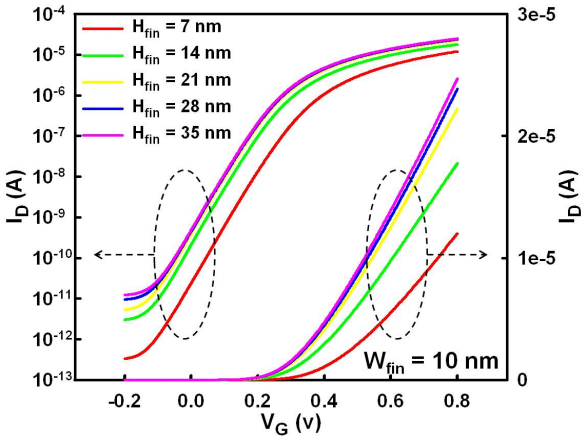

Fig. 6. I_D-V_G curves of the device with W_{fin} = 10 nm and different H_{fin}. The left axis is in log scale, and the right axis is in linear scale. Both I_{ON} and I_{OFF} decrease with shortening H_{fin}, and the reductions are getting considerable owing to the strong quantum confinement.

TABLE II. ELECTRICAL CHARACTERISTICS OF DEVICE WITH W_{FIN} = 10 NM AND VARIOUS VALUES OF H_{FIN}.

H_{fin}/W_{fin}	I_{ON} (A/μm)	I_{OFF} (A/μm)	I_{ON}/I_{OFF}	SS (mV/dec)	DIBL (mV/V)
35/10	$3.70x10^{-4}$	$2.61x10^{-10}$	$1.41x10^{6}$	71.54	41.33
28/10	$4.29x10^{-4}$	$2.42x10^{-10}$	$1.77x10^{6}$	71.31	42.67
21/10	$4.98x10^{-4}$	$1.88x10^{-10}$	$2.64x10^{6}$	70.03	46.67
14/10	$5.50x10^{-4}$	$1.67x10^{-10}$	$3.30x10^{6}$	68.97	57.33
07/10	$7.04x10^{-4}$	$1.38x10^{-10}$	$5.10x10^{6}$	70.76	73.33

band gap channel films. The quantum confinement will become stronger when keeping shortening H_{fin}. Thus, the I_{OFF} reduction with shortening H_{fin} is getting considerable. Because of the larger channel resistance, the shorter W_{eff}, and the smaller region of low conduction band energy, I_{ON} also decreases with shortening H_{fin}. For the devices with W_{fin} = 10 nm and the same calibrated threshold voltage (V_{th}) of 160 mV, the electrical characteristics with respect to various H_{fin} are listed in Table II, where I_{ON} and I_{OFF} are normalized by their individual W_{eff}.

Device with short H_{fin} shows large current ratio, but the drain-induced barrier lowering (DIBL) is worse owing to the large difference of the conduction band energy between the device applying high and low drain bias voltage. DIBL is also known as surface punch-through. As drain voltage enhances, the lateral electric field increases resulting in increasing subthreshold current and decreasing V_{th}. By observing the current density of devices with H_{fin}= 7 and 35 nm at V_G= 0.8 V and V_D= 0.05 and 0.8 V, as show in Fig. 7, device with short H_{fin} has the large difference of current density. The magnitude of SS has no significant changes with H_{fin} variation. Thus, to design the device channel, we examine the DIBL and I_{OFF} versus H_{fin}, as shown in Fig. 8. DIBL decreases with heightening H_{fin}; nevertheless, I_{OFF} increases with heightening H_{fin}. There is a tradeoff between DIBL and I_{OFF}; as a result, a proper value of H_{fin}, which is between 14 and 21 nm, can be found based on the results of device simulation.

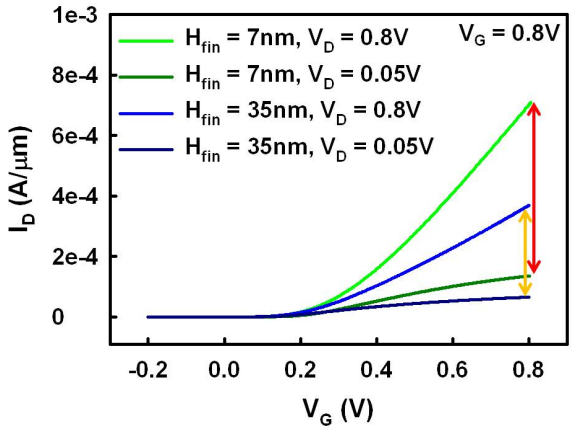

Fig. 7. Normalized current densities of the device with H_{fin} = 7 and 35 nm at V_G= 0.8 V and V_D= 0.05 and 0.8 V. Device with H_{fin} = 7 nm has the large difference indicating that device will suffer the large DIBL effect.

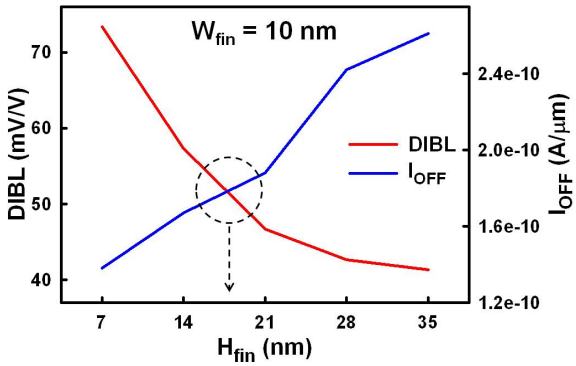

Fig. 8. Tradeoff plot of DIBL and I_{OFF} versus H_{fin} with W_{fin} = 10 nm. DIBL decreases with heightening H_{fin}, but I_{OFF} increases with heightening H_{fin}. As a result, an optimal value of H_{fin} between 14 to 21 nm can be found.

IV. Conclusions

In summary, we have studied the impact of W_{fin} and H_{fin} variation on 14-nm-gate InGaAs tri-gate MOSFET devices. The transport property is governed by W_{eff}, channel resistance, and quantum confinement. Device with W_{fin} = 10 nm has the largest current ratio. The tradeoff plot of DIBL and I_{OFF} indicates a proper region for selecting H_{fin}. To achieve the superior DC characteristic, the stronger quantum confinement, and the better suppression of SCEs, device with W_{fin} = 10 nm and H_{fin} between 14 and 21 nm could be adopted. We are currently study the effects of layer composition with the optimal settings of the device channel.

References

[1] C.-S. Shin, W.-K. Park, SH. Shin, YD. Cho, DH. Ko, T.-W. Kim, D.H. Koh, HM. Kwon, R. J. W. Hill, P. Kirsch, W. Maszara, and D.-H. Kim, "Sub-100 nm Regrown S/D Gate-Last $In_{0.7}Ga_{0.3}As$ QW MOSFETs with $\mu_{n,eff}$ > 5,500 cm^2/V-s," VLSI Symp. Tech. Dig., pp. 1-2, Jun. 2014.

[2] Y. Xuan, Y. Q. Wu and P. D. Ye, "High-performance inversion-type enhancement-mode InGaAs MOSFET with maximum drain current exceeding 1A/mm," IEEE Electron Device Lett., vol. 29, pp. 294-296, Apr. 2008.

[3] J. A. del Alamo, "Nanometre-scale electronics with III-V compound semiconductors," Nature, vol. 479, no. 7373, pp. 317–323, Nov. 2011

[4] M. Radosavljevic, B. Chu-Kung, S. Corcoran, G. Dewey, M. Hudait, J. Faste-nau, J. Kavalieros, W. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, W. Rachmady, U. Shah, and R. Chau, "Advanced high-k gate dielectric for highperformance short-channel $In_{0.7}Ga_{0.3}As$ quantum well field effect transistors on silicon substrate for low power logic applications," IEEE IEDM Tech. Dig., pp. 319-322, Dec. 2009.

[5] I.-H. Ahn and H. Joung, "Band Structure Dependence of Electron Mobility in Modulation-Doped Lattice-Matched InAlAs/InGaAs/InAlAs Heterostructures," Jpn. J. Appl. Phys., vol. 49, p. 084303, Aug. 2010.

[6] D.-H. Kim, T.-W. Kim, RH. Baek, P. D. Kirsch, W. Maszara, J. A. del Alamo, D. A. Antoniadis, M. Urteaga, B. Brar, HM. Kwon, C.-S. Shin, W.-K. Park, Y.-D. Cho, SH. Shin, DH. Ko and K.-S. Seo, "High-Performance III-V devices for future logic applications," IEEE IEDM Tech. Dig., pp. 578-581, Dec. 2014.

[7] T.-W. Kim, H.-M. Kwon, S. H. Shin, C.-S. Shin, W.-K. Park, E. Chiu, M. Rivera, J. I. Lew, D. Veksler, T. Orzali, and D.-H. Kim, "Impact of H_2 High-Pressure An-nealing onto InGaAs Quantum-Well Metal-Oxide-Semiconductor Field-Effect Transistors with Al_2O_3/HfO_2 Gate Stack," IEEE Electron Device Lett., vol. PP, no. 99, pp. 1-3, Jun. 2015.

[8] D. Hisamoto, W.-C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T.-J. King, J. Bokor, and C. Hu, "FinFET-A Self-Aligned Double-Gate MOSFET Scalable to 20 nm," IEEE Trans. Electron Devices, vol. 47, no. 12, pp. 2320-2325, Dec. 2000.

[9] Y. Li, and H.-M. Chou, "A Comparative Study of Electrical Characteristic on Sub-10 nm Double Gate MOSFETs," IEEE Trans. Nanotechnol., vol. 4, no. 5, pp. 645-647, Sep. 2005.

[10] M. Radosavljevic, G. Dewey, J. M. Fastenau, J. Kavalieros, R. Kotlyar, B. Chu-Kung, W. K. Liu, D. Lubyshev, M. Metz, K. Millard, N. Mukherjee, L. Pan, R. Pillarisetty, W. Rachmady, U. Shah, and R. Chau, "Non-Planar, Multi-Gate InGaAs Quantum Well Field Effect Transistors with High-K Gate Dielectric and Ultra-Scaled Gate-to-Drain/Gate-to-Source Separation for Low Power Logic Applications," IEDM Tech. Dig., pp. 6.1.1-6.1.4, Dec. 2010.

[11] S. Tewari, A. Biswas, and A. Mallik, "Impact of Different Barrier Layers and Indium Content of the Channel on the Analog Performance of InGaAs MOSFETs," IEEE Trans. Electron Devices, vol. 60, no. 5, pp. 1584-1589, May 2013.

[12] J. Mo, E. Lind, and L.-E. Wernersson, "InP Drain Engineering in Asymmetric InGaAs/InP MOSFETs," IEEE Trans. Electron Devices, vol. 62, no. 2, pp. 501-506, Feb. 2015.

[13] Y. Li, S.-M. Yu, J.-R. Hwang, and F.-L. Yang, "Discrete Dopant Fluctuations in 20-nm/15-nm-Gate Planar CMOS," IEEE Trans. Electron Devices, vol. 55, pp. 1449-1455, Jun. 2008.

[14] S. Odanaka, "Multidimensional discretization of the stationary quantum drift-diffusion model for ultrasmall MOSFET structures," IEEE Trans. Comput.-Aided Des. Integr. Circuits Syst., vol. 23, no. 6, pp.837-842, Jun. 2004.

[15] R. E. Nahory, M. A. Pollack, W. D. Johnston Jr., and R. L. Barns, "Band Gap Versus Composition and Demonstration of Vegard's Law for $In_{1-x}Ga_xAs_yP_{1-y}$ Lattice Matched to InP," Appl. Phys. Lett., vol. 33, pp. 659-661, Oct. 1978.

[16] F. Xue, A. Jiang, H. Zhao, Y.-T. Chen, Y. Wang, F. Zhou, and J. Lee, "Sub-50-nm $In_{0.7}Ga_{0.3}As$ MOSFETs with Various Barrier Layer Materials," IEEE Electron Device Lett., vol. 33, no. 1, pp. 32-34, Jan. 2012.

[17] C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, "A Physically Based Mobility Model for Numerical Simulation of Nonplanar Devices," IEEE Transactions on CAD, vol. 7, no. 11, pp. 1164-1171, Nov. 1988.

[18] M. N. Darwish, J. L. Lentz, M. R. Pinto, P. M. Zeitzoff, T. J. Krutsick, and H.-H. Vuong, "An Improved Electron and Hole Mobility Model for General Purpose Device Simulation," IEEE Trans. Electron Devices, vol. 44, no. 9, pp. 1529-1538, Sep. 1997.

[19] C. Canali, G. Majni, R. Minder, and G. Ottaviani, "Electron and Hole Drift Velocity Measurements in Silicon and Their Empirical Relation to Electric Field and Temperature," IEEE Trans. Electron Devices, vol. 22, p. 1045V1047, Nov. 1975.