Impact of Backplane Configuration on the Statistical Variability in 22nm FDSOI CMOS

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***Abstract*—In this paper, using variation aware device simulation, we study the local device variability and mismatch as affected by statistical variation resulting from differing backplane doping options in fully depleted SOI transistors. It is seen that discrete random doping effects associated with the choice of doping has a direct effect on mismatch, resulting in increased mismatch with larger channel doping. However, it is also seen that increased backplane doping may counter intuitively help to reduce the variability associated with discrete doping due modification of the electrostatic screening of the source/drain extensions.**

Keywords—FDSOI; mismatch; variability; discrete doping

I. INTRODUCTION

Fully Depleted SOI (FDSOI) CMOS technology was introduced by ST at 28nm, offering better scalability and performance compared to conventional 'bulk' CMOS technology and in competition with the FinFET technology introduced by Intel at 22nm. A very important FDSOI advantage is the dramatically reduced local statistical variability (mismatch) compared to bulk CMOS. Tolerance to low channel doping, due to the improved electrostatic integrity, almost eliminates the random discrete dopant (RDD) induced variability, which is the main source of statistical variability in bulk transistors [1, 2]. Better control of short channel effects also reduces the statistical variability associated with Line Edge Roughness (LER) [3]. Thin back oxide (BOX) in combination with different doping in the back plane is expected in the following FDSOI technology generations to improve further the electrostatic integrity and the back bias control and to offer multiple threshold voltage (VT) options for System-on-a-Chip (SoC) applications [4]. In certain cases, channel doping may be re-introduced to allow better VT control and to improve further the electrostatic integrity.

Until now there has been no systematic simulation study of the impact of these technology modification on the statistical variability and mismatch introduced by individual sources of statistical variability, including RDD, LER and Metal Gate Granularity (MGG), or any assessment of the relative importantance of intrinsic sources of variability in affecting mismatch. Such studies are an important step in characterising mismatch with a view to device design optimisation, or in propagating device variability into statistical circuit simulation with a view to device-technology co-optimisation (DTCO).

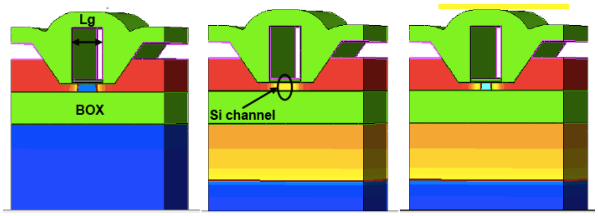

Fig. 1. FDSOI architectures analyzed in this paper: (left) without back-plane, (centre) with back-plane, (right) with back-plane with light doping

In this paper, using advanced 3D statistical TCAD simulations, we study the statistical threshold voltage variability in thin BOX FDSOI transistor suitable for 14nm CMOS technology. Device optimisation is highlighted by investigating three different design options featuring a combination of different choices for channel and back plane doping. The simulations were carried out with the GSS 'atomistic' TCAD simulator GARAND [5] using realistic device structures obtained from Sentaurus Process [6] simulation. The high level of automation available in the GSS tool chain has allowed the efficient simulation of large statistical transistor ensembles. This is necessarily required for accurately deriving threshold voltage variability results. This, in combination with the accurate physical modelling of each of the statistical variability sources in GARAND, has facilitated the analysis not only of the standard deviations of threshold voltage variation but also the shape of the statistical distributions associated with both individual and combined sources of intrinsic variability.

In addition to resolving the distributions of threshold voltages, the analysis of the complete *I-V* characteristics for every device within the statistical ensemble allows the correlation between multiple device figures of merit with respect to each other to be accurately captured. Often this reveals complex correlations not well described by simple principal component analysis. The capability to perform large-scale physical simulations of combined variability sources is a precursor to the extraction of accurate statistical SPICE models [7]. Such statistical SPICE models are in turn required in order to accurately propagate device variability into statistical circuit analysis so that assessment can be made on circuit performance or yield and facilitate co-optimisation.

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II. Simulated Transistors

Three different n-channel device options based upon the the same FDSOI transistor geometry, characteristic of 14nm CMOS technology, are used within this study. The three options are differentiated by their doping, including a reference transistor with no back plane doping, a transistor with back plane doping and an undoped channel, and a transistor with back plane doping and a lightly doped channel. The critical dimensions as well as source/drain and backplane doping, where applicable, are presented in Table 1, while the three FDSOI transistor options are illustrated in Fig. 1.

TABLE I. Device Critical Dimensions

L_G	T_{Si}	T_{BOx}	$N_{S/D}$	N_{BP}
20 nm	5 nm	20 nm	$5x10^{20}$ cm^{-3}	$1x10^{18}$ cm^{-3}

The three simulation domains were provided by accurate process simulation using Sentaurus Process [6]. Drift diffusion device simulation was undertaken using the GSS statistical device simulator GARAND. Quantum corrections are included in all simulations via the solution of the 3D density gradient equation, where the density gradient effective masses were first calibrated to recover the inversion charge distribution as a function of gate bias from a prior 2D Poisson-Schrödinger solution. The Poisson-Schrödinger solution, based upon an effective mass approximation, was obtained for a single cross section through the confined channel. An FDSOI-specific thin Silicon layer mobility model was also included within the GARAND simulations in order to capture the reduction in mobility associated with the small Silicon thicnkesses in these transistors.

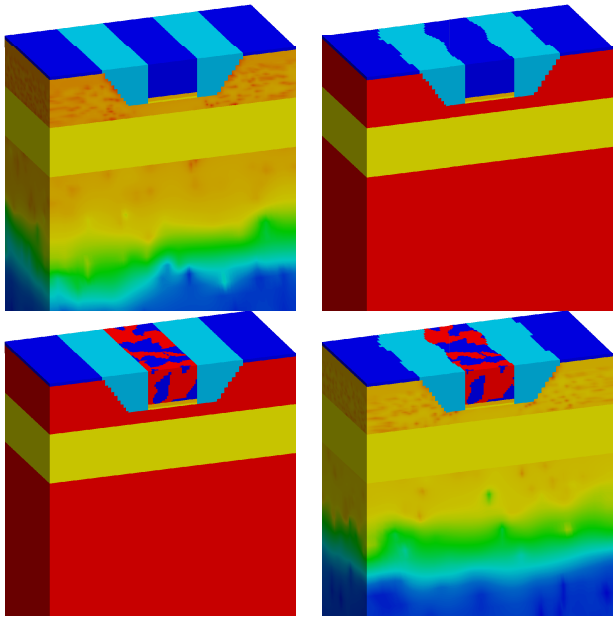

Fig. 2. Garand simulation results showing individual sources of variability: (a) RDD, (b) LER, (c) MGG, and (d) all combined.

In order to assess the statistical distribution of threshold voltage and to gather statistical data on the distribution of device figures of merit, statistical ensembles of 1000 microscopically different transistors were simulated for each of the three technology options. Complete I_DV_G transfer characteristics were obtained in linear and saturation regimes for every device within the ensemble. For each statistical ensemble, sources of intrinsic device variability were included within the simulations both individually and combined together. Such analysis allows the contributions to measured variability from individual sources to be assessed. Simulating combined sources is also vital in order to propoerly resolve effects associated with the physical correlation between sources of variability, which may see variation from one source lead to enhanced sensitivity to variation from another.

Random discrete dopants were considered, which acts as a function of the device doping only, based upon the underlying uniform doping profile provided by the earlier porcess simulation. Metal grain granularity within a TiN metal gate was simulated with average metal gate grain size of 7 nm and two grain orientations with 200mV work function difference and occurring with 40/60% probability. Gate line edge roughness with a 3σ RMS amplitude of 2nm and correlation length Λ=20nm was assumed. Typical results from the 'atomistic' simulations of one transistor from the statistical sample, subject to individual and combined variability sources, are illustrated in Fig. 2, where the impact of the single and combined sources of variability on the electrostatics of the transistor is clearly highlighted.

From the simulated ensemble I_DV_G data, the threshold voltage, as well as additional figures of merit, may be extracted and statistical distributions defined and comparisons made between each of the device options. In addition to simple distributions, the correlation between the extracted device figures of merit may also be defined. These distributions are essential targets for later SPICE model extraction and verification [7].

III. Simulation Results

Fig. 3 depicts the statistical threshold voltage distributions for the different technology options extracted from simulation of the individual and combined sources of device variability. The figure lists four quantile-quantile plots that are related to the threshold voltage cumulative distribution function. In this representation, a Gaussian distribution is idenfitied by a straight line and the best-fit Gaussian distributions to each measued distribution is shown as the red dashed lines. The standard deviation is represented by the slope, with narrowly dispersed data having a larger gradient. The mean is seen as the location of the midpoint of the data. Deviation form the Gaussian reference line represents departure from Normality, highlighting skewness and kurtosis in the measured distribution.

From Fig. 3, some interesting observations can be made. From the RDD only enduced variability: counter intuitively the presence of a back plane is seen to reduce the RDD variability when considering the two cases without channel doping. Considering the 'No back plane' curve as the reference, the includion of backplane doping in the 'Back plane clean' case is

seen to cause a shift in the threshold voltage as well as a slight increase in the gradient of the distribution, indicating more narrowly dispersed data and hence the reduced threshold voltage variability. The variation in this case comes primarily from the variation in the source and drain extensions, since there is little channel doping and because the backplane doping is physically isolated from the active region by the buried oxide. However, the reduction in the depletion layer thickness associated with the back plane doping helps to reduce the effects of discrete dopants due to enhanced screening of the RDD potential in the extensions from the mobile charge in the back plane.

Adding doping in the channel is seen in the 'Back plane' case to naturally increases the RDD variability by providing additional variation sources. This is also seen to cause the threshold voltage distribution to deviate significantly from a Gaussian distribution. The 'Back plane' distribution is seen to show skewness, owing to the relatively small mean number of dopants within the channel. This additionally indicates that methods that assume a Gaussian varaition *a priori* will not accurately capture the device variability.

When considering line edge roughess, as seen in the LER plot in Fig. 3, the effects of LER are seen to be comparable to RDD without channel doping in all cases. The presence of a back plane indicates a slight reduction in short channel effects and hence a slight reduction in the variability associated with gate length variation.

MGG variability is seen as the single greatest contributor to threshold voltage variation as it consistently has the largest dispersed data. The gradient of the distributions for each device option ensemble indicates that the enduced threshold voltage variation is barely affected by back plane and channel doping configuration.

The combined sources of variability show distributions that are dominated by the variance associated with MGG variation but show signs of the skew associated with RDD variation. RDD variation is also seen in the increased thrshold voltage variation associated with the lightly doped channel option. It is again important to note that the multiple distributions may not simply be combined independently as variation from one source modifies the sensitivity to variation from another. For example, variation in metal grains modifies the surface potential which in turn alters the screening and effect associated with local variations in discrete impuries.

Fig. 4 illustrates the correlations (or more accurately the de-correlation) between the important transistor figures of merit, $V_{T\,lin}$, $V_{T\,sat}$, $I_{D\,lin}$, $I_{D\,sat}$ and DIBL. Such de-correlations are well documented in measurements [7] and are critically important in low power SRAM design. Such complex correlations need to be considered when including variability in Monte Carlo circuit analyses in order that the distribution of expected performances in different modes of operation are correctly preserved. It is worth mentioning that the impedance-field approach used in other TCAD tools, which is essentially a perturbation approach [8], cannot capture such de-correlations and does not allow the simulation of combined variability sources.

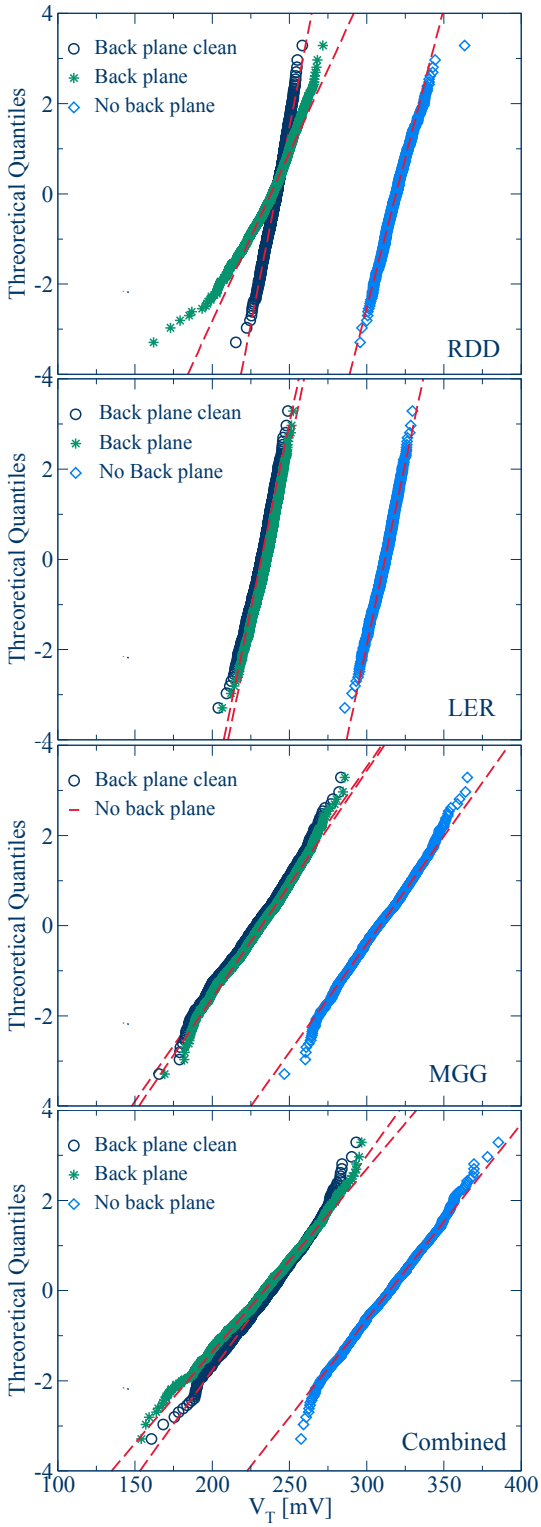

Fig. 3. Comparison of threshold voltage distributions for the three architectures studied in this paper for individual sources of variability, RDD, LER and MGG, as well as combined.

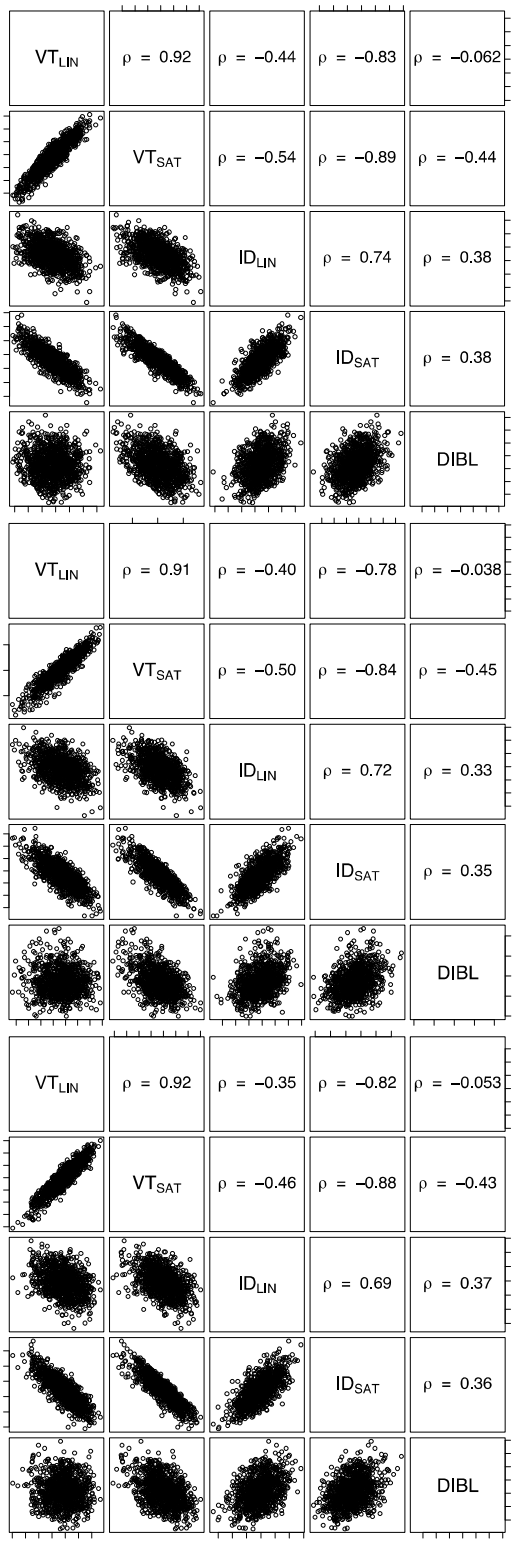

Fig. 4. Correlation plots between the key figures of merit for the total variability for (top) no backplane, (middle) backplane and (bottom) backplane with light channel doping.

IV. Conclusions

Statistical simulations of intrinsic device variability were performed in order to assess the impact on an n-channel FDSOI structure suitable for the 14nm technology generation. Random discrete dopants, line edge roughness and metal grain granularity were considered in isolation and in combination. The impact of the variability sources on threshold voltage was investigated for varying device options, considering devices with and without backplane doping and with and without light channel doping. As expected, a significant increase in threshold voltage variation was seen with the inclusion of light chanel doping, while however a slight reduction due to enhanced screening of dopants in the source / drain extensions was seen when inlcuding backplane doping. The excellent short channel effects in such devices is seen through the little sensitivity to device options when considering gate edge roughness, though there is a small improvement when including backplane doping. The correlation of devcie figures of merit

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