Advanced TCAD Simulation of Local Mismatch in 14nm CMOS Technology FinFETs

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***Abstract*— Local statistical variability (mismatch) is very important in advanced CMOS technologies critically affecting, among others, SRAM supply and holding voltages, performance and yield. TCAD simulation of statistical variability is essential for identification of variability sources and their control in the technology development and optimization. It also plays an important role in the development of accurate statistical compact models for SRAM design, statistical standard cell characterization and statistical circuit simulation and verification. In this paper we compare the TCAD simulation results of statistical variability in 14nm CMOS FinFET technology with Silicon measurements in order to understand the relative role of key statistical variability sources, to assist the technology optimization and to generate target characteristics for statistical compact model extraction.**

Keywords—14nm technology, FinFET, variability, DTCO

I. INTRODUCTION

Tri-gate devices, like the FinFET, are now widely used at the 14nm technology generation and below. FinFET [1] process flow can re-use many integration steps from planar CMOS, while providing better electrostatic integrity relative to planar FETs, owing to tighter control of the channel potential by multiple gates wrapped around the body. This translates to excellent short-channel effects (SCE), low-leakage, and high performance devices. In order to perform timing analysis for multi-gate devices accurately and to determine the most efficient knobs for optimization, it is essential to model and capture the physical behaviour of the devices accurately. This paper presents a full 3D FinFET process/device modelling flow where the impacts of dopant implantation/annealing on relevant device characteristics such as electrostatic control and Vth mismatch (MM) are addressed at device geometries relevant to 14nm technology.

II. TECHNOLOGY DESCRIPTION

In this paper we have simulated state of the art 14nm FinFET 'gate last' technology transistors, which are described in detail elsewhere [1][2][3]. This technology incorporates a raised S/D is used for both n- and p-FinFETs and the p-FinFET incorporates eSiGe channel stressor [4] and a triple-well implant scheme. The device channel doping profiles have been designed to achieve high drive and low leakage current including halo/extension implants with an optimal thermal budget. NFET and PFET logic devices have been used as a basis for uniform device calibration of TCAD simulations, while mismatch which is of significant importance in SRAM has been simulated using Pull-Up (PU) and Pull-Down (PD) devices whose device dimensions are given in Table I. TEM micrographs of both the n and p-type devices are shown in Fig. 1, and the critical FinFET dimensions for both the logic and SRAM devices in this technology are listed in Table I.

TABLE I
DEVICE CRITICAL DIMENSIONS

	Logic	**SRAM**
H_{fin}(nm)	36	36
W_{fin}(nm)	9	9
Taper Angle (°)	86	86
W (nm)	75	75
L_G (nm)	20	38
Vdd	0.9	0.9

In order to explore the use of simulation in technology optimization, 4 process splits have been modelled. These splits, whose parameters are given in Tab. III, are used to investigate the electrostatic control of these bulk FinFETs and their threshold voltage as well as the impact on Vt mismatch. Indeed, due to the application of ultra-shallow junctions (USJ), the FinFET channel doping achieved with different doses allows Vtsat modulation vs. dose as shown in Table III.

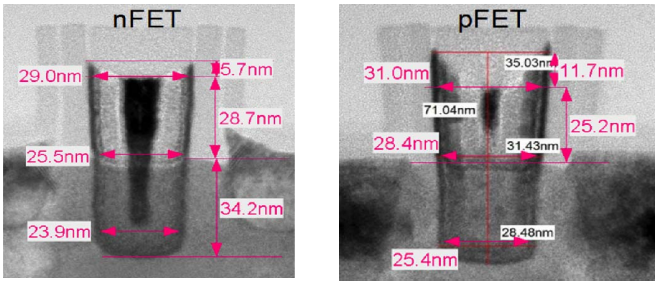

Figure 1: TEM Images of the NMOS (left) and PMOS (right) devices

A. TCAD Simulation Setup and Calibration

A 3D device simulation structure has been constructed based on transmission electron microscopy (TEM) images, providing a realistic simulation domain for dopant implantation and annealing simulations. Monte Carlo implantation models are used in Sentaurus process [6] to accurately simulate the ultra-shallow junction profiles and to account for point defect generation and damage accumulation. Comprehensive 3D

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process simulation then is used to model the experimental results obtained from the investigated process splits described in Table III. The device structures and the 3D doping profiles generated from the process simulations are transferred to the GSS Garand simulator [7] followed by comprehensive calibration to match the electrical behaviour of the simulation to available experimental measurement data. Fig. 2 shows the calibrated simulation to silicon measurements for the reference NFET and PFET and demonstrates the accuracy of the simulation data obtained from comprehensive calibration of both doping profiles and electrical simulation parameters.

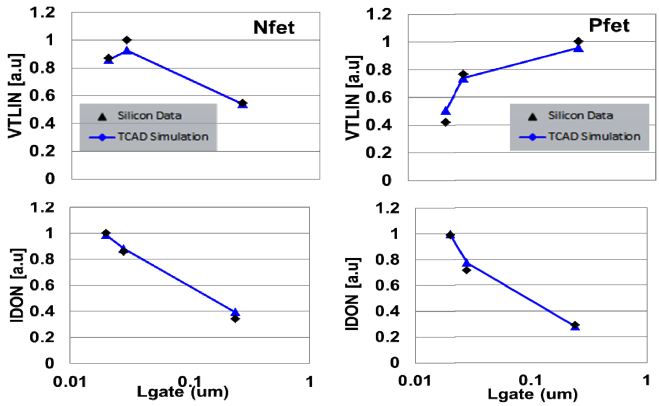
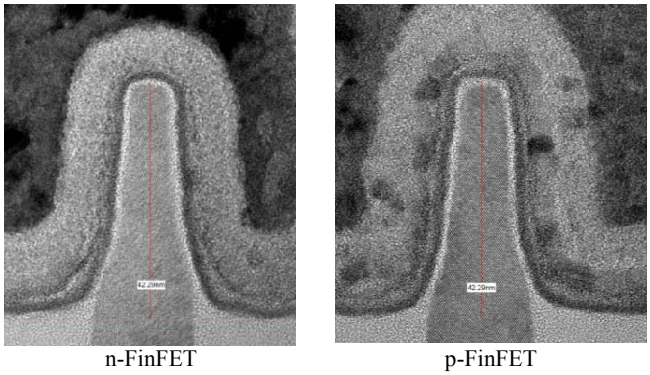


Figure 2: TCAD calibration for n-type and p-type bulk FinFET threshold voltage roll-off and on-current characteristics vs. Lg.

TABLE II
VARIABILITY PARAMETERS

Source	NMOS	PMOS
RDD	Yes	Yes
FER	σ=0.18nm λ=20nm	σ=0.18nm λ=20nm
MGG	None	⌀ = 10nm ΔWF = 200mV



n-FinFET p-FinFET

Figure 3: TEM images showing metal gate granularity.

B. Statistical Variability

GARAND has been designed to provide accurate physical simulation of both the individual and combined variability sources which affect FinFETs [8] including Random Discrete Dopants (RDD) , Fin Edge Roughness (FER) [10], Gate Edge Roughness (GER) [11] and Metal Gate Granularity (MGG) [12] The impact of the combined sources of variability have been simulated using the physical parameters given in Table II. This simulation of combined variability sources is essential to provide accurate and predictive variability assessments and for the generation of target statistical I-V characteristics for statistical compact model extraction and statistical circuit simulations which are necessary in a true Design Technology Co-optimisation (DTCO) flow.

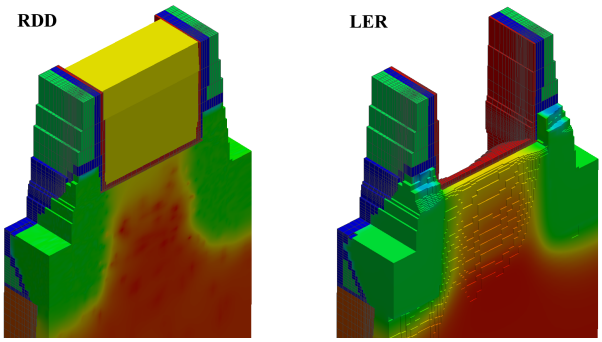
As shown in Fig. 3 the gate of the n-FinFETs are poly-amorphous whereas the p-FinFET gate shows distinct metal grains. To validate the variability parameters used and to ensure that the uniform device calibration is valid a comprehensive sensitivity analysis has been performed which compares the mean Vt for each split, and an example of such a sensitivity analysis for one of the PU device splits is shown in Table III.

TABLE III
PROCESS PARAMETERS AND NORMALISED VT SENSITIVITY

SRAM	Process Item	S1	S2	S3	S4
PU	Vt adjust dose [cm^{-2}]	0	1e13	4e13	6e13
PD	Vt adjust dose [cm^{-2}]	0	1e13	3e13	6e13
FOM	**Type**	**S1**	**S2**	**S3**	**S4**
VtSat	Experiment (ET)	0.967	1.033	1.196	1.285
VtSat	TCAD	0.952	1.022	1.154	1.220
VtLin	Experiment (ET)	1.000	1.081	1.249	1.330
VtLin	TCAD	1.015	1.086	1.217	1.282

III. RESULTS

Variability simulations using the parameters given in Table II have been carried out for the 4 process splits and in each case an ensemble of 1000 statistical devices has been simulated. The impact of the individual and combined sources of variability on the potential profile of an example device are illustrated in Fig. 5.



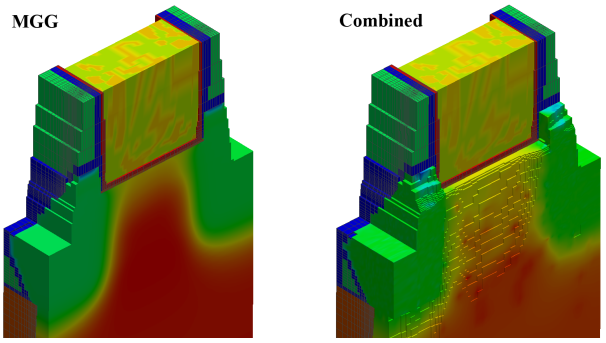


Figure 4: Example 3D potential distributions obtained from simulations of the PU device with individual and combined sources of variability.

The impact of each of the process split conditions on the device mismatch is shown in Figs. 6 and 7 where good agreement is obtained between simulation and measurement. In order to achieve a stable SRAM cell the Pull Up consists of two fins per device. Additionally due to the increaseed effective width of the device, this helps to reduce the local mismatch as depicted in Fig. 6.

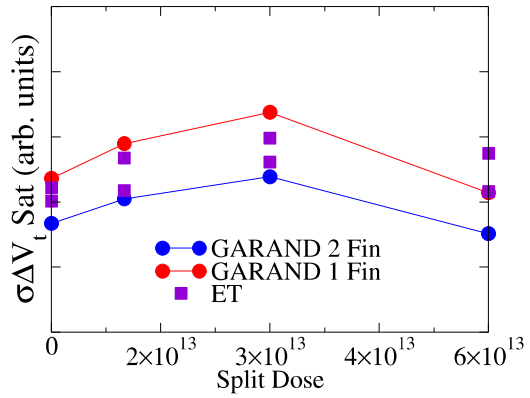


Figure 5: PD device VtSat mismatch. ET shows experimental data.

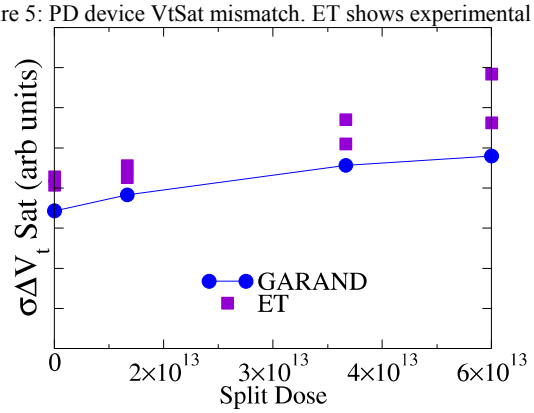


Figure 6: PU device Vtsat mismatch. ET shows experimental data.

Figures 8 and 9 show example plots of the correlations between various device figures of merit (FOM) for both the Pull Up and Pull Down devices of Split 1.

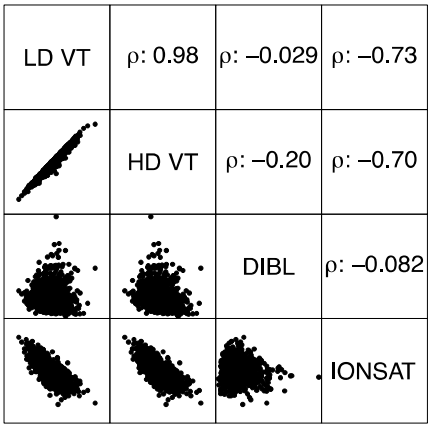


Figure 7: Figure of merit correlation plots for the PD device S1.

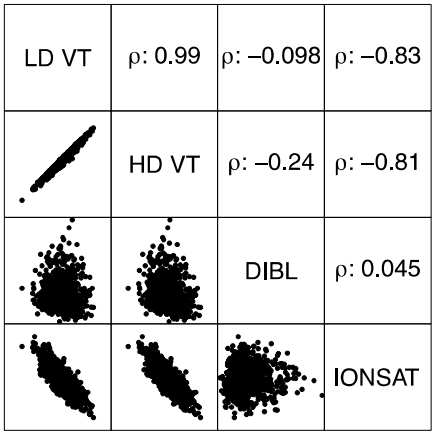
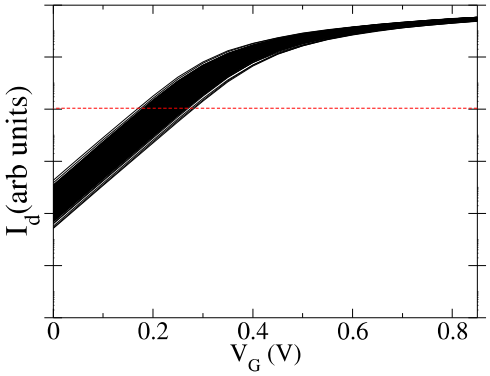


Figure 8: Figure of merit correlation plots for the PU device, S1

It is interesting to note that there are complex correlations between Ion, Vt and DIBL (which is important in SRAM), that can only be accurately obtained via the simulation of all sources of variability in combination. In fact DIBL shows a very strong de-correlation with the other FoM. The impact of the combined sources of variability on the electrical performance of the PD and PU devices for two of the simulated implant splits can be seen in Figs. 11 and 12.



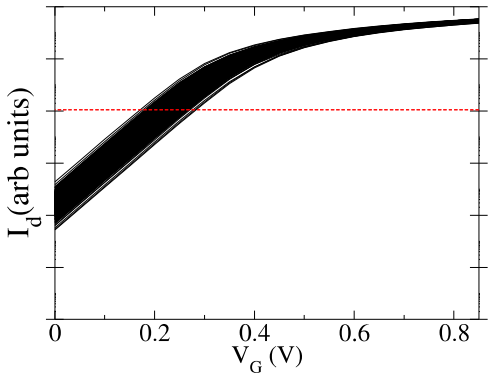


Figure 9: PD Device statistical IdVg characteristics with combined sources of variability for S1 (top) and S4 (bottom)

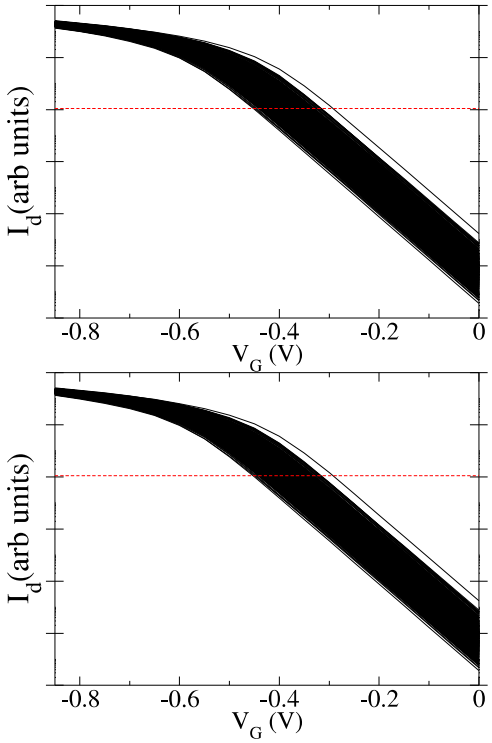


Figure 10: PU Device statistical IdVg characteristics with combined sources of variability for S1 (top) and S4 (bottom).

By performing simulations that include all expected sources of device mismatch, and capturing the inherent correlations and de-correlations between figures of merit, we are in a position to extract compact models that can be used for variability-aware SRAM design. Using the GSS ModelGen technology an unlimited number of compact model cards can be generated that retain the statistical distributions (mean, standard deviation, skew and kurtosis) and the correlations between compact model parameters so that the transistor models used in the SPICE circuit simulation will match the statistical characteristics of the underlying devices that were obtained from the TCAD device simulations [13]. Global variability coming from process variations can also be included to produce a full variability-aware PDK for SRAM design, statistical standard cell characterization and statistical circuit simulation and verification.

IV. Conclusions

Technology scaling presents an abundance of opportunities where TCAD can make significant contributions. In this work, an optimized TCAD process and device simulation strategy for 3D FinFETs is presented. After calibration, the resulting 3D doping profiles correctly predict the short-channel behaviour of the devices for the investigated splits. These calibrated inputs are then used to perform an assessment of FinFET variability improvement. We have presented a simulation methodology that accurately models the effect of combined sources of variability on a state of the art 14nm FinFET technology under a range of process conditions which is essential in order to fully realize the potential of a technology when the impact of mismatch on optimal device design is considered. TCAD is expected to become an essential part of strategy for companies to contain R&D cost and continue timely delivery of new technology nodes. The rapid production of TCAD-based PDKs for SPICE circuit simulations allow rapid investigation of the effect of technology process decisions on circuit design, facilitating a true design-technology co-optimisation (DTCO) [14] that can help minimise the effects of variability on circuit performance by optimising the process design stage for final circuit performance and yield.

References

[1] Henson K., Bu H., Na MH., Liang Y., Kwon U., Krishnan S., et al. International electron devices meeting; December 2008. p.645–48.

[2] Chen X., Samavedam S., Narayanan V., Stein K., Hobbs C., Baiocco C., et al. Symposium on VLSI Technology; 2008. p. 88–9.

[3] A. Keshavarzi, et al., in International electron devices meeting Tech. Dig., 2011, pp. 67-70.

[4] Ghani T., Armstrong M., Auth C., Bost M., Charvat P., Glass G., et al.. International electron devices meeting; December 2003. p. 978–80.

[5] D. Hisamoto, W. C. Lee, J. Kedzierski, H. Takeuchi, K. Asano, C. Kuo, E. Anderson, T. J. King, J. Bokor and C. Hu, IEEE Trans. Electron Devices, 12:2320-2325, 2000.

[6] Synopsys, http://www.synopsys.com

[7] Gold Standard Simulations, http://www.GoldStandardSimulations.com

[8] X. Wang, A. R. Brown, B. Cheng and A. Asenov, International Electron Devices Meeting (IEDM) Technical Digest, pp.5.4.1-5.4.4, Washington, DC, USA, 5-7 December 2011

[9] A. Asenov, , IEEE Trans. Electron Dev.,Vol.45, pp.2505, 1998

[10] X. Wang, B. Cheng, A. R Brown, C. Millar and A. Asenov, Proc. European Solid-State Device Research Conference (ESSDERC), pp.113-116, Denver, CO, USA, 2012

[11] A. Asenov, S. Kaya and A. R. Brown, IEEE Trans. on Electron Devices, Vol.50, No.5, pp.1254-1260, 2003

[12] A. R. Brown, N. M. Idris, J. R. Watling and A. Asenov, IEEE Electron Device Letters, Vol.31, Iss.11, pp.1199-1201, 2010

[13] B. Cheng, X. Wang, A. R. Brown, C. Millar, A. Asenov, J. B. Kuang, S. Nassif, International Conference on Simulation of Semiconductor Processes and Devices (SISPAD), Denver, USA, 2012

[14] A. Asenov, B. Cheng, X. Wang, A. R. Brown, C. Millar, C. Alexander, S. M. Amoroso, J. B. Kuang, S. R. Nassif, IEEE Trans. Electron Devices, Vo. 62, No.6, pp.1682-1690, 2015