A Circuit Model for a Si-based Biomimetic Synaptic Time-keeping Device

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***Abstract*—Spike time dependent plasticity (STDP) is synaptic conductivity modulation which is dependent upon the time difference between pre- and post-synaptic neuronal spikes. Superposition of extended waveforms from pre- and post-synaptic neurons has been proposed to apply a pre- vs. post-neuron spike time difference dependent voltage across an RRAM based synapse to implement STDP. Such long waveforms are power-intensive. We have recently proposed an equivalent synaptic time-keeping based on impact ionization based NPN diode (I-NPN).Here the time difference between *sharp* pre- and post-neuronal spikes enables conductance change due to the internal charge carrier dynamics of I-NPN device. Such an approach is low power and biomimetic. In this paper, we propose a SPICE model of the I-NPN device. The model is able to emulate DC, transient and pulse train response of I-NPN diode. STDP is demonstrated. The SPICE simulations are much faster than TCAD, thus enabling circuit level simulation of neural network. Such a circuit model is essential for the evaluation of the impact of device characteristics on the learning performance of neuromorphic circuits which will provide essential device specification and enable learning efficiency benchmarking.**

I. INTRODUCTION

A synapse connects a pre- and a post- synaptic neuron. Learning consists of modifying synaptic conductance to affect inter-neuronal signal transfer. Thus, the connectivity in the neural network may be reconfigured by synaptic conductance change. Bipolar RRAM based synapse enables such conductance modification [1]. A further requirement is that synaptic conductance change must depend upon the time difference (Δt) between a pre- and post-synaptic neuronal spike known as Spike Time Dependent Plasticity (STDP) (Fig. 1). However, bipolar RRAM devices primarily convert voltage to conductance change. Long waveforms generated by pre- and post-synaptic neurons offset by Δt (Fig. 1a) produce a Δt-dependent peak voltage and consequently a peak current through the RRAM device (Fig. 1b) [1,2,3] to cause a Δt-dependent conductance change that enables STDP. Unfortunately, the long waveforms cause power and speed of learning challenges. We have recently proposed a bio-mimetic approach to STDP based on short neuronal pulses [4] in comparison to long waveforms as noted above.This is based on the impact ionization based n+/i/δp/i/n+ diodes (I-NPN), which have been widely explored [5, 6]. We have shown sub-

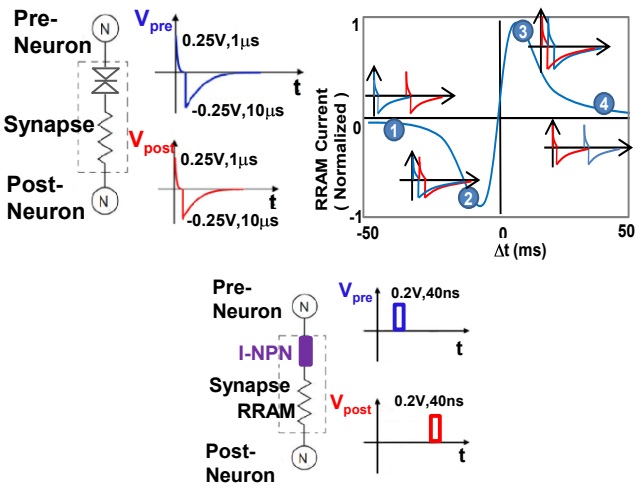

Fig. 1. (a)The synapse is modeled by a bidirectional diode in series with RRAM. Conventional pulsation waveforms scheme used to generate an STDP which uses long duration pulses (1μs-10μs) which limits the rate of spiking.(b) STDP curve generated by the extent of superposition of two waveforms. The resultant voltage across the synapse depends upon the time offset Δt between the waveforms. More the overlap, higher is the programing current flowing through the synapse for programming the RRAM. (c)The new proposed scheme in which synapse is modeled by the I-NPN selector in series with RRAM. The intrinsic turn-on/turn-off time scale of the I-NPN produces spike time correlation dependent current with narrow width (40ns) pulses, thus increasing the spiking rate and learning by 1000x..

0.5V impact ionization experimentally [7] to verify low voltage operation. To enable neural networks with array of synapses, a circuit model essential. In this paper, we represent a SPICE based circuit model for the I-NPN based synaptic timekeeping device.

II. PHYSICAL MECHANISMS OF I-NPN DIODE

The I-NPN device consists of an n+/i/δp/i/n+ doping profile (Fig. 2), where the device operates in punch-through. At zero bias, there is a sufficient barrier height near equilibrium for NPN device to be in the off state (Fig.3a). At low voltage, barrier is modulated to obtain exponential current(Fig. 3b). However, built-in electric field isn't high enough to start impact ionization. At moderate bias, the impact ionization (II)begins.The II-generated electronsare swept away by the built-in electric field as output electron current. The II-

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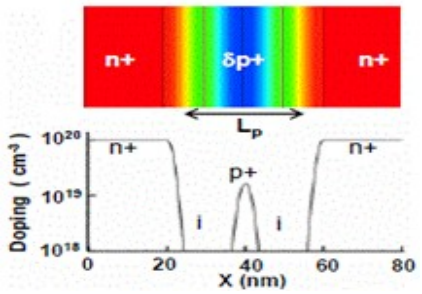

Fig. 2. NIPIN diode structure and doping profile [5]

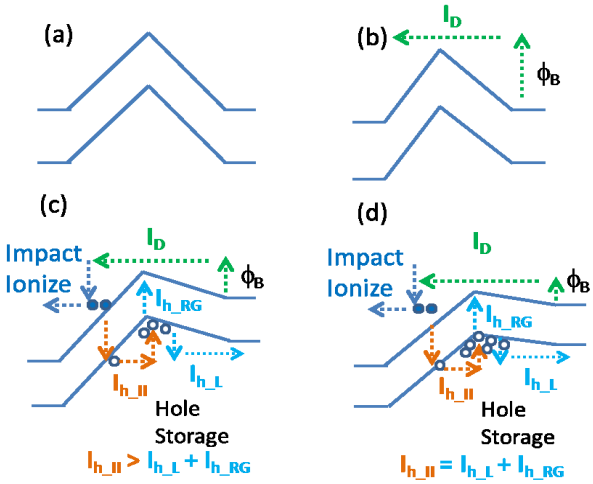

Fig. 3. Band diagram showing (a) equilibrium, (b) Barrier limited current at low input voltages (c) II-generation and trapping of holes in the well with the positive feedback process at high input voltage and (d) steady state is reached when rate of impact ionization hole generation become equal to leakage rate[2]

generated holes, on the other hand, are trapped in the hole-well formed in the p-region (Fig.3c) and reduce the barrier for subsequent electron injection. This produces a positive feedback as when electron current increases, impact ionization increases as well causing an increased hole storage and which further increases electron current.Finally,a steady state(Fig. 3d) is reached when the hole generation process is equal to hole loss process either by recombination or by hole current over the "source" hole barrier out of the hole well[5,7].

III. Equivalent Circuit Model

I-NPN has two regimes: (i) at small applied bias (Vin), the barrier (Φ_B) (Fig. 4a) is lowered by voltage division to get exponential current [5,7]. This is implemented by a voltage divider circuit (Fig. 4b) whose voltage V_a is applied to the gate of the MOSFEToperating in subthreshold region (which is essentially a voltage controlled current source) as shown in Fig. 4 to get exponential collector current (I_C) with Vin. (ii) At higher V_{in}, impact ionization occurs and the generated holes get stored in the p-well which lowers the electron barrier (Fig. 4c), hence current increases. Higher current causes more impact ionization to create a positive feedback. This hole-generation current by Impact Ionization is implemented by a current source (I_{II}) which is defined as follows.

$$I_{II} = (M-1)*I_C \qquad (1)$$

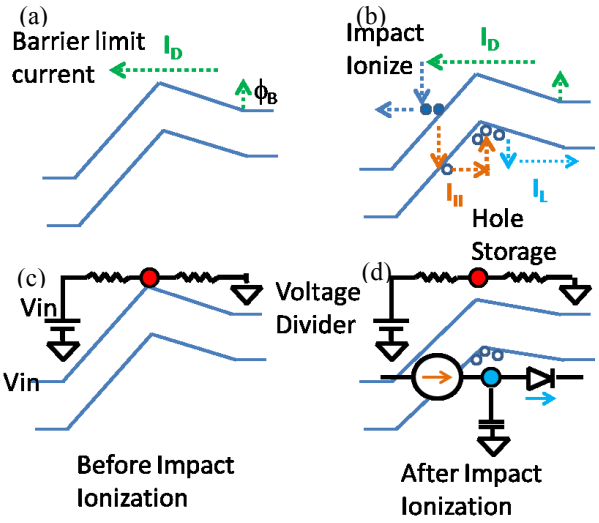

Fig. 4. (a)At low voltage barrier lowering due to punch-through (b) Equivalent voltage divider circuit for barrier modulation. (c) At high voltage, impact ionization based hole storage cause barrier reduction, current increase and further impact ionization (positive feedback) (d) Impact ionization modeled as current source (I_{II})and diode current (I_L)for stored hole loss. Stored holes in the capacitorC1 produce V_b.

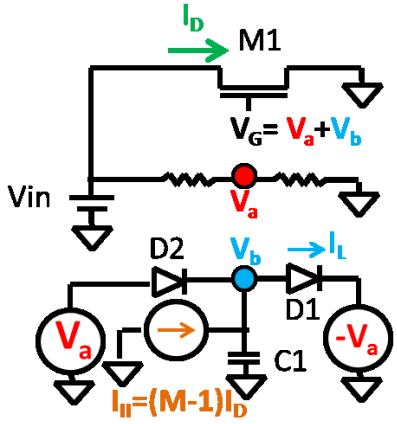

Fig. 5. $V_G = V_A + V_B$ is applied to the gate of MOSFET working in subthreshold region to obtain exponential drain current I_D. Diode D2 ensures without impact ionization V_b=0 for lower voltages

Where $M = 1/(1 - \int ae^{-\frac{b}{E}}dx)$ is the multiplication factor based on a simple model of impact ionization coefficient[8].

For the calculations, electric field is assumed constant in the i-region where impact ionization occurs.The current causing loss of stored holes (I_L) over the source hole barrier is modeled as a diode D1. The net current (I_{II}-I_L) charges a capacitor (C1) to produce a further barrier lowering V_b due to holes stored in the p-region. The diode current I_L depends upon total barrier lowering i.e. $V_G(=V_a+V_b)$. As it already has V_b on one end, a $-V_a$ source is added to the other end to apply the bias dependent barrier lowering. As V_b increases, leakage current increases and multiplication factor decreases. Hence V_b will settle to a voltage such that impact ionization current becomes equal to diode leakage current. A second diode D2 is

added to ensure that without impact ionization V_b=0 for low input voltages. This is physically equivalent to the drain barrier for hole leakage.To obtain exponential current-voltage relationship, $V_G = V_a$(barrier lowering by applied bias) + V_b (barrier lowering by hole storage) is applied to MOSFET M1 operating in subthreshold region. Thus, the circuit elements mimic the main physical mechanisms.

IV. DC AND TRANSIENT RESPONSE

A. DC I-V

Similar to DC I-V by TCAD simulations, I-V by SPICEshows the improved ideality upon enabling impact ionization (Fig. 6a) [4,7]. The structure, doping and Germanium content of I-NPN device determines ideality and the threshold voltage for onset of impact ionization. The SPICE model ideality and the threshold voltage for onset of impact ionization can be engineered by selecting parameters of *M* i.e. *a* and *b* (Fig. 6b).

B. Turn-on/Turn-off Transients

TCAD based turn-on transient is slow initially but shows a sharp turn-on eventually as holes builds up with positive feedback (Fig. 7a) while turn off shows an exponential decay [4,7]. Instantaneous modulations in the turn-on and turn-off transients respectively are because of barrier changes due to voltage division. The SPICE based turn-on and -off transients show similar behavior (Fig. 7b). The turn-on causes the charge up of the capacitor due to the net current between I_{II} and I_L while turn off transient is due to capacitor discharge through the D1 due to I_L. For fixed impact ionization parameters *a* and*b*, leakage diode (D1) saturation current and capacitor C1 can be used for engineering transient properties.

C. Pulse-train response

The TCAD based pulse-train response shows gradual increase of I_D as holes build up during spikes and then partially leaks out during the next low bias part[4]. The SPICE response shows similar gradual current response build up to a pulse train (Fig.8). This demonstrates that the SPICE circuit model is able to capture the salient electrical behavior exhibited by TCAD simulations.

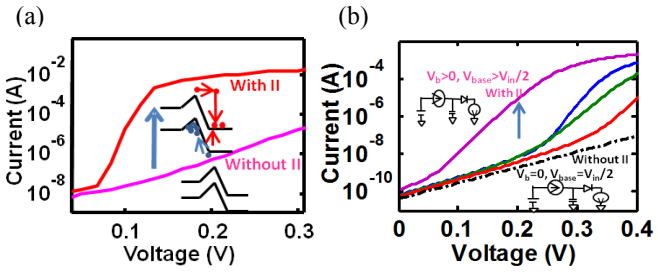

Fig. 6. a) TCAD (b) SPICE I-V characteristics of the device with and without II. TCAD shows ideality improvement with hole storage. SPICE shows ideality improvement with C charge up. Modifying multiplication factor M can engineer ideality

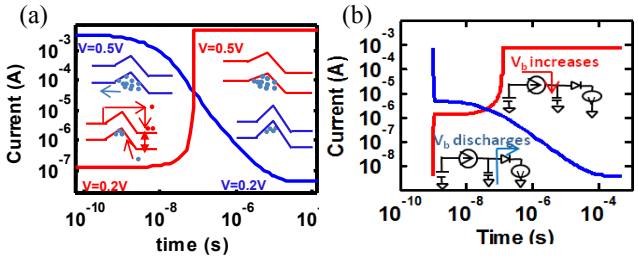

Fig. 7. Simulated turn-on (V_{OFF}→ V_{ON} :red) and turn-off (V_{ON}→ V_{OFF} :blue) transients of the device which depend upon stored hole build up and stored hole escape in the p-region well respectively.(a) TCAD (b)SPICE shows charge discharge of capacitor

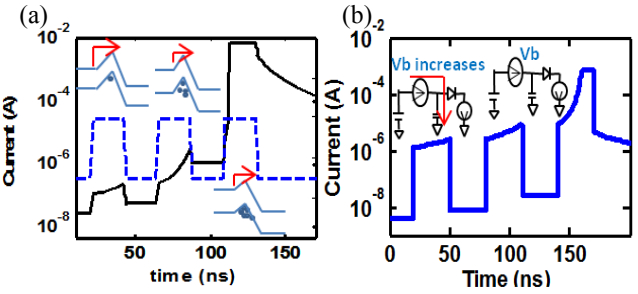

Fig. 8. The response to a pulse train shows increase in stored hole density and the resultant I_D increase by barrier reduction in (a) TCAD (b) SPICE

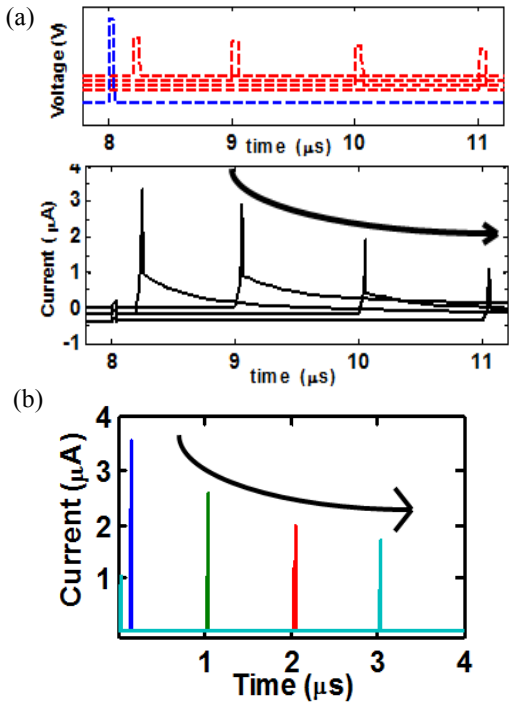

Fig. 9. Effect of spike time difference shows high current for low time difference between pulses a) TCAD- 1st graph corresponds to two input pulses given with different time difference; 2nd graph shows output current for different sets of pulses b) SPICE model: Output current for two pulses with increasing time difference

V. SPIKE TIME DEPENDENT PLASTICITY

The TCAD simulations show that when the spike time difference is small (time difference $<t_{off}$), the stored holes do not get enough time to escape leading to a large I_D response for the second pulse[4]. As the spike time difference increases, the stored holes are reduced and the I_D response to second pulse decreases[4]. The SPICE simulations show the same behavior as it is able to charge up the capacitor during spiking and partially discharge the capacitor based on the time difference. This is the synaptic time-keeping function. Using this time keeping function in series with RRAM device, time difference can be converted to conductance change and hence generating STDP. Based on these features, an STDP learning rule is demonstrated in SPICE and compared to the TCAD results (Fig. 9, 10)

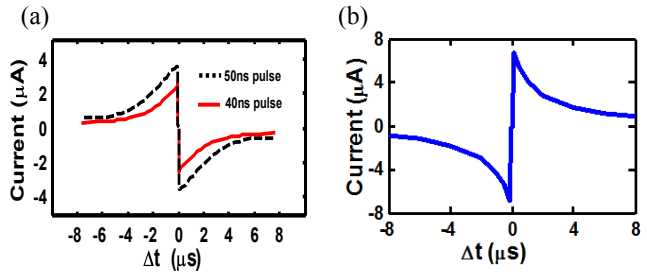

Fig. 10. STDP learning implemented in (a) TCAD and (b) SPICE show essentially similar behavior

VI. CONCLUSION

In this paper, we have presented a simple circuit model for the synaptic timekeeping device based on I-NPN. SPICE (~3s) accelerates simulations by 200× compared to TCAD (600s). The circuit model is able to replicate the key features of TCAD simulations including DC, transient pulse- train response and time keeping properties. Such a circuit model is essential for the evaluation of the impact of device parameter dependence on the learning performance of neuromorphic circuits which will provide essential device specification and enable learning efficiency benchmarking.

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