A physics-based compact model for Fully-Depleted Tunnel Field Effect Transistor

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***Abstract*—Tunnel FETs (TFET) are promising candidates for integration in logic circuits at very low supply voltages. We report here a SPICE compact model that describes all regimes of the TFET transistor. The current contribution from source and drain sides is described by an original set of equations including the electrostatic behavior and the effect of superlinear onset. Finally, this model is implemented using Verilog-A language and compared with TCAD simulations.**

***Keywords*—Compact model, TFET, Tunneling current, Fully-Depleted-Silicon-On-Insulator (FDSOI), SPICE, TCAD.**

I. INTRODUCTION

Traditionally, the downscaling of CMOS technologies improves performance and increase the circuit density. Unfortunately in the most advanced generations, these performances are degraded through the loss of the electrostatic control. In addition, the energy budget necessary per application increases. To overcome these limitations, the Tunnel Field Effect Transistors (TFET) has been developed and studied [1-3]. In theory, this architecture can achieve lower subthreshold slope below the classical MOSFET limit of 60 mV/dec because the local nature of tunneling from the source to the channel provides a better electrostatic control. So, this "Steep-Slope" structure operating with tunnel transport mechanisms is a serious track for ultra-low-power applications.

From physical modeling point of view, some well-known papers [5-6] detail the physics of tunneling and transport properties in TFET. This transistor is a Band To Band Tunneling (BtBt) current switch between source to channel and channel to drain controlled by electrostatic behavior (depending of depletion into channel, source and drain) and corresponding Fermi-Dirac distribution which plays a fundamental role in the superlinear onset of TFET IdVd curve. So our objective is to propose a full analytical dedicated model to Fully-Depleted TFET including this physical aspect to reproduce the particular behavior of tunnel transistor.

The paper is organized as follows: in Section II, we explain the global behavior of the TFET operation and detail the basic analytical equation of electrostatic model. In section III, we present our approach for current and charge modeling and we validate it by comparison with TCAD simulations.

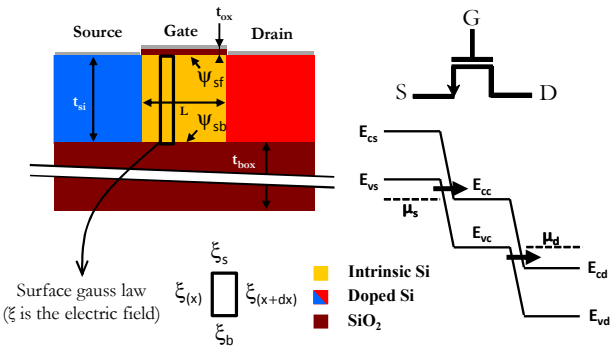

Fig. 1. TFET structure and definition of the main geometrical, electrical and band diagram parameters. ξ is the electric field, E is the energy with corresponding index v for valence band, c conduction band, s for source, d for drain and μ is the Fermi level. Ψ is the surface potential with corresponding index sf for front surface potential and sb for back surface potential.

II. ELECTROSTATIC MODEL: GEOMETRICAL PARTITIONING

A. Position of the problem

The considered basic TFET structure and geometrical definition are described on figure 1; the source and drain are heavily doped at $N_{sd}=10^{20}$ cm^{-3} and the channel is intrinsic at $N_a=10^{15}$ cm^{-3} with abrupt junctions which are aligned with gate edges. In fact, TFET behavior is based on the variation of depletion widths along the structure which is the cause of band bending for tunneling windows at source to channel and channel to drain (represented by arrow on band diagram in inset of figure 1). Thus, our electrostatic model is built on a conceptual description based on geometrical partitioning: the depletion widths into the source and/or the drain (L_d) and the depletion widths into the channel (W_d). Figure 2 illustrates schematically the charge sharing for 2 different TFET operations: $V_{GS}>>0$ for $V_{DS}>0$ (figure 2.a) and $V_{GS}>>0$ for $V_{DS}>0$ (figure 2.b).

As already explained in reference [6] for Double-Gate transistor, the total charge is the sum of the corresponding inversion charge into the channel and depletion charge due to source depletion. In the first case (figure 2.a) the positive gate voltage combined to positive drain voltage suggests both depletion into source and channel. The quasi-Fermi level into the inversion layer part is constant and the relative charge is normalized to the depletion width into the channel. In the same way (figure 2.b), the negative gate voltage combined to

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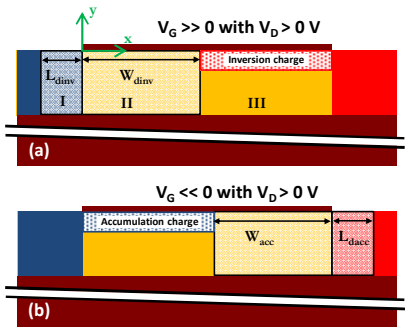

Fig. 2. Schematical reprensetation of depletion widths for positive V_{GS} (a) and negative V_{GS} (b). This figure is purely conceptual.

positive drain voltage suggests both depletion into drain and channel with the same behavior on capacitance. Note that the variation of channel/source depletion widths is not constant along the depth of the channel, nevertheless to simplify our approach we consider à constant depletion along the depth.

The electrostatic model is built using a similar approach to [6]. For this, the surface potential in inversion is calculated as in the LETI-UTSOI model dedicated to undoped Fully-Depleted transistors [7] and adapted here for the tunnel transistor. The following assumptions are performed on the surface potential calculation along the channel, we consider: fixed charges in the source and drain (parabolic potential in the source), depletion potential into the channel by applying Gauss's law (region II of figure 2.a) and rest of the channel in inversion (region III of figure 2.a). Thus, the basic boundary conditions between region I, II and III are:

$$\psi_I(-L_{dinv}) = -\phi_s \;\&\; \frac{d\psi_I(-L_{dinv})}{dx} = 0 \tag{1.a}$$

$$\psi_I(0) = \psi_{II}(0) \;\&\; \frac{d\psi_I(0)}{dx} = \frac{d\psi_{II}(0)}{dx} \tag{1.b}$$

$$\psi_{II}(W_{dinv}) = \psi_{sf} \;\&\; \frac{d\psi_{II}(W_{dinv})}{dx} = 0 \tag{1.c}$$

$$\frac{d^2\psi_{II}(x)}{dx^2} = \frac{q.N_{sd}}{\varepsilon_{si}} \tag{1.d}$$

where ψ_i is the potential and i=I,II or III corresponds to the region number or i=sf or sb corresponds to front surface potential or back surface potential, q is the electron charge, ε_{si} the silicon permittivity and ϕ_s is the built in voltage.

B. Depletion width calculation

The description of the core equation for electrostatic model is detailed here only in the case of figure 2.a. Thanks to first approximation and eq. (1.d), the potential into the source (region I) is equal to:

$$\psi_I = a.x^2 + b.x + c \tag{2}$$

where a, b and c are constant determine with boundary condition. We applied the gauss law theorem [8] on the silicon film in region II (surface Gauss law is represented on figure 1). After some algebraic manipulations, the potential in region II is:

$$\psi_{II} = C_{II1}.e^{m.x} + C_{II2}.e^{-m.x} - \frac{R}{m^2} \tag{3.a}$$

$$m = \sqrt{(\eta/\varepsilon_{si}.t_{si}).(C_{ox} - \alpha_c.C_{box})} \tag{3.b}$$

$$R = (\eta/\varepsilon_{si}.t_{si}).\begin{pmatrix} q.Na.tsi - C_{ox}.(V_{GS} - V_{FBf}) \\ + C_{box}\cdot(V_{GS} - V_{FBb}) \end{pmatrix} \tag{3.c}$$

where C_{II1} and C_{II2} are constant determine with boundary condition, C_{ox} is the oxide capacitance, Csi is the film capacitance and C_{box} is the box capacitance. η is the fitting parameter that includes the effect of lateral field variation in the depleted film [8]. The inversion region III is described by the surface potential adapted to our problem (for more information see reference [7]). The main assumption is the relation between front and back surface potential which consider depletion in back interface:

$$\psi_{sb} = \alpha_c \cdot \psi_{sf} + \varepsilon \tag{4.a}$$

$$\alpha_c = C_{si}/(C_{si} + C_{box}) \;\&\; \varepsilon = C_{box}/(C_{si} + C_{box}) \cdot V_{GB} \tag{4.b}$$

After some algebraic manipulations and using equations (1-3), we obtain the key equation to solve the system:

$$A.[sh(m.W_{dinv})]^2 - B.ch(m.W_{dinv}) + C = 0 \tag{5.a}$$

$$A = m^2.\varepsilon_{si}.\left(\psi_{sf} + (R/m^2)\right)^2/(2.q.N_{sd}) \tag{5.b}$$

$$B = \left(\psi_{sf} + (R/m^2)\right) \tag{5.c}$$

$$C = \left((R/m^2) - \phi_s\right) \tag{5.d}$$

By solving equation (5.a) and several mathematical manipulations, we obtain an analytical solution of depletion widths into the channel (W_{dinv}) and then source side (L_{dinv}):

$$W_{dinv} = \frac{1}{m^2}.\ln\left[\frac{1}{2.A}.\begin{pmatrix} B + .\sqrt{\Delta} \\ + \sqrt{2}.\sqrt{B^2 - 2.A.C + B.\sqrt{\Delta}} \end{pmatrix}\right] \tag{6.a}$$

$$\text{with } \Delta = 4.A^2 - 4.C.A + B^2$$

$$L_{dinv} = -\varepsilon_{si}.m.\frac{\psi_{sf} + \dfrac{R}{m^2}}{2.q.N_{sd}}.\left(e^{-m.W_{dinv}} - e^{m.W_{dinv}}\right) \tag{6.b}$$

As mentioned earlier, these solutions (eq. 6.a and 6.b) are only valid for positive gate voltage. Thus, to have a continuous model, we limit the channel depletion widths calculation at 0V with smoothing function. In the same way, the source depletion is also calculated thanks to this approximation and limited to zero for negative V_{GS}.

Figure 3 shows the results of analytical solution proposed here. In accordance with the TFET behavior, when $V_{GS}>0$ (electron charge growing): the depletion width into the channel decreases ($W_d=W_{dinv}$ fig. 3.a), source depletion increases ($L_d=L_{dinv}$ fig. 3.b) and are modulated by the V_{DS} value. Note that the strong variation of W_{dinv} with V_{DS} for high V_{GS} value is directly linked to the quasi-Fermi level variation of the inversion charge which is linearly proportional to drain potential. The analytical model predicts a smooth increase of W_{dinv} with $V_{GS}<0$, nevertheless this variation is not physic because we do not have inversion charge into the channel. As describe earlier and due to technical consideration, this smoothing function is well adapted for capacitance calculation avoiding any discontinuity on whole V_{GS} range. Note that L_{dinv} is not equal to 0 when $V_{GS}=0V$ because of the building voltage at the source to channel junction.

In the same way, when $V_{GS} < 0$ (hole charge growing): $W_d=W_{dacc}$ decreases (fig. 3.c) and $L_d=L_{dacc}$ increases (fig. 3.d) and are modulated by V_{DS} value. Again as L_{dinv}, L_{dacc} is not equal to 0 when $V_{GS}=0V$ which is influenced by the building voltage plus V_{DS} potential at the channel to drain junction.

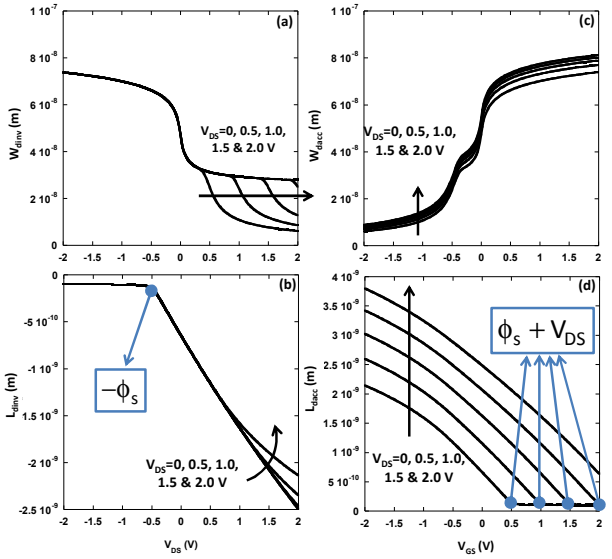

Fig. 3. Illustration of the geometrical partitioning with source, drain and channel depletion width corresponding to (a) W_{dinv}, (b) L_{dinv}, (c) W_{dinv} and (d) L_{dacc} versus V_{GS} for different V_{DS}. These simulations are realized with the corre-sponding geometry: L=100 nm, t_{si}=10 nm, t_{box}=145 nm and t_{ox}=1nm.

III. Confrontation with TCAD

A. Current and charge modeling

The Landauer equation [4-5] with the corresponding integral on energy coupled to the calculation of tunneling probabilities is complex for SPICE modeling. To simplify this approach, we propose to split the calculation of the current with separated calculation of the Fermi-Dirac distribution (call later Occupancy Function, OF) and tunneling probabilities (which classically calculate as 1D tunneling):

$$I_D \propto T_{s-c}\times\max\{OF_{s-c};0\}+T_{c-d}\times\max\{OF_{c-d};0\} \quad (7.a)$$

$$OF_{s-c} = f_{((E_{max}-\mu_s).fs0)} - f_{((E_{vs}-\mu_s).fs1)} - f_{((E_{max}-\mu_d).fs2)} + f_{((E_{vs}-\mu_d).fs3)} \quad (7.b)$$

$$OF_{c-d} = f_{((E_{cd}-\mu_s).fd0)} - f_{((E_{vc}-\mu_s).fd1)} - f_{((E_{cd}-\mu_d).fd2)} + f_{((E_{vc}-\mu_d).fd3)} \quad (7.c)$$

$$T_{s-c} = A_{kane}.e^{B_{kane}/\xi_{s-c}} \;\&\; T_{c-d} = A_{kane}.e^{B_{kane}/\xi_{c-d}} \quad (7.d)$$

where OF_{s-c} (resp. OF_{c-d}) represents the sum of different energy levels of source to channel tunneling windows (resp. channel to drain), f represents the Fermi distribution, $f_{si}/_{fdi}$ (i=1,2,3 & 4) represents calibration parameters at source and drain side. E_{max} represented the maximum energy value between E_{cc} and E_{cd} (inset of figure 1). ξ is the electric field with corresponding index s for source, d for drain and c for channel: $\xi_{s-c}=q.N_{sd}.L_{dinv}/\varepsilon_{si}$ and $\xi c\text{-}d=q.N_{sd}.L_{dacc}/\varepsilon_{si}$. A_{kane} and B_{kane} is the corresponding Kane parameter of BtBt generation. The tunneling probabilities (T) are calculated with the electric field at the interface between source and channel (for source side) and channel to drain (for drain side) which is an explicit formulation depending on source and drain depletion widths (respectively L_{dinv} and L_{dacc}). Even if the basic equation has the expected behavior of TFET operation; unfortunately as detailed in equations (7), we introduce several fitting parameters. The main advantage of this approach is an exact description of drain in any regime (in linear or logarithmic scale) with zero current for $V_{DS}=0V$ in accordance with TFET behavior.

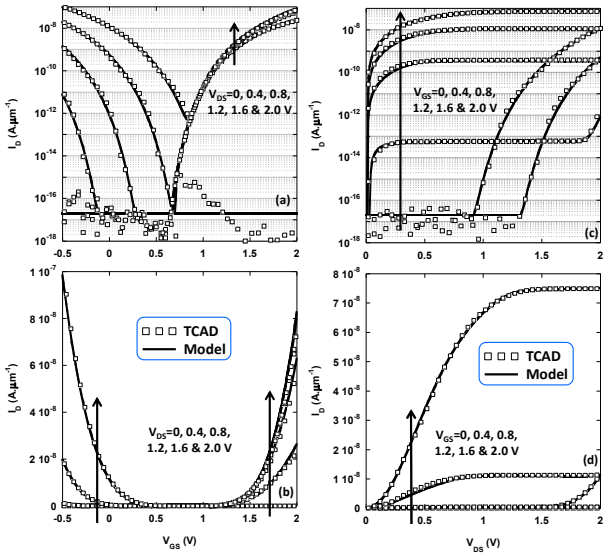

Fig. 4. Comparison between TCAD (symbol) and model (line): Current versus V_{GS} (respectively V_{DS}) in log scale (a) (respectively (c)) and lin scale (b) (respectively (d)) for different V_{DS} (respectively V_{GS}). These simulations are realized with the corre-sponding geometry: L=100 nm, t_{si}=10 nm, t_{box}=145 nm and t_{ox}=1nm.

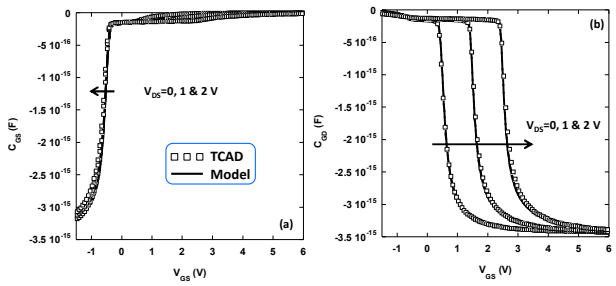

Fig. 5. Comparison between TCAD (symbol) and model (line), capacitance versus V_{GS} for different VDS: C_{GS} versus V_{GS} (a) and C_{GD} versus V_{GS} (b). These simulations are realized with the corre-sponding geometry: L=100 nm, t_{si}=10 nm, t_{box}=145 nm and t_{ox}=1nm.

The charge model for TFET is basically the sum of different charges related to source/drain depletions and channel inversion. For example, the source charge (Q_s) is the sum of the depletion into the source and the inversion charge into the channel thanks to geometrical partitioning. Note that contrary to the current model; the charge model doesn't use any fitting parameters:

$$Q_g = Q_b + Q_s + Q_d \quad (8.a)$$

$$Q_s = Q.(L - W_{dacc}) + q.t_{si}.N_{sd}.L_{dinv} \quad (8.b)$$

$$Q_d = Q.(L - W_{dinv}) - q.t_{si}.N_{sd}.L_{dacc} \quad (8.c)$$

$$Q_b \approx Q_{bg}.(L - W_{dacc}) + Q_{bg}.(L - W_{dinv}) \quad (8.d)$$

where Q_i is the charge and i=s for source, d for drain, g for front gate and b for back gate. In the last equation (7.d) we neglect the impact of source and drain charge. In fact our model is dedicated for thick BOX only because of the geometrical partitioning which imposes to have a constant depletion width along the silicon layer as explain earlier.

B. Comparison with TCAD

The corresponding architecture presented on figure 1 has been simulated with TCAD software [9-10] with the following activated electrical models: Shockley-Read-Hall Recombination (classic SRH with dopant dependencies), constant mobility model for carrier scattering and non-local band to band tunneling. This last model is the only one able to capture the realistic behavior of TFET operation. Note that Kane's parameters haven't been calibrated on experimental data. We also have to notice that our model is implemented in SPICE environment using Verilog-A language to simulate the architecture represented on figure 1.

Figure 4 represents the drain current versus V_{DS} and V_{GS}, the simulation marched well with TCAD simulation thanks to the parameter extraction of both Kane's parameters (eq. 7.d) and fitting parameter (equation 7.a and 7.b). Figure 5 represents the C_{GS} and the C_{GD} capacitance versus V_{GS}. These good agreements are mainly due to a rigorous geometrical partitioning of the charges. Nevertheless, the corresponding capacitance of the source and drain charge could be improved in term of accuracy but negligible compare to inversion charge.

IV. Conclusion

In this work, we developed a complete SPICE model for Fully-Depleted TFET transistor including physical behavior. For this, we built a complete electrostatic model to calculate the different depletion widths. Based on it, the current and charge expressions have been proposed. Unfortunately, due to the complexity of tunneling transport, the current model introduces several fitting parameters to reproduce accurately TCAD simulations results. Nevertheless, the geometrical partitioning seems to be an appropriate solution between accuracy and complexity; especially for capacitance point of view. Thus, the core model is well adapted for any surface potential approach, thanks to that we could use our methodology to nanowire TFET.

Acknowledgment

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References

[1] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," Proc. IEEE, vol. 98, no. 12, pp. 2095–2110, Dec. 2010.

[2] A. M. Ionescu and H. Riel, "Tunnel field-effect transistors as energy-efficient electronic switches," Nature, vol. 479, no. 7373, pp. 329–337, Nov. 2011.

[3] A. Villalon, C. Le Royer, P. Nguyen, S. Barraud, F. Glowacki, A. Revelant, L. Selmi, S. Cristoloveanu, L. Tosti, C. Vizioz, J.-M. Hartmann, N. Bernier, B. Prévitali, C. Tabone, F. Allain, S. Martinie, O. Rozeau and M. Vinet, "First demonstration of strained SiGe nanowires TFETs with ION beyond 700µA/µm", VLSI 2014, p1-2.

[4] L. De Michielis, L. Lattanzio and A. M. Ionescu, "Understanding the Superlinear Onset of Tunnel-FET Output Characteristic", IEEE Electron Device Letters,V33 n°11, p1553-1525.

[5] E. Gnani, A. Gnudi, S. Reggiani and G. Baccarani, "Drain-conductance optimization in nanowire TFETs by means of a physics-based analytical model", Solid-State Electronics, V84, p96-102.

[6] Lining Zhang, Xinnan Lin, Jin He, and Mansun Chan, "An Analytical Charge Model for Double-Gate Tunnel FETs", IEEE Transaction on Electron Devices, V 59 n°12, p3217-3223.

[7] LETI-UTSOI manual, 1.13 May 2012. http://www-leti.cea.fr/en/How-to-collaborate/Focus-on-Technologies/UTSOI.

[8] S. R. Banna, P. C. H. Chan, P. K. Ko, C. T. Nguyen and M. Chan, "Threshold Voltage Model for Deep-Submicrometer Fully Depleted SOI MOSFET's", IEEE Transaction on Electron Devices, V 41 n°11, p1949-1955.

[9] A. Villalon, G. Le Carval, S. Martinie, C. Le Royer, M-A.Jaud and S. Cristoloveanu, "Further Insights in TFET Operation", IEEE Transaction on Electron Devices, V 41 n°11, p1949-1955.

[10] TCAD Sentaurus Device Manual, Synopsys, Inc.: J-2014.09.