A Generic Approach for Capturing Process Variations in Lookup-Table-Based FET Models

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***Abstract*—We propose a generic approach for introducing process variations (e.g., die-to-die, wafer-to-wafer, lot-to-lot) into lookup-table-based, FET compact models. The output of the models has been carefully verified with TCAD simulation results for both conventional MOSFETs and Tunnel FETs. It is clear that this approach enables circuit-level analysis of novel transistors with the consideration of various process variation sources.**

Keywords—compact modeling; process variations; MOSFET; Tunnel FET (TFET); statistical modeling; Monte-Carlo simulation

I. INTRODUCTION

The *lookup table (LUT)* based modeling methodology has gained increasing attraction due to its fast turn-around time for generating compact models from TCAD or experimental data without losing any accuracy in model fitting [1]. This approach is particularly useful for modeling emerging devices, such as Tunnel FETs (TFETs) [1, 2], for which no standard compact models are available. However, different from equation-based compact models (e.g., BSIM [3], PSP [4]), in which *process variations (PVs)* can be captured through a selected set of model parameters [5, 6], treating PVs in LUT-based models is challenging, which may limit the application of the LUT-based modeling methodology.

In this paper, we introduce a practical approach to accurately model PVs in a LUT-based model library. A fully automated flow is developed for building *Verilog-A* [7] based model libraries using LUTs generated from TCAD data. With this approach, circuit Monte-Carlo (MC) simulations with multiple PV sources become feasible, which is critical for comprehensive performance benchmark of the modeled devices.

II. METHODOLOGY

To build a LUT-based model library with PV capability, we first create a well-calibrated TCAD deck for the nominal device. Then we identify a number of PV sources (P_i, i=1,…,*NP*) and perform TCAD simulations by varying one PV source to its +3σ or −3σ value at a time. After that, a Verilog-A model is built by using all the 2·*NP*+1 LUTs generated from the TCAD data (two LUTs for each PV and one for the nominal case).

To perform a MC simulation, a Gaussian distribution is applied to each PV source. So for each MC instance, an array, ΔP_i (i=1,…,*NP*), is passed to the Verilog-A model as instance parameters. For each bias point, the following two quantities are calculated,

$$I_d(lin) = I_{d0} \cdot \left(1 + \sum_{i=1}^{NP} \frac{I_{di} - I_{d0}}{I_{d0}} \cdot \frac{|\Delta P_i|}{3}\right) \quad (1)$$

$$I_d(exp) = I_{d0} \cdot \prod_{i=1}^{NP} \left(\frac{I_{di}}{I_{d0}}\right)^{\frac{|\Delta P_i|}{3}} \quad (2)$$

where I_{d0} is the *nominal* drain current and I_{di} is the drain current when P_i is at +3σ (−3σ) if $\Delta P_i \geq 0$ ($\Delta P_i < 0$). (ΔP_i is in numbers of σ.) Finally, the current for this bias point is computed as,

$$I_d = \eta \cdot I_d(lin) + (1 - \eta) \cdot I_d(exp) \quad (3)$$

where η is a bias-dependent, transition coefficient extracted from the nominal *I-V* curve (see Table I for details). (The calculation of *C-V* values is the same as the *I-V* case.)

TABLE I. EXTRACTION OF η FROM NOMINAL *Id-Vg* CURVE

Step	*Procedures*
1	For a given bias point (*Vgs0*, *Vds0*), measure **the *Id* dependence on *Vth* variation** by exacting the following two values from the LUTs (e.g., ΔVth=20mV): *Id(p) = Id@Vgs=Vgs0−ΔVth, Vds=Vds0* *Id(m) = Id@Vgs=Vgs0+ΔVth, Vds=Vds0*
2	Calculate $I_d(ave1) = [Id(p) + Id(m)]/2$ and $I_d(ave2) = \sqrt{Id(p) \cdot Id(m)}$
3	$$\eta = \frac{I_{d0} - I_d(ave2)}{I_d(ave1) - I_d(ave2)}$$ where I_{d0} is the *nominal* current. Note that in the sub-threshold regime, the current has an exponential dependence on *Vth*, so $I_{d0} \approx I_d(ave2)$ and $\eta \approx 0$. And in the super-threshold regime, the current has an approximately linear dependence on *Vth*, so $I_{d0} \approx I_d(ave1)$ and $\eta \approx 1$.
4	It is observed that to further improve the smoothness of the *IdVg* curves generated from the model, a damping factor, β ($0 < \beta < 1$), can be applied to η (i.e., $\eta \rightarrow \beta \cdot \eta$). β=0.6 is used for all the results presented in this paper.

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The procedure above is inspired by the observation that for a well-designed FET, its threshold-voltage (*Vth*) has an approximately linear dependence on PVs. When the FET is operating in the *sub-threshold* regime, the drain current (*Id*) has an exponential dependence on *Vth*, therefore, *Id* tends to vary with PVs exponentially, as described in Eq. (2). When the FET is operating in the *super-threshold* regime, its *Id* value responds to the *Vth* variation in an approximately linear manner, so the *Id* variation can be estimated using a linear function of the PVs, as shown in Eq. (1). To cover the full dynamic bias range, the transition coefficient, η, is introduced to calculate the drain current under a given bias condition as a combination of the linear case (i.e., $I_d(lin)$) and the exponential case (i.e., $I_d(exp)$). As shown in the next section, this method can well reproduce the drain current dependence on various PVs in the full operating region for both MOSFETs and TFETs.

III. Results

A. Model Validation at Various Process Variation Corners

To validate this methodology, we compare the output of the generated LUT-based model library vs. TCAD data for both an n-type, planar bulk MOSFET and an n-type, Ge-source/Si-channel TFET [2] with *various PV combinations*. (The cross-section of the TFET is illustrated in Fig. 1.) In this testcase, we chose three PV sources ($\{\Delta P_i\}$) for each device – gate oxide thickness (*Tox*), gate length (*Lg*) and channel doping concentration (*Nch*) for the MOSFET, and gate oxide thickness (*Tox*), source doping concentration (*Ns*) and N+ pocket doping concentration (*Npck*) for the TFET. The nominal and 3-σ values for each PV source are summarized in Table II. (More PV sources can be added for more realistic performance benchmark.)

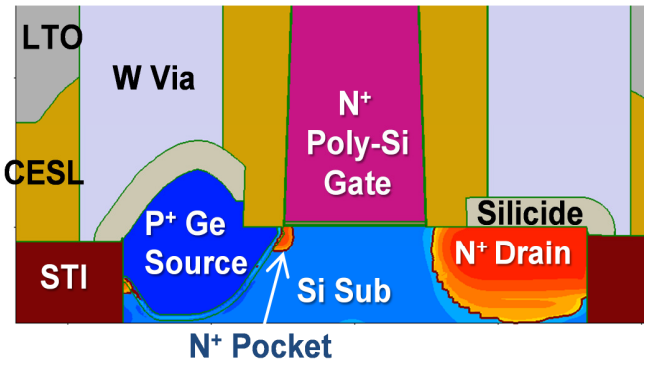

Fig. 1 Cross-section of the simulated n-type TFET with a Ge source, a Si channel and an N+ pocket near the source region. [2]

TABLE II. Nominal and 3-σ Values for Each Process Variation Source

Devices	Process Variation Sources ($\{\Delta P_i\}$)		
MOSFET	***Tox***	***Lg***	***Nch***
	1.6±0.1nm	40±3nm	5.6×10^{18} cm^{-3} ±10%
TFET	***Tox***	***Ns***	***Npck***
	1.2±0.1nm	6×10^{19} cm^{-3} ±10%	4×10^{19} cm^{-3} ±10%

Figure 2 compares the *Id-Vg* curves generated from our LUT-based compact models (symbols) and TCAD simulations (lines) at various process variation corners for both the MOSFET (a&b) and the TFET (c&d). It is clear that our compact models produce smooth *Id-Vg* curves in the full dynamic range ($0\leq Vgs\leq$VDD) and the compact model results well match TCAD data under all bias conditions. Fig. 3 shows the ON-current comparison between TCAD and compact model for more PV combinations, and an excellent agreement is observed for both the MOSFET and the TFET.

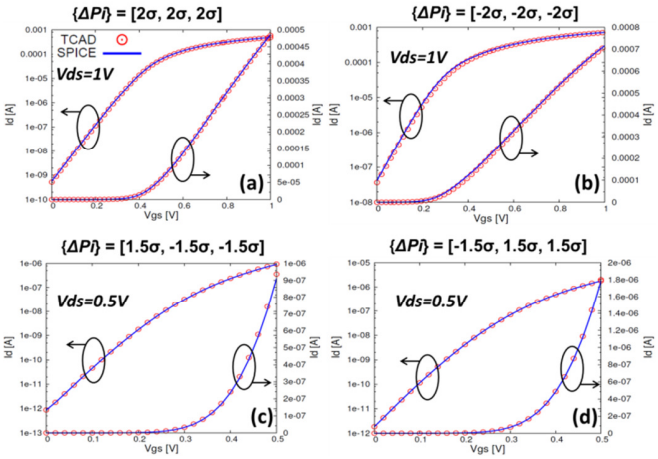

Fig. 2 *Id-Vg* curves generated from compact (SPICE) models (symbols) and TCAD simulations (lines) at various process variation corners for both an n-type MOSFET (a&b, *Lg*=40nm, *W*=1µm) and an n-type TFET (c&d, *Lg*=40nm, *W*=1µm, with a Ge source and a Si channel [2]).

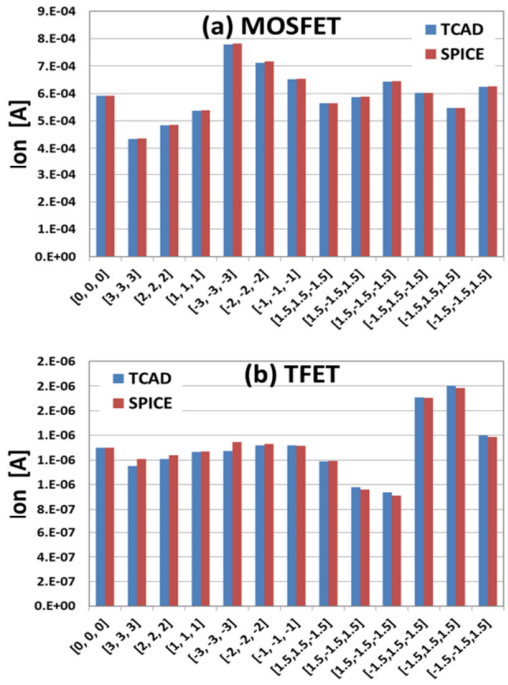

Fig. 3 Comparison of ON-currents between TCAD and compact (SPICE) model results for (a) n-type MOSFET (VDD=1V) and (b) n-type TFET (VDD=0.5V) with various PV combinations. (The σ values of $\{\Delta P_i\}$ in each case are labeled under the *x* axis of each plot.) The RSS of the fitting errors for all the cases is 0.3% for MOSFET and 2.2% for TFET, respectively.

From the results shown above, we can conclude that with the methodology we proposed, our LUT-based model can accurately reproduce TCAD data for arbitrary PV combinations. In other words, for each MC instance (i.e., a device with a given $\{\Delta P_i\}$), our LUT-based model can well match the TCAD results. As a result, the statistical distributions generated from our LUT-based model library will be a good representation of those from TCAD simulations. (In practice, direct TCAD simulations of a large number (e.g., 1000) of device samples can be prohibitive due to high computational costs.)

B. *Monte-Carlo Simulation of Individual FETs*

Using the LUT-based model libraries generated in this work, we perform MC simulations of individual MOSFETs and TFETs. Figs. 4 and 5 show the MC simulation results (1000 runs) for the n-type MOSFET and the n-type TFET, respectively. As expected, the *Ion* data cloud of the MOSFET follows a normal distribution while that for the MOSFET *Ioff* obtains a log-norm distribution. For the TFET case, the *Ioff* distribution is also in a log-norm form, similar as the MOSFET case. The TFET *Ion* data, however, start to deviate from a normal distribution at higher σ values, mainly due to the fact that at VDD=0.5V, the TFET *Ion* doesn't have a strict linear dependence on *Vth*, so the shape of the TFET *Ion* distribution is between a normal form and a log-norm form. From the distributions of the MC simulation data, we can extract device variation specs (e.g., LSL and USL of *Ion*, *Ioff*, etc.), which are very important for device targeting and design optimization.

As we know, proper modeling of device variability correlations among different device types (e.g., regular-*Vth* n-MOSFET vs. regular-*Vth* p-MOSFET, or low-*Vth* n-MOSFET vs. high-*Vth* n-MOSFET) is critical for accurate circuit simulation and benchmark. Given the fact that a Gaussian distribution is explicitly applied to each PV source in our LUT-based model library, the correlations of process-induced variations among different device types are well captured in our MC simulations. Fig. 6 illustrates the correlations between the n-type MOSFET and its p-type counterpart for (a) *Ion* and (b) *Ioff* variations. Here we assume that the two devices have a perfect correlation on *Tox* and *Lg*, and no correlation on *Nch*. As a result, the two devices are partially correlated (i.e., $0<corr<1$) on both *Ion* and *Ioff* variations. The ability to capture device variability correlations in a fundamental way is certainly a very attractive feature of this methodology.

C. *Monte-Carlo Simulation of Ring Oscillators*

Finally, we simulate the Inverter-based ring oscillators (ROs) using our LUT-based model libraries for both MOSFETs and TFETs. Fig. 7 plots the delay vs. leakage power MC results for both (a) MOSFET and (b) TFET. From the distribution of the MC simulation data, the worst-case circuit metrics (e.g., delay, power consumptions) can be estimated with the consideration of process variations.

SUMMARY

In this paper, we introduced a generic approach for capturing process (or global) variations in lookup-table-based, FET compact models. A conventional MOSFET and a Ge-source TFET are used as testing vehicles for model validation. The results clearly show that the output from our compact models can accurately match the TCAD data at various process variation corners, and process-induced, variability correlations among different devices are well captured. With the model libraries generated using this approach, Monte-Carlo simulations can be performed to evaluate the impact of process variations on device specs as well as circuit metrics.

In conclusion, the introduction of this approach has greatly improved the capability of the lookup-table-based modeling methodology, making it suitable for circuit-level analysis of novel transistors with the considerations of process variations. It should be also noted that the modeling of *local variations* [8], such as random-dopant-fluctuations, line-edge-roughness, metal-gate-granularity, etc., is beyond the scope of this paper, and it will be explored in our future work.

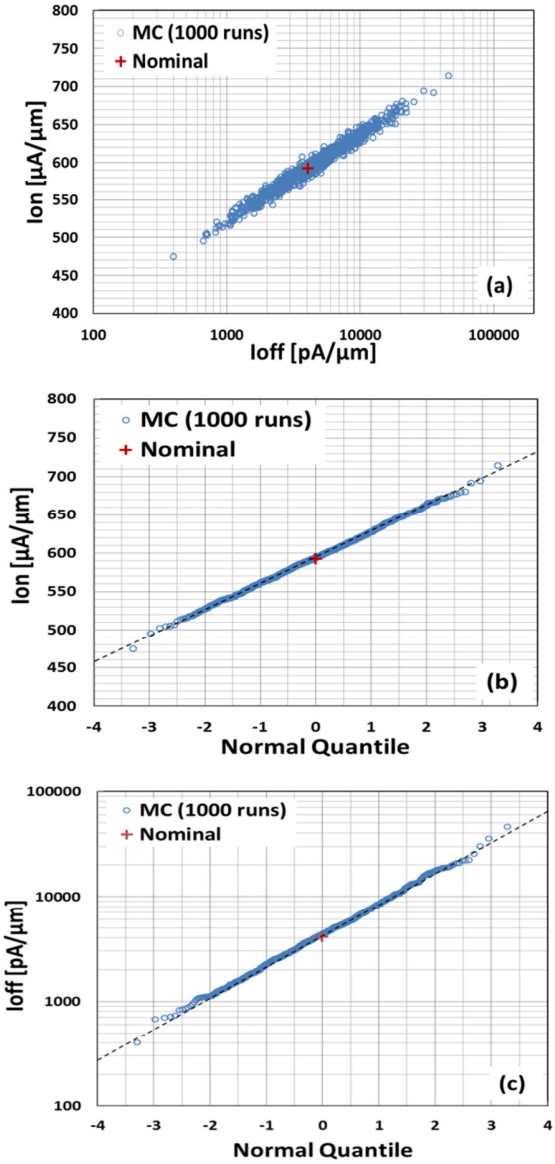

Fig. 4 MC simulation results (1000 runs) for n-type MOSFET (VDD=1V). (a) *Ion vs. Ioff* (log), (b) *Ion vs. normal quantile* and (c) *Ioff* (log) *vs. normal quantile.*

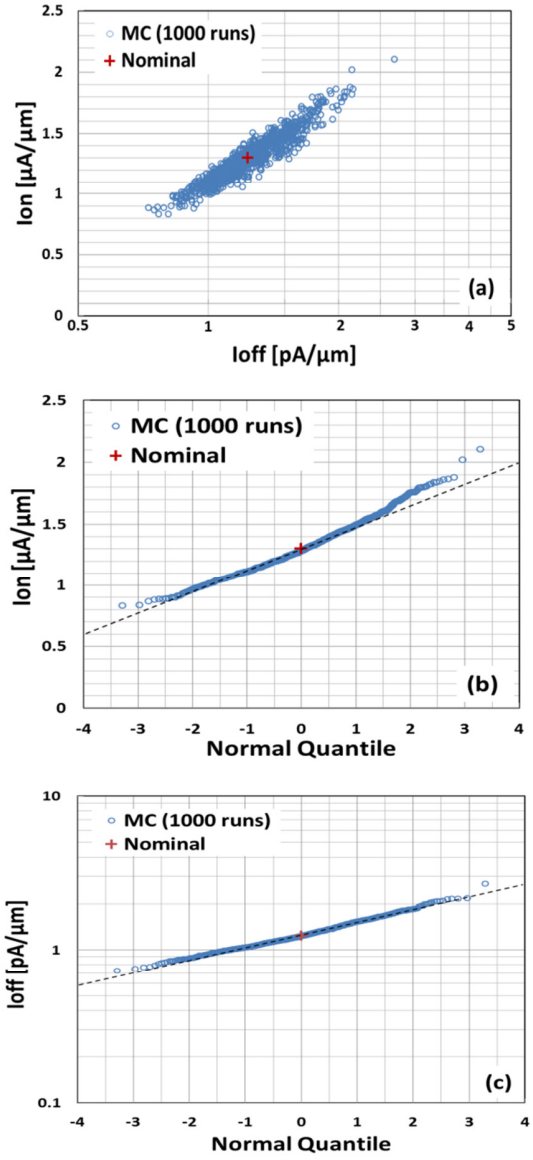

Fig. 5 MC simulation results (1000 runs) for n-type TFET (VDD=0.5V). (a) *Ion vs. Ioff* (log), (b) *Ion vs. normal quantile* and (c) *Ioff* (log) *vs. normal quantile.*

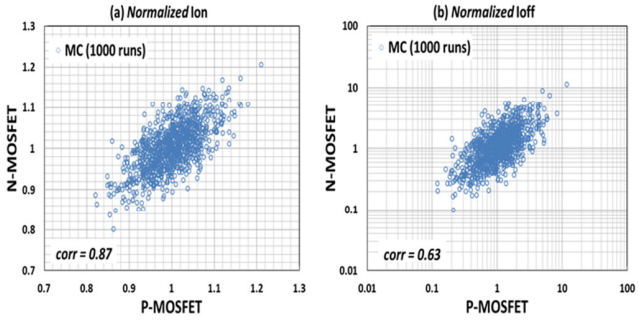

Fig. 6 Correlations of process-induced variations between n-MOSFET and p-MOSFET. MC simulation results (1000 runs) are included for (a) *Ion* and (b) *Ioff*, with all currents normalized by the corresponding nominal values.

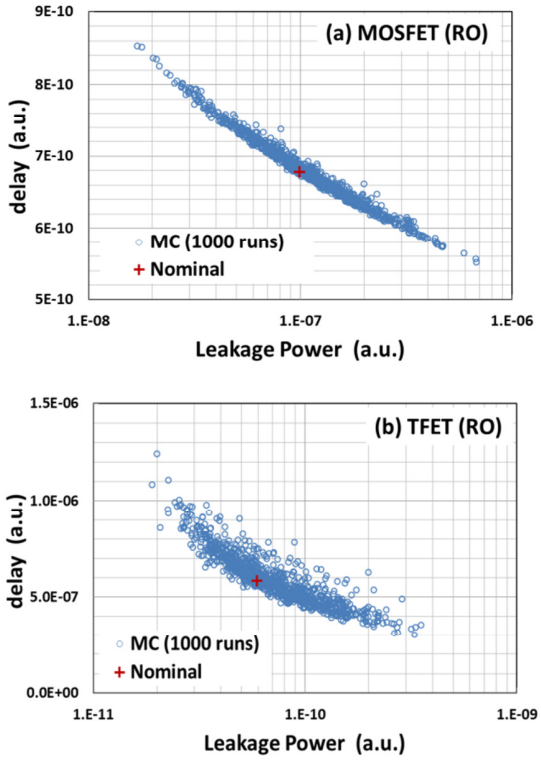

Fig. 7 MC simulation results (1000 runs) for (a) MOSFET RO delay vs. leakage power (VDD=1.0V) and (b) TFET RO delay vs. leakage power (VDD=0.5V).

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