FinFET to Nanowire Transition at 5nm Design Rules

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***Abstract*—Semi-classical and quantum transport approaches are applied and compared to analyze the relative driving strength of nmos nanowires compared to FinFETs at 5nm design rules. Both transport approaches show better-than-expected nanowire drive current. The reason for this strong performance is explained in terms of electrostatic and subband structure effects. The impact of scattering on the fin to nanowire transition is also examined.**

Keywords—FinFET; nanowire; quantum transport; multi-subband BTE

I. Introduction

The Tri-gate FinFET architecture enables scaling beyond the 20nm technology node due to better gate control than single-gate, planar MOSFETs. From electrostatic considerations, the Gate-All-Around (GAA) transistor architecture can potentially provide further improvements in gate control and therefore enable scaling beyond the FinFET design. In addition, manufacturing considerations, such as mechanical stability, may place a practical limit on how narrow fin structures can be scaled. Replacing fins with nanowires may provide a further path to scaling, but for a given layout pitch, it is important to understand the relative tradeoffs in drive strength. In this paper, we use both semi-classical and quantum transport approaches to characterize the intrinsic device performance of a fin as it is scaled down to a nanowire.

II. Benchmark Approach

A. Device Structures

We benchmark silicon GAA nmos transistors based on design rules extrapolated to the 5nm technology node (Table 1). This extrapolation is performed by starting at established design rules for the 14nm technology node and assuming a traditional 2x reduction in layout area per technology node. As shown in Fig. 1, the transistors are composed of a rectangular cross-section that changes from 5nm x 30nm for a fin to 5nm x 5nm for a nanowire (NW). The channel is left undoped while the source and drain of length 10nm are doped at 2.0e20 cm^{-3}. Abrupt doping profiles with zero gate overlap are used. The gate is modeled as a metal with an adjustable workfunction.

TABLE I. Key Design Rules

Parameter	Value
Channel Length	11 nm
Gate Dielectric EOT	0.8 nm
Fin/wire width	5 nm
Fin/wire pitch	16 nm
Power Supply Voltage	0.7 V
Channel & S/D Doping	0, 2.0e20 cm^{-3}
Off-state current	1 nA/μm
Channel direction	<110>

B. Transport Approaches

Due to the highly scaled cross-sectional dimensions, we perform subband-based carrier transport using 3D ballistic quantum transport (QT) [1] and quasi-ballistic semi-classical transport based on the multi-subband Boltzmann Transport Equation (MS-BTE) [2,3,4]. Both approaches use a parabolic band model for the three Δ valleys in silicon and employ Neumann boundary conditions at the source and drain contacts. For QT, a wavefunction-based, coupled mode space approach is used. For MS-BTE, an uncoupled mode space approximation is used for computing subbands along the channel. The BTE for the distribution function within each subband is solved using a deterministic algorithm. While QT is limited to ballistic transport, MS-BTE includes scattering models for acoustic and inter-valley phonon scattering as well as surface roughness scattering.

Simulations of the on-current at a fixed supply voltage of 0.7V are performed for different fin heights ranging from 5nm to 30nm. The on-currents are compared at a fixed off-current of 1nA/μm by adjusting the gate workfunction. The current is normalization by the fin pitch in order to fairly compare devices with the same layout area.

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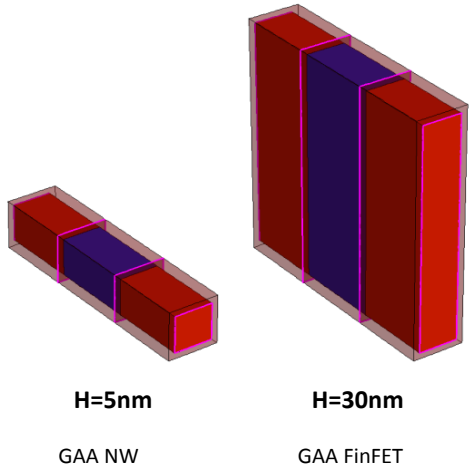

Fig. 1. Device structures for Nanowire (NW) and FinFET

III. Results

A. Ballistic Results

We first analyze the fin to nanowire transition in the ballistic limit using both QT and MS-BTE. As shown in Fig. 2, all fin heights exhibit volume inversion in the on-state (V_{gs}=V_{ds}=0.7V). In addition, the peak electron density increases as the height is reduced from a tall fin down to a square nanowire.

Fig. 3 shows a comparison of the on-current computed using QT and MS-BTE in the ballistic limit. The results from both approaches agree well. From Fig. 3 it is also evident that the on-state current dependence on the fin height is much weaker than a simple cross-sectional area scaling factor would give. In fact, the NW case is surprisingly strong, reaching 70% of the strength of the 30nm tall fin that has six times the cross-sectional area. A breakdown of this strong drive current is given it terms of electrostatic and subband structure effects.

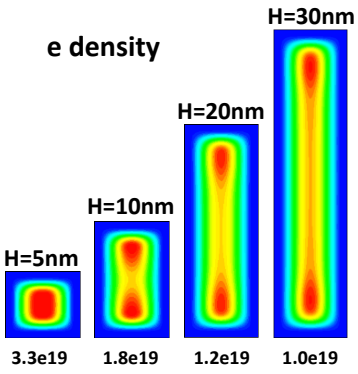

Fig. 2. Electron Density in the on-state from QT. Peak levels listed in cm^{-3}

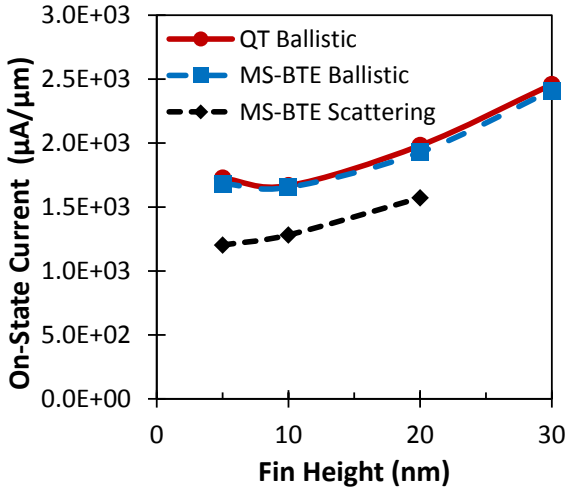

Fig. 3. Driving strength vs. fin height

As shown in Fig. 4, transitioning from fin to NW improves the sub-threshold slope from 80+ mV/decade to below 70 mV/decade. The QT and MS-BTE transport approaches produce consistent sub-threshold slopes indicating that direct source/drain tunneling is not significant at this gate length (11nm).

It is convenient to analyze the on-current behavior in terms of the product of the inversion charge and velocity at the top of the source/drain barrier (ToB). Fig. 5a shows the height dependence of the ToB on-state inversion charge based on ballistic MS-BTE. The inversion charge scales relatively weakly with the Fin height, dropping only by a factor of about 2 when the cross-sectional area drops by a factor of 6. A large contribution to this strong inversion charge arises from the dependence of the total gate oxide capacitance on the fin height. Fig. 5a also shows the expected scaling of the inversion charge based on the total gate oxide capacitance (Cox) as computed from the solution of a 2D Poisson equation for the channel cross-section.

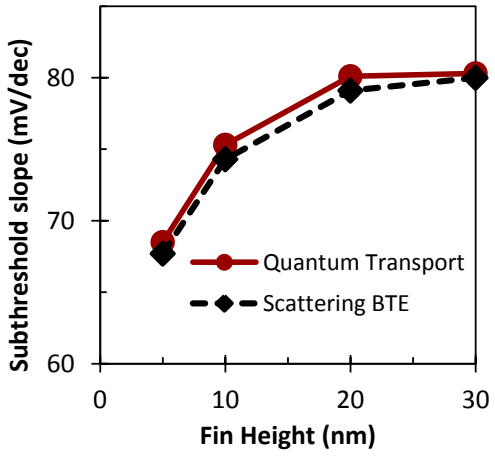

Fig. 4. Sub-threshold slope vs. fin height

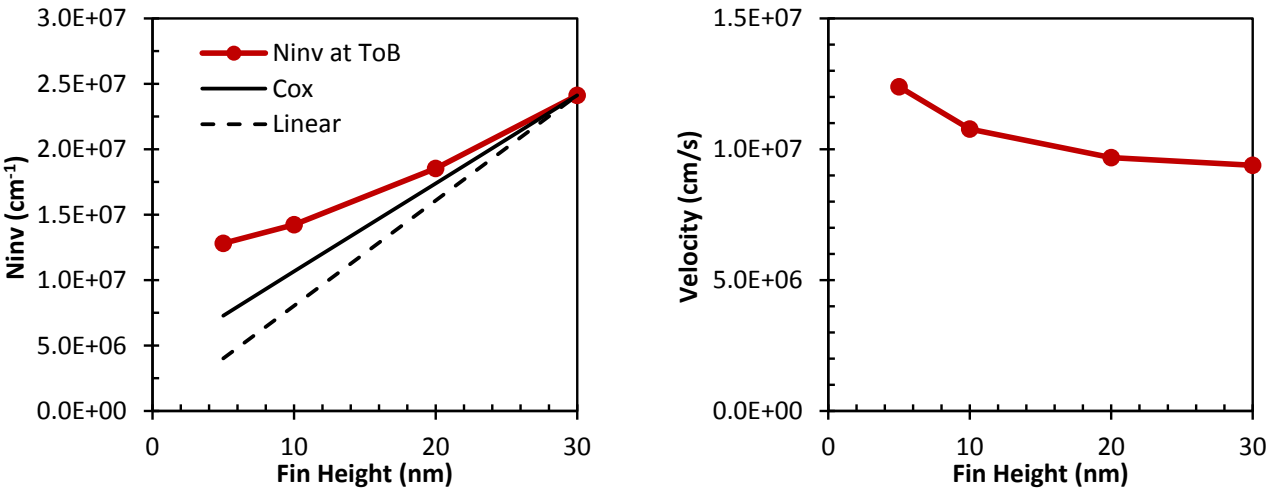

Fig. 5. a) ToB inversion charge (Ninv) from MS-BTE vs. fin height. Also shown is the expected fin height scaling based solely on a simple linear height dependence and on the scaling of Cox. b) ToB velocity vs fin height from MS-BTE.

For a tall fin, the gate capacitance is dominated by the sidewalls, while for a square nanowire, both the top and sidewalls contribute equally to Cox, thus doubling the sidewall contribution. An additional contribution to the inversion charge for the NW case arises from the improved sub-threshold slope, which for fixed Ioff and supply voltage, gives rise to a larger gate overdrive compared to the tall fins.

As shown in Fig. 5b, the ToB velocity is also improved when reducing the fin height. This improvement is partially explained by looking at the Δ valley orientations relative to the cross-section, shown in Fig. 6. As the fin height is reduced, quantum confinement effects increase the subband energy of the $\Delta_{1,2}$ valleys more than the Δ_3 valley due the small confinement mass along the vertical direction for $\Delta_{1,2}$. This produces increased carrier occupation in Δ_3 as the fin height is reduced, as shown in Fig 7. This re-population effect is beneficial for transport because the transport mass of the Δ_3 valley (0.19) is significantly less than that of the $\Delta_{1,2}$ valleys (0.55) resulting in increased thermal injection velocity.

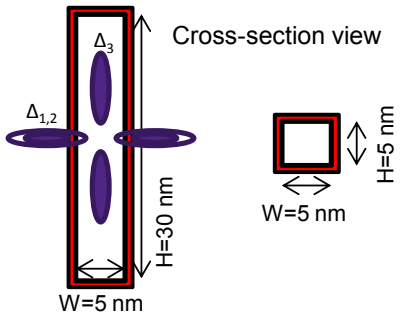

Fig. 6. Δ valley orientation relative to the device cross-section. With a <110> channel, the $\Delta_{1,2}$ valleys are impacted by stronger quantum confinement as the height is reduced.

The impact of valley re-population on the injection velocity for the 5nm and 30nm height cases is highlighted in Fig. 8. At low gate bias in the non-degenerate carrier regime, the velocity is increased by 25% when the fin height is reduced from 30nm to 5nm. The NW injection velocity receives an additional boost in the on-state because the carrier density is pushed further into the degenerate regime due to the lower DOS of the Δ_3 valley and also because of increased gate overdrive relative to the fin case [5].

B. Scattering Results

As shown in Fig. 3, the inclusion of phonon and surface roughness scattering in the MS-BTE approach produces a similar trend in the on-current vs. height as in the ballistic case. A ballistic ratio of about 80% is maintained down to 10nm fin height.

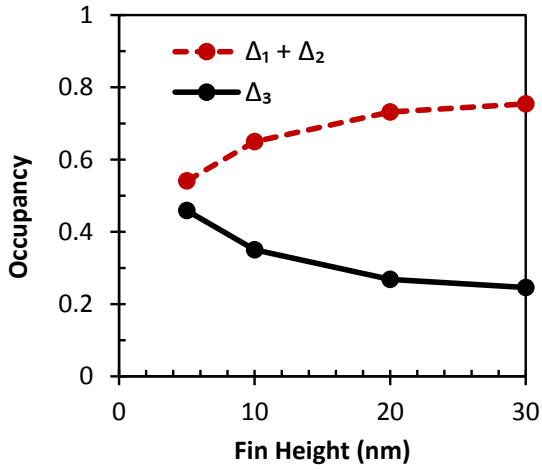

Fig. 7. Valley occupancy vs. fin height from MS-BTE

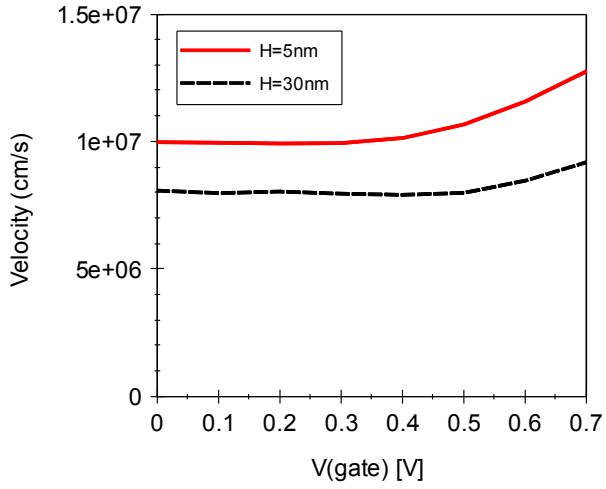

Fig. 8. Injection velocity vs. gate bias for fin heights of 5nm and 30nm from MS-BTE

Phonon scattering is proportional to the wavefunction form-factor. As shown in Fig. 9, for the larger fin heights the form-factor displays a weak dependence on the fin height and is determined primarily by the narrow 5nm fin width. Below the 10nm fin height, the form-factor strongly increases which in turn increases scattering and spreads the distribution function around the top of the source/barrier, as shown in Fig. 10. As the fin height is scaled below 10nm, the ballistic ratio ($I_{scatter}/I_{ballistic}$) degrades to 70% for the NW case.

IV. Conclusions

Two independent subband-based transport approaches, 3D quantum transport and multi-subband BTE, provide consistent evidence of strong NW intrinsic drive current relative to a tall fin, or equivalently, a wide nano-ribbon. Detailed analysis in the ballistic limit identified improved short-channel effects, NW gate oxide capacitance, beneficial subband re-population, and increase carrier degeneracy as the reasons for this strong performance. Analysis of the transition from fin to NW using the MS-BTE approach with scattering showed the strong performance of the NW is maintained, but by the 5nm cross-section size, increased scattering due to stronger wavefunction overlap degrades the ballistic ratio.

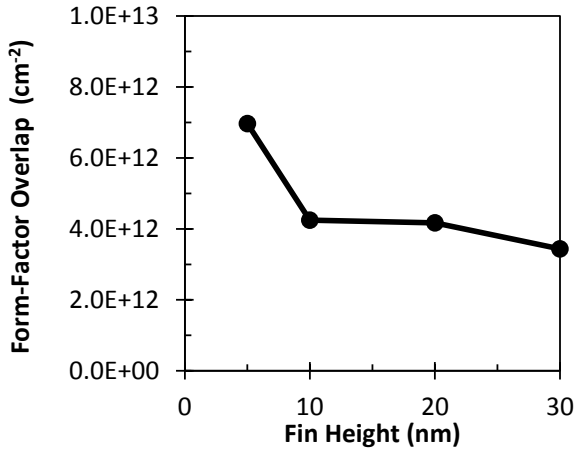

Fig. 9. Valley-occupancy weighted form-factor vs. fin height

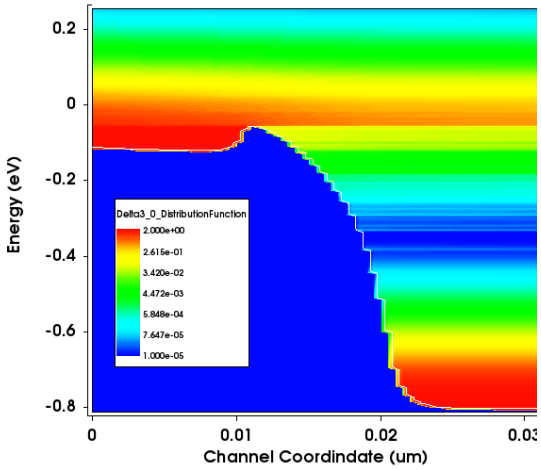

Fig. 10. Distribution function as a function of total carrier energy along the channel direction for the lowest subband in the NW in the on-state from MS-BTE

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