Impact of Gate Oxide Complex Band Structure on *n*-Channel III-V FinFETs

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***Abstract*—FinFET geometries have been developed for the sub-22 nm regime to extend Si-CMOS scaling via improved electrostatics compared to planar technology. Moreover, engineers have incorporated high-k oxide gate stacks. Beyond leakage current, less discussed is the impact of the gate oxide's complex band structure on the device performance. However, it defines the boundary condition for the channel wavefunction at the interface, which, in turn, affects the quantum confinement energy for channel electrons. Here we show that the ON-state performance of *n*-channel FinFETs may be sensitive to the oxide's complex band structure, especially with light-mass III-V channel materials, such as $In_{0.53}Ga_{0.47}As$. We study this effect using an ensemble semi-classical Monte Carlo device simulator with advanced quantum corrections for degeneracy and confinement effects. Our simulations suggest that using a surface oxide with a heavy effective mass may lower the channel carrier confinement energies, mitigating unwanted quantum side-effects that hinder device performance. Ultimately, future high-k stacks may benefit from oxide gate stack heterostructures balancing effective mass and dielectric permittivity considerations.**

I. Introduction

Physical limits [1] have become the pressing challenge for Si planar metal-oxide-semiconductor-field-effect-transistors (MOSFETs) when considering future device nodes. Simply reducing device dimensions is no longer sufficient, as nano-scale planar CMOS devices suffer from debilitating short-channel effects (SCE) [2]. Poor electrostatic control can lead to substantial drain-induced barrier lowering ($DIBL$) and degraded device subthreshold swing (S), as well as limiting transconductance (g_{m}), contributing to poor ON/OFF ratios.

Incorporation of new three-dimensional (3D) geometries, especially that of the 3D fin-shaped MOSFET (FinFET) [3], has extended the scaling life of MOSFETs via improved gate control, as well as reduced on-chip surface area. FinFETs are likely to drive scaling in future device nodes [4]. Moreover, high dielectric constant (high-k) oxide stacks have improved gate-to-channel capacitive coupling, allowing for reduced effective electrostatic oxide thicknesses (EOT), despite increased physical thicknesses to prevent tunneling.

Alternate channel materials also are being considered widely for future device nodes, such as III-Vs for n-channel devices in particular [5]. III-Vs may provide a performance boost versus Si in the ON-state via higher bulk mobilities and higher thermal injection velocities associated with lighter masses, the latter being more important approaching the ballistic limit. In particular, $In_{0.53}Ga_{0.47}As$, which is lattice-matched to fabrication-friendly InP [6], provides Γ-valley electrons with an effective mass of $m^*_\Gamma = 0.047\ m_e$. However, for deeply-scaled devices a host of quantum mechanical effects may diminish the otherwise expected advantages. Considerations of the Pauli Exclusion Principle lead to reduced quantum/density-of-states (DOS) capacitance (C_{q}), while quantum confinement reduces intervalley separations, increases phonon scattering rates, and decreases electrostatic capacitance as the carriers are shifted further from the interface.

In this paper, we show that the choice of gate oxide may affect device performance not just through the electrostatics but also through these quantum confinement effects, as it establishes the boundary conditions on the channel wavefunction. To this end, we use the ensemble semi-classical Monte Carlo (EMC) simulation tool with advanced quantum corrections that was described in [7] to model nano-scale $In_{0.53}Ga_{0.47}As$ FinFETs. We find that use of lighter gate oxide effective masses (m^*_{ox}) actually leads to increased quantum confinement effects, including increased scattering and intervalley transfer, and, thus, reduced ON-state performance. In this way, we find that the otherwise expected advantage of higher-k materials may be minimized by often-associated lighter masses, and that oxide stacks combining higher-mass surface dielectrics with higher-k dielectric over-layers could prove optimal.

II. Model and device-level quantum corrections

To efficiently and accurately model 3D FinFETs, with $In_{0.53}Ga_{0.47}As$ channels including non-parabolic band structures, an appropriate simulation methodology is EMC [8], [9]. EMC seamlessly handles regimes of transport from diffusive through ballistic, while including all relevant scattering processes, including long-range polar optical phonon scattering that can dominate electron scattering in III-Vs.

Our software generates complex 3D geometries, such as the model FinFET considered in this study (Fig. 1), with material-specific band structures—valley edge separations, masses, and non-parabolicity constants—and other parameters borrowed from other studies [10]–[13]. Our EMC calculations provide quantum corrections to capture the essential physics of important quantum confinement effects, in addition to Pauli Exclusion considerations in degenerate systems.

A. Quantum corrections for degeneracy

Scaling principles demand degenerate dopant densities approaching solid-solubility limits. For $In_{0.53}Ga_{0.47}As$ channels, we choose an activated source/drain dopant density of

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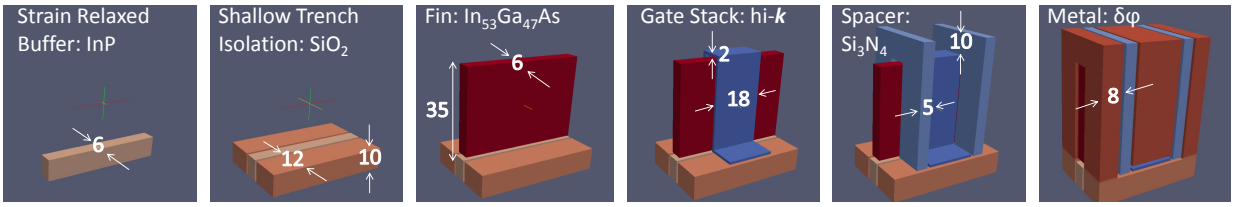

Fig. 1: Edge view of simulated *n*-channel $In_{0.53}Ga_{0.47}As$ FinFET showing each material region. The source and drain reservoirs have an activated dopant density of N_D=5×10^{19} cm^{-3}. The $\delta\phi$-metals are variable work function contacts used to set the Fermi distribution injection boundaries. All dimensions are in nm.

$N_D = 5 \times 10^{19}$ cm^{-3}, a realistic estimate which can be reached with current *in situ* doping techniques, and possibly future implantation technology [14]. Comparable or higher carrier densities can be induced in the channel by the gate electrode. We therefore establish a beyond-Fermi treatment of Pauli-Exclusion-blocked scattering, appropriate for highly non-equilibrium conditions, by self-consistently determining the local carrier occupation as a function of energy, transport direction, and valley. In the ON-state, Pauli blocking reduces C_q and ultimately forces carriers out of the light-mass Γ-valley. For $N_D = 5 \times 10^{19}$ cm^{-3}, the equilibrium Fermi energy is driven nearly 500 meV into the Γ-band, transferring carriers to the peripheral bands, even absent quantum confinement.

B. Quantum corrections for confinement

To model quantum confinement effects in 3D FinFET systems, we calculate valley- and space-dependent quantum-corrected effective potentials, whose fields move the semi-classical Monte Carlo particles into a more quantum-mechanical spatial configuration, i.e. away from the channel-oxide interface. These valley-dependent corrected-potentials also reduce intervalley separations, further enhancing intervalley transfer. Quantum confinement enhances phonon processes, scattering electrons in $\boldsymbol{k}$-space via recalculated phonon rates [15], including a stronger onset of intervalley scattering [7]. In addition, surface roughness scattering, which is commonly calculated in terms of quantum confinement energies [16]–[18], is treated as a function of the quantum correction in our method.

Critical to this work, these quantum-corrected effective potentials are based on effective mass Schrödinger equation bound state energy eigenstate calculations [15]. However, once the bound state energies are found within this effective mass approximation, we also employ a non-parabolicity correction on each quantum-corrected effective potential.

III. Gate Oxide Dielectric Constant Effects

$In_{0.53}Ga_{0.47}As$ transistors with the geometry of Fig. 1 are simulated with varying gate oxide dielectric constants. Fig. 2 shows the result of increasing the gate oxide dielectric constant from an Al_2O_3-like $\varepsilon_r = 7.8$ (gray curves) to a HfO_2-like $\varepsilon_r = 22.3$ (black curves), but otherwise using Al_2O_3-like parameters [19] in both cases. As expected, a larger ε_r delivers better performance (Fig. 2a), emphasized by the larger peak transconductance $g_M = \mathrm{MAX}\{dI_{DS}/dV_{GS}\}$, lowered OFF-state $S = (\ln 10)dV_{GS}/d(\ln I_{DS})$, and $DIBL = d\Phi_b/dV_{DS}$, where Φ_b is the channel potential barrier (Table I). The better performance can be understand in terms of the increased capacitive coupling of the gate to the channel (Fig. 2b).

TABLE I: Variation of gate oxide dielectric constant

Dielectric constant	$\varepsilon_r = 7.8$	$\varepsilon_r = 22.3$
EOT (nm)	1.0	0.35
g_M (mA/μm/V)	2.4	3.8
S (mV/dec)	76	67
$DIBL$ (mV/V)	94	55

IV. Gate Oxide Effective Mass Effects

Fig. 3 shows the result of decreasing the gate oxide effective mass from an Al_2O_3-like $m^*_{ox} = 0.4m_e$ [19] (gray curves) to a HfO_2-like $m^*_{ox} = 0.08m_e$ [20] (black curves), but otherwise using Al_2O_3-like parameters in both cases.

Fig. 3a shows diminished drive current when lowering the oxide effective mass. Table II shows that the g_M is reduced by almost 30% relative to the device with higher m^*_{ox}. The culprit is increased quantum confinement for the device with lighter m^*_{ox}, as shown by the larger ensemble average quantum correction for carriers injected over the channel potential barrier-top (Fig. 3b, left-axis). In these simulations, the oxide's complex band structure is parameterized by its m^*_{ox} along with its barrier height. An increase in calculated quantum-confined bound state energies with reduction in m^*_{ox} can be seen as a by-product of the required mass-difference-induced discontinuity in the wavefunction derivative at the interface [21], despite also increased barrier penetration depths. (We note that our Schrödinger equation and wavefunction are discretized in our calculations, with the mass change reflected only in (Hermitian) changes in the inter-site hopping potentials. However, this approach preserves this basic effect of the impact of the mass change across the interface.)

The resulting increase in quantum corrections bolsters an already strong transfer of electrons to the heavy-mass

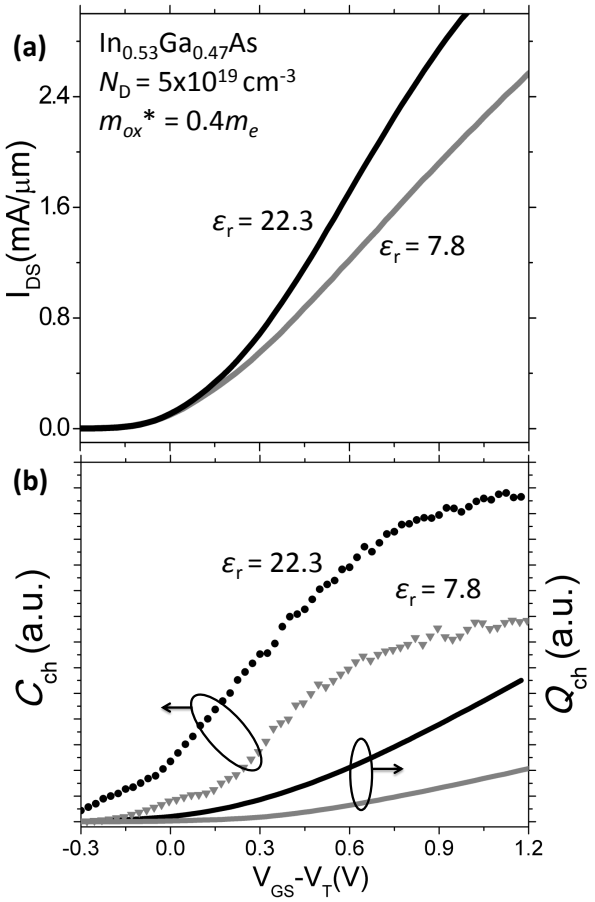

Fig. 2: Varying oxide dielectric constant. (a) $I_{\rm DS}$ vs. $V_{\rm GS}$ for otherwise identical FinFETs having gate oxide dielectric $\varepsilon_{\rm R} = 7.8$ (gray) compared to $\varepsilon_{\rm R} = 22.3$ (black). (b) Increasing the dielectric constant (from gray to black) induces a larger channel inversion charge density $Q_{\rm ch}$ (right-axis) and capacitance $C_{\rm ch} = {\rm d}Q_{\rm ch}/{\rm d}V_{\rm GS}$ (left-axis).

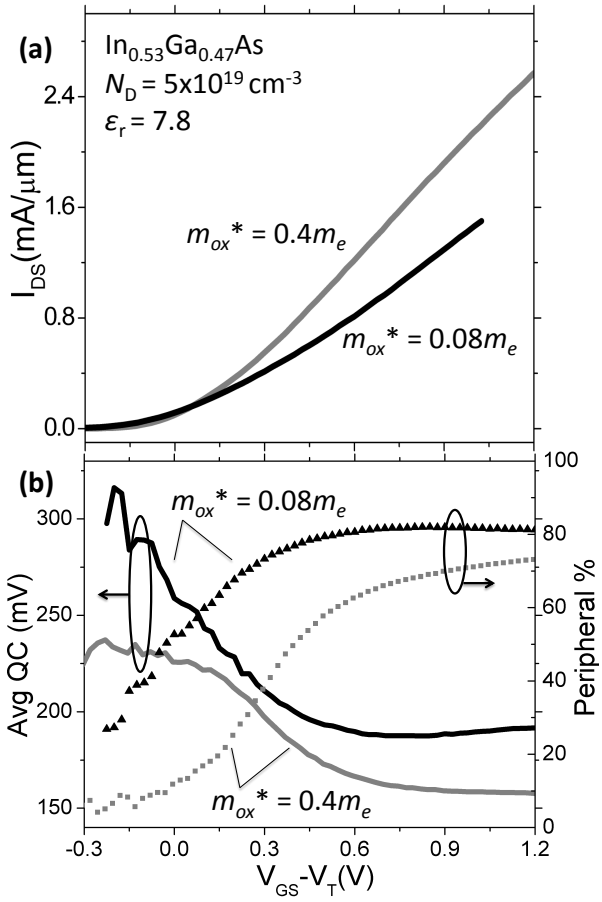

Fig. 3: Varying oxide effective mass. (a) Transfer curves comparing gate oxide effective mass $m^*_{\rm ox} = 0.4$ (gray) to $m^*_{\rm ox} = 0.08$ (black). (b) Decreasing the gate dielectric's effective mass increases the average quantum confinement energy (left-axis) and occupation of heavy-mass peripheral valley states (right-axis).

TABLE II: Variation of gate oxide effective mass

Effective mass	$m^*_{\rm ox} = 0.4m_{\rm e}$	$m^*_{\rm ox} = 0.08m_{\rm e}$
EOT (nm)	1.0	1.0
$g_{\rm M}$ (mA/μm/V)	2.4	1.73
S (mV/dec)	76	75
$DIBL$ (mV/V)	94	94

peripheral valleys (Fig. 3b, right-axis) and degrades the current density. However, SCE are shown to be insensitive to confinement, as the S and $DIBL$ are relatively unaffected (Table II).

V. Gate oxide trade-off: alumina vs. hafnia

Finally, we compare two otherwise identical FinFET structures of Fig. 1, changing only the gate oxide material from Al_2O_3 ($m^*_{\rm ox} = 0.4m_{\rm e}$, $\varepsilon_r = 7.8$, and an electron affinity [19] producing a 2.56 eV band offset within the electron-affinity rule) to HfO_2 ($m^*_{\rm ox} = 0.08m_{\rm e}$, $\varepsilon_r = 22.3$, and an electron affinity [20] producing a 2.46 eV band offset). The *physical* thickness of the gate oxide is kept at $t_{\rm ox} = 2$ nm in both cases as a control, although in practice a greater physical thickness would be expected for the higher-k material.

HfO_2, with a larger ε_r and therefore thinner EOT for a given physical gate oxide thickness, exhibits superior short channel control in terms of S and $DIBL$ (Table III). A more interesting comparison is the ON-state performance. Use of Al_2O_3 leads to weaker electrostatic coupling, and generates a smaller inversion charge density than the use of HfO_2 (Fig. 4, right-axis). However, with a heavier $m^*_{\rm ox}$, use of Al_2O_3 produces smaller quantum corrections in our model, and thus relatively more Γ-valley carriers in the channel and larger carrier velocities as compared to the use of HfO_2 (Fig. 4, left-axis). The counterbalance between degraded electrostatics but moderated quantum confinement effects leads to nearly equal

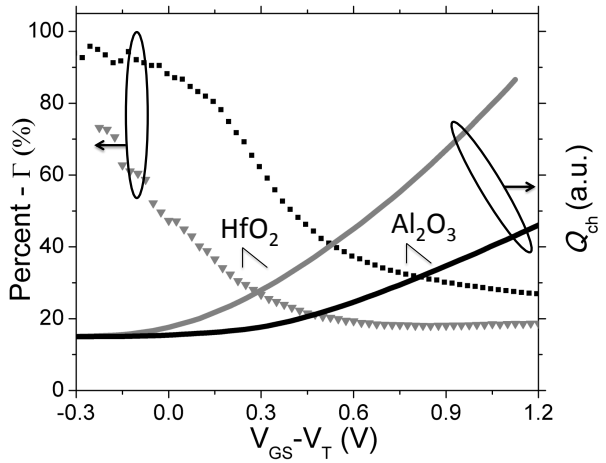

Fig. 4: Trade-offs between Al_2O_3 and HfO_2 gate dielectrics. Al_2O_3 (black), with its smaller dielectric constant than HfO_2 (gray), generates a smaller inversion charge density $Q_{\rm ch}$ (right-axis). However, with its heavier effective mass and smaller quantum confinement, Al_2O_3 retains more Γ-valley carriers than HfO_2 (left-axis).

TABLE III: Variation of gate oxide material stack

Gate oxide	Al_2O_3	HfO_2
ε_r (ε_0)	7.8	22.3
$m^*_{\rm ox}(m_{\rm e})$	0.4	0.08
EOT (nm)	1.0	0.35
$g_{\rm M}$ (mA/μm/V)	2.4	2.5
S (mV/dec)	76	68
$DIBL$ (mV/V)	94	55

channel $g_{\rm M}$ between the materials (Table III).

VI. Conclusion

Performing EMC simulations with state-of-the-art quantum corrections, we have shown that FinFET devices with light-mass III-V channels may be sensitive to the gate oxide's complex band structure via its impact on channel confinement. For the common device structure considered here, we have found that heavier-mass Al_2O_3, even with a smaller dielectric constant and larger EOT for the same physical oxide thickness, compares well against HfO_2 in the ON-state due to reduced carrier confinement conditions. Qualitatively, these results suggest that Al_2O_3 may be preferred to HfO_2 at the same EOT. A larger oxide dielectric constant provides increased gate capactitance. However, a larger oxide effective mass reduces quantum confinement while also reducing the wavefunction penetration depth in the oxide. Therefore, combining a heavy-mass interface oxide with an over-layer oxide with a large dielectric constant could provide both benefits simultaneously. (Notably, such a combination already exists in Si-channel devices with high-k gate stacks incorporating heavy-mass native oxide SiO_2 surface layers. However, less and less deleterious—and some even beneficial—quantum confinement occurs in Si devices [7], [15]). Finally, we focused on the effect of differing oxide $m^*_{\rm ox}$ on device performance (here with the band offsets/barrier heights expected to be much the same for HfO_2 and Al_2O_3 [19], [20]). More generally, this work suggests that anything that significantly affects the boundary conditions on the quantum mechanical wavefunction at the channel-gate dielectric interface may impact device performance, especially for strong quantum confinement as expected in scaled III-V based n-channel MOSFETs.

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