Interplay between quantum mechanical effects and a discrete trap position in ultra-scaled FinFETs

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Abstract: **In this work we establish a link between positions of a single discrete charge trapped in an oxide interface and between the performance of ultra-scaled FinFET transistors. The charge trapped in the oxide induces gate voltage shift (ΔV_G). This ΔV_G is presented as a function of the device geometry for two regimes of conduction – from a sub-threshold to an ON-state. For specific trap positions in the oxide, we show that the trap impact decreases with scaling down of the FinFET size and of the applied gate voltage. We also compare the Drift-Diffusion (DD) calculations with the Non Equilibrium Green Functions (NEGF) simulations in order to investigate the importance of quantum charge confinement in transport and of reliability resilience in ultra-scaled non-planar transistors, such as FinFETs.**

I. INTRODUCTION

Ultra-scale non-planar multi-gate transistors have become dominant architectures for the sub-22-nm technology [1]. However, even though the multi-gate transistors provide superior options for scalability, they also suffer from negative effects of various sources of variability [2-4]. For example, interface traps represent a non-negligible source of variability in ultra-scaled low-doped channel devices, such as FinFETs [4-6]. Therefore, in order to fully understand the nano-scaled FinFET performance it is essential to establish a correlation between the positions of the oxide-trapped charges in the presence of a strongly confined quantum effect and the device performance. It should be noted that the fin shape and the dimensions of the simulated FinFETs require quantum mechanical treatment of the electron transport [7]. For this reason in this paper we compare the threshold voltage shift amplitude (ΔV_G) obtained from the DD and NEGF computational results. We also study the impact of the device scaling on the gate voltage shifts associated with a single trapped charge and we investigate the influence of specific positions of the single trapped charge in the gate oxide on the FinFETs reliability performance.

II. METHODOLOGY

All simulations are carried out by a means of the DD module (including density-gradient quantum corrections) and the mode space NEGF approach module of the GSS atomistic
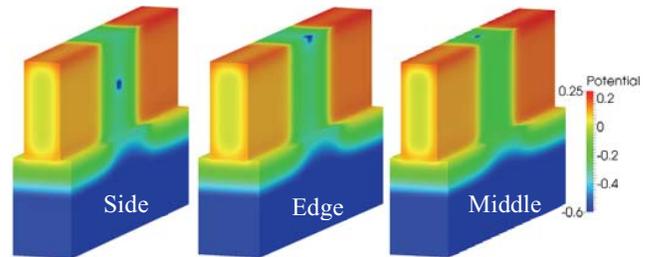

Fig. 1 Electrostatic potential for the L_G=15 nm FinFET. A single discrete trap is located on the <u>side</u> (left) of the vertical oxide, at the <u>edge</u> of the fin (middle) and in the <u>middle</u> of the top oxide (right).

TABLE I
GEOMETRICAL DIMENSIONS AND MAIN CHARACTERISTICS FOR ALL FINFETS STUDIED IN THIS WORK.

Gate Length (L) [nm]	Fin Width (W_{FIN}) [nm]	Fin Height (H_{FIN}) [nm]
5	2	15
10	4	15
15	6	15

simulator GARAND [8, 9]. For the purpose of this work, we assume ballistic transport without scattering and absence of statistical variability. The ratio between the fin width and channel length is kept constant (see Table I) when scaling down the devices in order to maintain electrostatic integrity. Due to a single trapped charge located in the oxide, the gate voltage shifts (ΔV_G). This shift is evaluated by the transistor transfer characteristics in the sub-threshold regime (V_G=0.05V) and in the ON-state regime (V_G=0.6V) at low drain biases (V_D=0.05V). The effective oxide thickness is 0.8 nm. The doping concentration in the source/drain region is 1e20 [cm^-3] and in the channel it is 1e14 [cm^-3]. We consider only four of the six lowest valleys of the Si conduction band [9]. The effective masses correspond to their bulk values for <100> crystal orientation in Si: m_l=0.916*m_0 and m_t=0.19*m_0. It is important to point out that the effective masses do not scale with the device size in our calculations. This might be not sufficient for devices with severe charge confinement [10]. Further investigation is required and it is currently being undertaken.
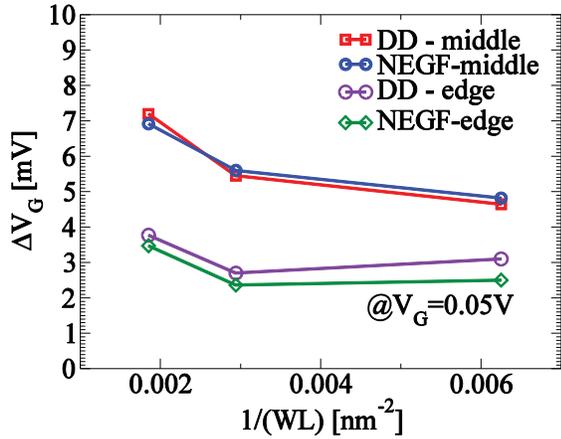
Fig. 2 Gate voltage shift due to a single discrete trapped charge at the edge of the fin and in the middle of the top oxide as a function of the FinFET active area size obtained by the DD and NEGF simulations with a current reading criterion in the *sub-threshold region (100nA)*. Note, here $W=W_{FIN}+2\times H_{FIN}$.

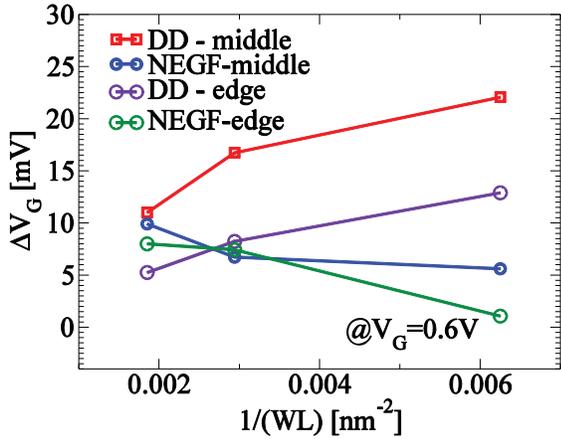Fig. 4 Gate voltage shift due to a single discrete trapped charge located on the side of the vertical oxide, at the edge of the fin and in the middle of the top oxide as a function of the FinFET active area size obtained by the DD and NEGF simulations with a current reading criterion in the *sub-threshold region (100nA)*.

Fig. 3 Gate voltage shift due to a single discrete trapped charge at the edge of the fin and in the middle of the top oxide as a function of the FinFET active area size obtained by the DD and NEGF simulations with a current reading criterion in the *ON-current region (71μA)*.

Fig. 5 Gate voltage shift due to a single discrete trapped charge located on the side of the vertical oxide, at the edge of the fin and in the middle of the top oxide as a function of the FinFET active area size obtained by the DD and NEGF simulations with a current reading criterion in the *ON-current region (71μA)*.

III. RESULTS

Fig.1 shows the electrostatic potential for a device with the gate length of 15 nm and the fin width of 6 nm. A fingerprint of a single trap located in the middle of the top oxide, at the edge of the top oxide and in the middle of the side oxide (Fig.1) is clearly visible.

Fig.2, Fig.3, Fig.4 and Fig.5 reveal the threshold voltage shift amplitude (ΔV_G) obtained for a current reading of 100nA and 71μA as a function of scaling. ΔV_G is obtained as the change of the gate voltage, allowing the same drain current for the empty (neutral) and the filled (negatively charged) trap.

Fig.2 and Fig.3 present the ΔV_G results at current reading of 100nA and 71μA, respectively, for two types of devices – one with the edge and another one with the middle trap position. Fig.2 shows that both transistors have a similar performance, with a surprising 'inverse-scaling' behaviour. Indeed, the impact of the trap located on top oxide of the fin increases when the fin size increases. This behaviour is opposite to the trend expected in conventional planar MOSTEFs [11, 12].
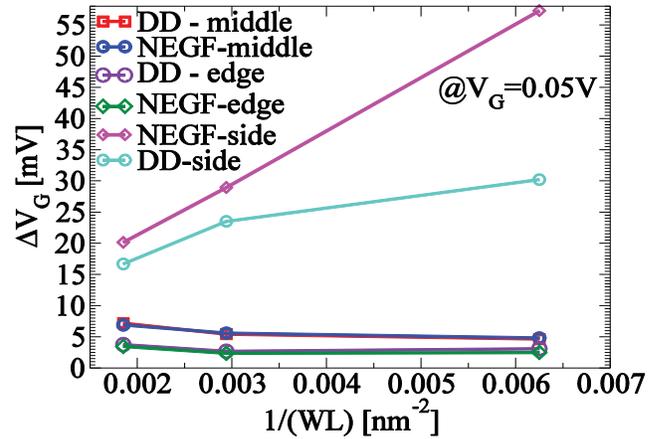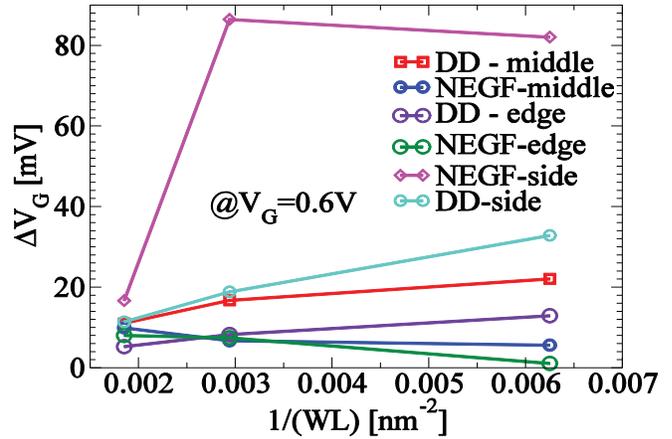
Moreover, Fig.3 shows the scaling of ΔV_G for the same two types of devices in the ON-state regime based on the DD and NEGF simulations. In this case the DD simulations show results that are consistent with a planar bulk transistor. Also, the NEGF calculations reveal lower ΔV_G values with a trend similar to the behaviour from Fig.2. Additionally, ΔV_G increases when moving from the sub-threshold to the ON-state region, in contrast to what is confirmed by conventional planar MOSFETs. It is important to point out that the DD and NEGF results confirm a positive trend between the ΔV_G value and the gate drive voltage.

However, an expected scaling trend is obtained for the transistor with the side trap position, which is shown in Fig.4. In Fig.4 we also observe discrepancies in the ΔV_G trends between devices with traps on the top oxide and the device with the charged trapped on the side oxide. Also, for the side device the DD and NEGF results reveal a similar behaviour where both types of calculations reveal the expected scaling trends.
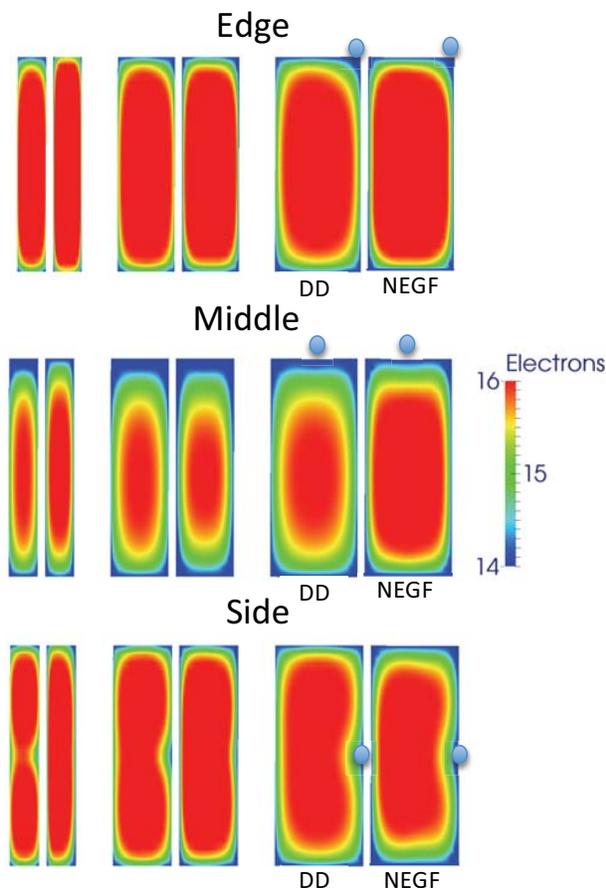
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Fig. 6 2D cross-sections (at the center of the channel) of the simulated electron density at the threshold voltage conditions for a current criterion in the *OFF-state regime (V_G=0.05V)*. The left (right) of each couple of the FinFET cross-sections represents the DD (NEGF) results. Top: FinFETs with the trap in the edge (top right corner); Middle: Transistors with the trap in the middle of the top oxide; Bottom: Transistors with the trap at the side of the fin (in the middle of the vertical right oxide).
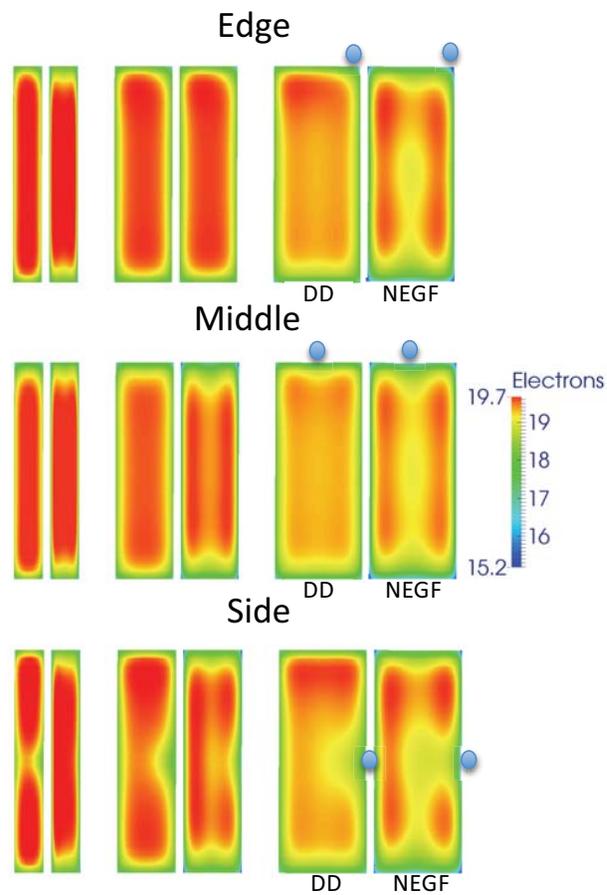
Fig. 7 2D cross-sections (at the center of the channel) of the simulated electron density at the threshold voltage conditions for a current criterion in the *ON-state regime (V_G=0.60V)*. The left (right) of each couple of the FinFET cross-sections represents the DD (NEGF) results. Top: FinFETs with the trap in the edge (top right corner); Middle: Transistors with the trap in the middle of the top oxide; Bottom: Transistors with the trap at the side of the fin (in the middle of the vertical right oxide).

Fig.5 shows the ΔV_G values and trends for all devices discussed in this work in the ON-state regime. It is clear from this figure that the DD calculations show the expected scaling behaviour. The NEGF curve for the side device shows behaviour that is close to the DD trend.

In order to understand the ΔV_G trends observed in the tri-gate architecture, in Fig.6 and Fig.7 we report the simulated 2D charge density at V_G=0.05V and V_G=0.60V correspondingly. Fig.6 shows that the channel inversion occurs deeply inside the bulk in the OFF-state regime and the profile of the charge distribution is similar for both the DD and NEGF simulations. As a result, the ΔV_G results reported in Fig.2 and Fig.4 have a similar trend with close values.

However, Fig.7 reveals a different 2D charge distribution profile obtained with the NEGF and DD simulation methodology. From this figure we can draw the following important conclusions. Firstly, in all devices, the charge distribution moves closer to the oxide interface in the ON-state regime. This behaviour explains why the trap impact increases with increasing of V_G (a common feature for the DD and NEGF simulations). It should be noted that this behaviour cannot be observed in the conventional planar MOSFET

where the inversion charge centroid is always close to the oxide interface and barely modulated by the gate voltage conditions.

Secondly, the DD and NEGF charge distributions differ in the ON-state regime: while the DD charge moves uniformly towards the fin top interface, the NEGF charge follows a similar trend but it maintains two distinct peaks close to the lateral fin sidewalls. More importantly, it is evident that the DD charge distribution is mainly localised at the top interface of the fin, while the NEGF solution of the charge shows that it is predominately positioned at the vertical sidewalls of the fin. Also, the single trap charge in the oxide breaks the symmetry of the 2D charge distribution, which is visible at the 2D charge density plots for each device.

Additionally, it is important to point out that the device with the side trap shows the expected scaling behaviour at V_G=0.05V and V_G=0.6V (see Fig.4 and Fig.5). The main reason being that the charge inversion layer moves from the bulk body to the surface of the lateral gates. Moreover, the distribution of the charge along the length of the side gate is uniform and the profile is similar to what is observed in the planar MOSFETs.

Fig. 8 ΔV_G as a function of the trap position along the top oxide of FinFETs. The trap is moved from the edge of the fin to the middle of the top oxide.

Fig. 9 ΔV_G as a function of the trap position along the side oxide of FinFETs. The trap is moved from the edge of the fin to the middle of the side oxide.

In order to clarify the link between the 2D charge distribution and ΔV_G we calculate sensitivity maps, which are shown in Fig.8 and Fig.9. Fig.8 presents the sensitivity map where the trap is moved with a step of 0.5 nm from the edge of the fin to the middle of the top oxide. In Fig.9 the trap is moved from the edge of the fin to the centre of the side oxide with a step of 1 nm.

The results presented in Fig.8 and Fig.9 can be summarised in the following way. Both the DD and NEFG simulations show a specific behaviour. For example, in Fig.8, when the trap moves from the middle to the edge of the device, both the DD and NEGF calculations show a constant increase of the values of ΔV_G. Also, values for ΔV_G obtained with the NEGF method are higher than for the DD calculations in most cases. The only exception is the middle device where the NEGF calculations give a number lower than the DD simulations. The reason for this is that in the NEGF case most of the charge inversion happens close to the corners of the device. Hence, the trap placed there in the NEGF simulations has a smaller impact on ΔV_G.

Moreover, in Fig.9 the difference between the NEGF and DD results is even more pronounced. Moving a trap from the edge of the device to the side reveals a different behaviour for the DD and NEGF calculations. The impact of ΔV_G in the DD case is almost constant, while in the NEGF case the sensitivity curve shows an oscillating behaviour. The main reason being that the quantum effects lead to maintaining of two distinct peaks close to the lateral fin sidewalls. This is related to the complex 2D quantum charge distribution, especially at a high gate bias.

IV. CONCLUSIONS

In this paper we presented calculations based on the 3D Drift-Diffusion and NEGF simulations, where we investigated the impact of the single discrete trapped charge on the performance of ultra-scaled nMOS FinFET transistors. The gate voltage shift was evaluated for three device sizes, several trap positions and for two regimes of conduction: sub-threshold and ON-state. We showed that in the sub-threshold region, due to the FinFET volume inversion, the trap located on the top oxide and the edge can show an 'inverse-scaling' behaviour contrary to what is expected in the conventional planar MOSFETs. However, the trap located on the side oxide of the FinFETs shows the expected gate voltage shift behaviour. More importantly, we showed that the quantum effects in charge distribution play an important role in evaluating the reliability issues in ultra-scaled devices.

V. ACKNOWLEDGMENT

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[12] S. M. Amoroso, C. M. Compagnoni, A. Ghetti, L. Gerrer, A. S. Spinelli, A. L. Lacaita, *et al.*, "Investigation of the RTN Distribution of Nanoscale MOS Devices From Subthreshold to On-State," *Ele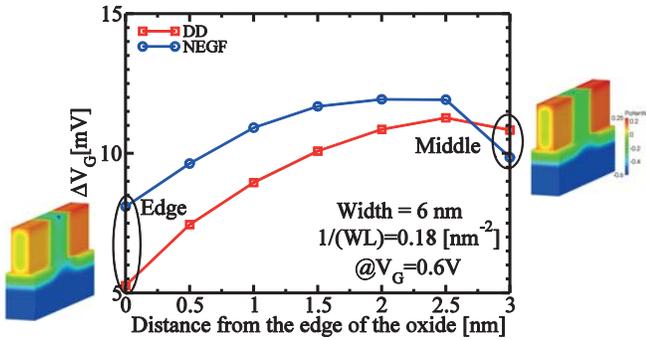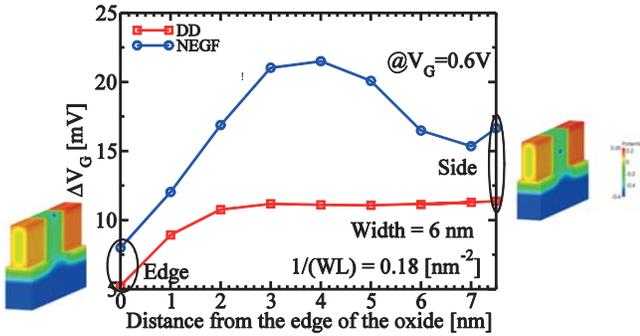ctron Device Letters, IEEE*, vol. 34, pp. 683-685, 2013.