Extending Drift-Diffusion Paradigm into the Era of FinFETs and Nanowires

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***Abstract*—This paper presents a feasibility study that the drift-diffusion model can capture the ballistic transport of FinFETs and nanowires with a simple model extension. For FinFETs, Monte Carlo simulation is performed and the ballistic mobility is calibrated to linear & saturation currents. It is validated that the calibrated model works over a wide range of channel length and channel stress. The ballistic mobility model is then applied to a nanowire with 5nm design rules. Finally, the technology scaling trend of the ballistic ratio is explored.**

Keywords—Ballistic transport; FinFETs; Nanowires; Drift-Diffusion; Quantum transport solver; NEGF; Monte Carlo simulation; Subband Boltzmann transport equation solver

I. Introduction

With channel length scaling, the electron and hole transport in transistors is expected to become increasingly ballistic [1], which can be modeled by Monte Carlo (MC) simulation, the deterministic subband Boltzmann approach [2], or Quantum transport (wavefunction formalism, NEGF formalism) [3], [4]. This nearly ballistic transport can also be simulated by the drift-diffusion (DD) model by introducing a concept of ballistic mobility [1], [5-7].

The computational cost and maturity of the DD model is well suited to technology optimization work. Here, we evaluate extending DD simulation with a ballistic mobility model and apply it to FinFET and nanowire technologies. Through this approach, the ballisticity trend is examined as the device technology evolves into the nanowire era.

II. Simulation Model

Here, we use several advanced transport approaches: Monte Carlo (MC) simulation [8], Quantum transport solver (QTSolver) [9], subband Boltzmann transport solver (sbandBTE) [10] as a reference to calibrate the DD ballistic mobility model (Fig. 1) and then apply it to FinFETs and nanowires (NW) that are scaled down to 2nm design rules.

Monte Carlo simulation is used to simulate FinFETs (the channel length down to 12nm). QTSolver simulation is done to model 5nm node gate-all-around (GAA) nanowire FETs in the ballistic limit. QTSolver solves the multi-dimensional Schrödinger equation with open boundary conditions. The ballistic ratio is calculated using sbandBTE. sbandBTE solves the Schrödinger equation on two dimensional slices along the channel and then the one-dimensional Boltzmann transport equation along the channel. sbandBTE can model carrier transport with and without scattering (phonon and surface roughness scattering).

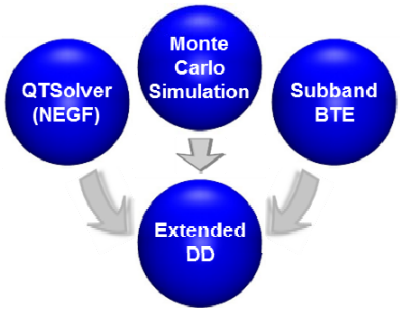

Fig. 1. Modeling methodology

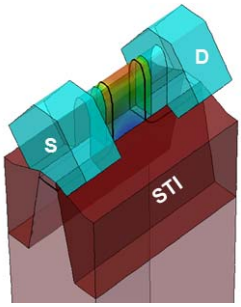

Fig. 2. 3D N-FinFET view (Channel length split from 12nm to 450nm. Fin width=5nm. EOT=8.5Å. Fin pitch=45nm. Gate pitch=60nm. VDD=0.7V. Undoped channel and source/drain doping of 2e20cm^{-3}.)

III. FinFET Application

A Si N-FinFET (Fig. 2) with different channel lengths is modeled by 3D Monte Carlo simulation at low (Vds=50mV) and high (Vds=0.7V) drain biases (Fig. 3). The channel length is swept from 12nm to 450nm. The fin width is 5nm, EOT is 8.5Å, the fin pitch is 45nm, the gate pitch is 60nm, VDD is 0.7V, the channel is undoped, and the source/drain doping is 2e20cm^{-3}. The gate workfunction is adjusted to keep off-state current at 1 nA/μm. At channel lengths below 50 nm, the

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deafult DD model overestimates the currents similar to observations in [11].

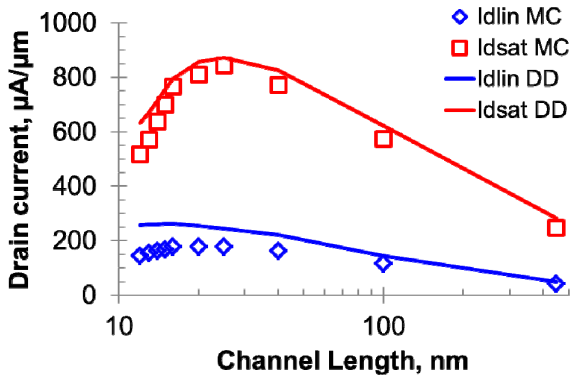

Fig. 3. N-FinFET with 2GPa tensile stress w/o ballistic mobility in Drift-Diffusion (Off-state current=1 nA/µm)

The ballistic mobility is proportional to the channel length:

$$\mu_{\_BAL}=k\cdot L_g \quad (1)$$

where k is the proportional coeficient and L_g is the channel length.

For the detailed analysis, 2D double-gate (DG) FET is simulated and the effective mobility of FinFETs (L_g=12nm~450nm) is extracted by measuring the carrier velocity and the gradient of the quasi-Fermi potential at the middle of the channel from MC results, as in [7]. The effective mobility reduces towards shorter channels for the several fin widths (5nm, 8nm, 10nm) (Fig. 4) and the different stress levels (0GPa, 1GPa, 2GPa) (Fig. 5). The ballistic mobility is evaluated from the effective mobility and the long channel mobility, assuming Matthiessen's rule:

$$1/\mu_{\_eff} = 1/\mu_{\_BAL} + 1/\mu_{\_scattering} \quad (2)$$

The long channel mobility is assumed to be the scattering-limited mobility ($\mu_{\_scattering}$). It is observed that the ballistic mobility converges to the unified model across different fin widths (Fig. 6) and different stress levels (Fig. 7). Therefore, once the ballistic mobility is calibrated to a certain technology node, the model can be used for technology development of that node.

With the calibration of the ballistic mobility model and the high-field saturation velocity model, DD can describe the behaviors of 3D N-FinFET (Fig. 8) and 3D P-FinFET (Fig. 9) in a wide range of channel lengths scaled down to 5nm design rules and across different channel stresses.

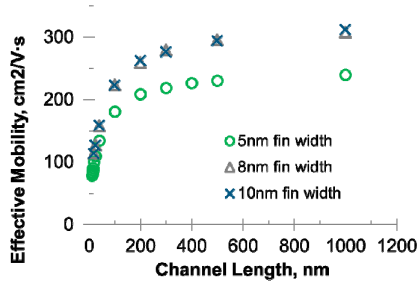

Fig. 4. Effective mobility from Monte Carlo simulation vs. channel length for different fin widths

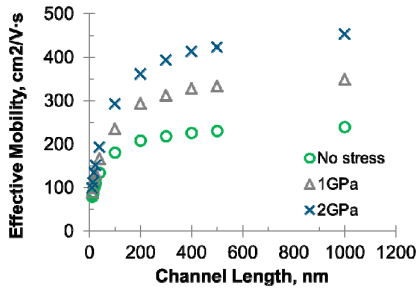

Fig. 5. Effective mobility from Monte Carlo simulation vs. channel length for different channel stresses

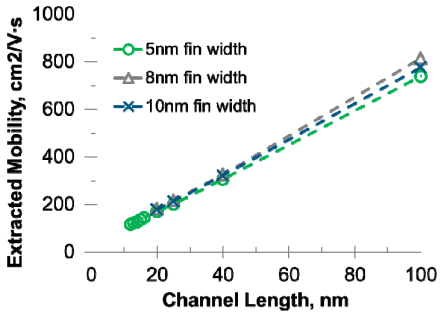

Fig. 6. Ballistic mobility for different fin widths

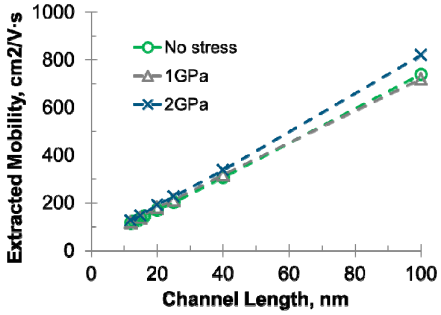

Fig. 7. Ballistic mobility for different stress levels

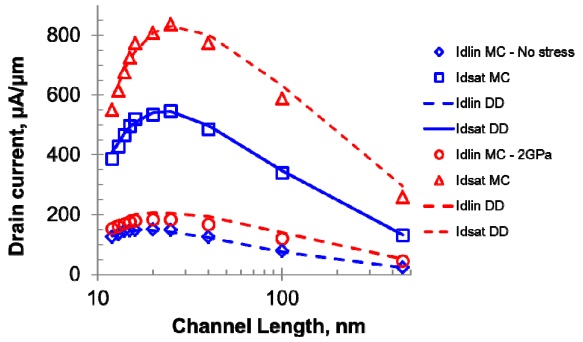

Fig. 8. Monte Carlo simulation vs Drift-Diffusion model with ballistic mobility for 3D N-FinFET (L_g=12nm~450nm, channel stress=0GPa,2GPa)

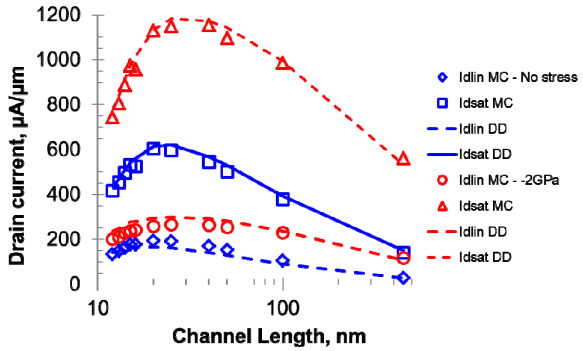

Fig. 9. Monte Carlo simulation vs Drift-Diffusion model with ballistic mobility for 3D P-FinFET (L_g=12nm~450nm, channel stress=0GPa,-2GPa)

IV. Nanowire Application

It has been reported that the gate-all around (GAA) nanowire (NW) provides a performance advantage over FinFETs at 5nm design rules due to the better channel control and lower parasitic capacitances [12]. We perform analysis of Si NW FET with round channel cross-section (Fig. 10) scaled to 5nm design rules. The channel length of the NW FET is 11nm, EOT is 8Å, the diameter of the channel is 5nm, the diameter of the source/drain is 10nm, the channel direction is <100>, the fin pitch is 16nm, the gate pitch is 30nm, VDD is 0.7V, the channel is undoped, and the source/drain doping is 2e20cm^{-3}. The off-current is normalized to 1nA/µm.

First, the ballistic mobility is calibrated to the QTSolver results for the cylindrical nanowire. Extended DD (with ballistic mobility) matches PMOS and NMOS NW IV curves with QTSolver in the entire range of gate bias for 0.05V and 0.70V drain biases (Fig. 11). Second, assuming only the ballistic transport in the channel and the actual models in the source/drain, the IdVg curve (Fig. 12) is simulated with the extended DD model. The larger diameter (10nm) of source/drain is assumed, which decreases the source/drain extension resistance. A doping-dependent mobility model and realistic contact resistance are included in the source/drain.

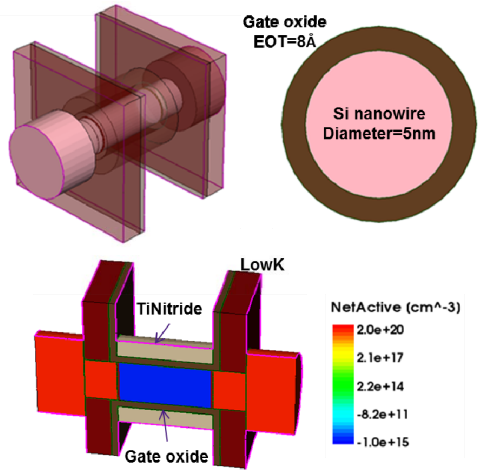

Fig. 10. Gate-all-around (GAA) nanowire geometries and doping (Channel length==11nm. NW channel diameter=5nm. Source/drain diameter=10nm. EOT=8Å. Fin pitch=16nm. Gate pitch=30nm. VDD=0.7V. Undoped channel and source/drain doping of 2e20cm^{-3}.)

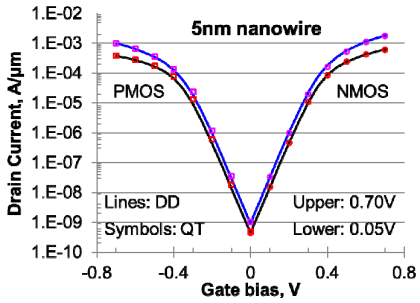

Fig. 11. Nanowire: Quantum Transport & Drift-Diffusion with ballistic mobility

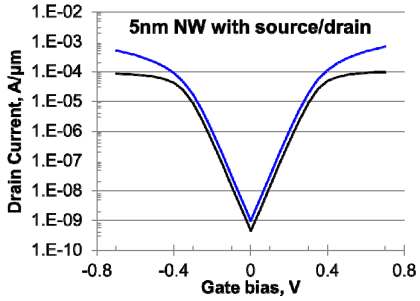

Fig. 12. Nanowire: Extended Drift-Diffusion with the source/drain model

V. Ballistic Ratio

Ballisticity has been historically increasing with scaling of planar FETs and FinFETs [13], [14]. However, as the diameter of the NW shrinks, surface roughness scattering increases [2], [15], [16] and becomes a dominant factor. It is therefore interesting to investigate the technology trend of the ballistic ratio including planar FETs, FinFETs, and NW FETs.

sbandBTE [9] is employed for this analysis in order to model both ballistic transport and diffusive transport with phonon and surface roughness scattering. The ballistic ratio is calculated by the ratio of the diffusive current to the ballistic current.

Distribution functions versus position and momentum of the NW FET are illustrated for ballistic transport and diffusive transport (Fig. 13). The ballistic distribution of Fig. 13 shows the electron distribution with the positive velocity (drain bound) in the channel region, but the scattered distribution of Fig 13 demonstrates the source-bound electron distribution in the channel due to the scattering.

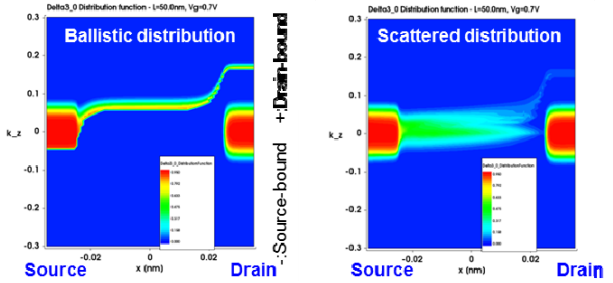

Fig. 13. Distribution functions for nanowire with ballistic transport and with phonon and surface roughness scattering

Fig. 14 plots the trend of the ballistic ratio. The ballistic ratio increases as the channel length shrinks in the planar FET and the FinFET technologies. However, as the gate length is scaled, the diameter of NW FET should be reduced to maintain strong gate control. At small diamters, surface roughness scattering starts to dominate in the NW era and both phonon and surface roughness scattering increase. The ballistic ratio is therefore seen to decline as the NW is scaled.

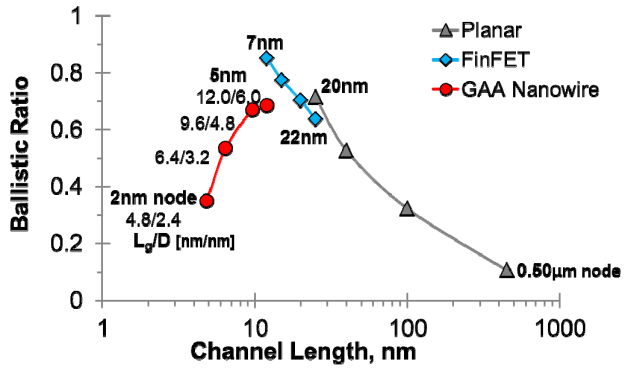

Fig. 14. Evolution of ballistic ratio for planar FETs, FinFETs, and nanowires (Ballistic ratio is for the historic transistor scaling in the industry down to 14nm node and it is projected for the expected transistor scaling down to 2nm node.)

VI. Conclusions

A simple ballistic mobility model has been demonstrated to capture FinFET and NW FET behavior in a wide range of design rules and stress levels and therefore provides a pragmatic way to extend DD into the era of Si FinFETs and NW at least down to 2nm design rules. The prediction of the scaling trend of the ballistic ratio is presented and the results show that the ballistic ratio stops increasing in NW FET nodes due to increased surface roughness and phonon scattering.

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