Impact of S/D Tunneling in Ultrascaled Devices, a Multi-Subband Ensemble Monte Carlo Study

C. Medina-Bailon*[†], C. Sampedro*[†], F. Gamiz*[†], A. Godoy*[†] and L. Donetti*[†]
* Nanoelectronics Research Group, Universidad de Granada, 18071 Granada, Spain.

[†] CITIC, Universidad de Granada, 18071 Granada, Spain.

e-mail: cmedba@ugr.es

Abstract—Because of the scaling of electronic devices, quantum effects play an important role on their characteristics which are becoming more and more dominant as transistors approach to nanometer scales. Therefore, the inclusion of these effects in advanced device simulators will be mandatory to predict the behavior of future transistors targeting sub-10nm nodes. This work implements Source-to-Drain Tunneling mechanisms (S/D tunneling) in Multi-Subband Ensemble Monte Carlo (MS-EMC) simulators showing the importance of quantum transport effects and the possibility of being implemented in a reliable way on advanced device simulators.

I. INTRODUCTION

To achieve higher integration density, lower power consumption and delay time, electronic devices have been scaled down for more than 40 years. As the nanoscale is reached, it has been mandatory the inclusion of additional phenomena to explain its behavior. Quantum effects in the confinement direction were taken into account in a first step as the channel thickness was reduced to improve scalability. However, nowadays channel length is approaching 10 nm in the development stage, quantum effects in the transport direction also start to play a significant role. In particular, Source-to-Drain tunneling (S/D tunneling) is expected to set a scaling limit [1], [2] as already demonstrated in ballistic Non-Equilibrium Green Functions (NEGF) simulations. S/D tunneling can introduce a nondesired effect in electronic devices, especially in subthreshold bias conditions, because electrons can be injected from source to drain without any gate control. This work presents a meticulous study of this effect in ultra-scaled Double-Gate Silicon-On-Insulator transistors (DGSOI) by means of a Multi-Subband Ensemble Monte Carlo (MS-EMC) simulator.

II. SIMULATION SET-UP

In this work, S/D tunneling effect has been developed in the frame of a MS-EMC simulator, which has already demonstrated its capabilities studying a large range of nanodevices [3]–[6]. This algorithm is based on the mode-space approximation of quantum transport [7] where the system is decoupled in the confined direction and the transport plane as depicted in Figure 1. The Schrödinger equation and the BTE are solved respectively and are coupled with the 2D Poisson equation to keep the self-consistency of the simulator. The main advantage of this tool against NEGF is the reasonable computational time when scattering mechanisms and quantum

effects on the ultrascaled devices are taken into account. In addition, MS-EMC simulator can enable to switch on and off S/D tunneling in order to determine the impact of such process in a direct way.

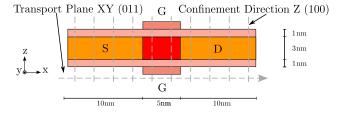


Fig. 1. DGSOI structure analyzed in this work. 1D Schrödinger equation is solved for each grid point in the transport direction and BTE is solved by the MC method in the transport plane.

The model developed here is an extension of the non-local band-to-band tunneling algorithm [8]. In that work, the tunneling path for electrons started in the Valence Band and finished in the Conduction Band. In the case under study, the tunneling path and probabilities are calculated considering the starting and finishing points in the Conduction Band.

The MS-EMC simulator is based on the stochastic and ergodicity processes in which the motion of an electron is studied in the transport direction over a random flight time. This period finishes because of the random choice of a scattering event. After each flight of an electron, its new position is calculated. In a semiclassical approximation if the total energy of this electron is lower than the minimum of the corresponding subband at this position, it will rebound from the potential barrier in the point where the electron and subband energies are the same. In the case of S/D tunneling, the electrons would rebound from the potential barrier or would tunnel through the barrier. For this reason, the first step is to determinate the probability of tunneling through the barrier at a specific energy. Then, if the electron suffers from S/D tunneling, it is necessary to calculate the tunneling path to completely determine its new position.

The tunneling probability of the electron T_{dt} is calculated using the WKB approximation [9]:

$$T_{dt}(E) = \exp\{-\frac{2}{\hbar} \int_{a}^{b} \sqrt{2m_{tr}^{*}(E_{c}(x) - E)} \,dx\}.$$
 (1)

Where a and b are the starting and ending points, E and m_{tr}^* are the energy and transport effective mass of the electron respectively and $E_c(x)$ the energy of the corresponding subband. This approximation has already been used to study Schottky contact MOSFETs [10]. In this work, thanks to the detailed description of the subband structure provided by the MS-EMC simulator, T_{dt} has been calculated for each electron considering the minimum of the energy of its subband instead of the Conduction Band [11].

Because of the stochastic nature of this effect, a uniformly distributed random number r_{dt} between 0 and 1 is chosen. If $r_{dt} \leq T_{dt}$, the electron will go through the barrier and the particle will be marked to show that it is suffering S/D tunneling. In addition, that particle will be drifted in a ballistic way whereas it is in a region inside the barrier. On the other hand, if $r_{dt} > T_{dt}$, it will turn back with $v_x = -v_x$.

Several assumptions have been considered after each integration step to enhance the calculation of T_{dt} . The exact starting and ending points where the electron goes through the barrier are calculated. A maximum tunneling rejection length is also introduced (L_{max}) . If the path of a electron suffering S/D tunneling from the starting point to a specific integration step is higher than L_{max} , the calculation of T_{dt} stops. In this work, a L_{max} equal to L_G has been considered. As can be extracted from equation 1, the longer the tunneling path the smaller T_{dt} is. For this reason, if the comparison is included after each step of integration, when $r_{dt} > T_{dt}$, the calculation of T_{dt} can be stopped. Then, the electron automatically would rebound from the potential barrier flying to the source. As a result, the benefits of including these considerations in the integral calculation are a reduction of the computational effort and an accurate value of T_{dt} . However, the limitation of this code is the integration time of the tunnel probability.

Subsequently, it is necessary to find the most probable tunneling path. If we assume that all the electrons reach the potential barrier in the starting point with normal direction, the tunneling path can be easily found considering Newton mechanics in the inverted potential $V(\vec{r}') \rightarrow -V(\vec{r}')$ and energy $E \rightarrow -E$ [12]. In this system, the potential barrier becomes a valley and electrons go through it undergoing the electric field obtained from this new potential profile.

This classical trajectory could be found by the following steps (Fig. 2). Firstly, an imaginary particle is placed at the starting point a in minimum of its energy subband with zero kinetic energy. Before starting its tunneling path, the angle, which determines the relationship between k_x and k_y and, as a consequence, its flight direction, is maintained. Then, it enters the valley where it is accelerated in accordance with Newton's second law of motion. Finally, it appears at some

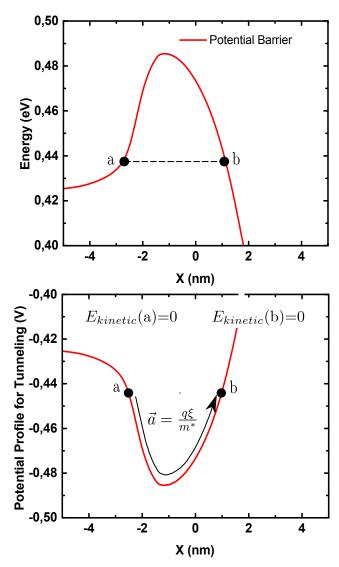


Fig. 2. Representation of the tunneling model: The potential barrier (top) is inverted and the particle follows a classical path obeying Newton's second law of motion (bottom).

point *b* in the minimum of its subband with zero kinetic energy. That particle continues to flow into the device with the same transport properties.

III. RESULTS AND DISCUSSION

In order to perform this in-depth study of S/D tunneling in ultra-scaled devices, DGSOI transistors were analyzed with a channel thickness of $T_{Si}=3$ nm, EOT=1 nm and a gate length ranging from 5 nm to 15 nm as shown in Figure 1. The doping profile has been chosen to follow an abrupt Gaussian lateral decay as shown in Figure 3.

The inclusion of this effect has an important impact on $I-V_G$ characteristics in all ballistic and diffusive regimes. I_D vs. V_{GS} curves with $V_{DS}=100mV$ for the different

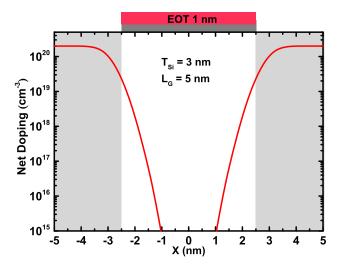


Fig. 3. Simulated DGSOI structure including net doping profile.

regimes are represented in Figure 4. An increase in current is observed when this effect is included because of the number of electrons that flow from source to drain are higher. In addition, this effect becomes more important near the threshold voltage (V_{th}) where tunneling contributes in an important way to increase the leakage current. It therefore introduces an important reduction of in the threshold voltage.

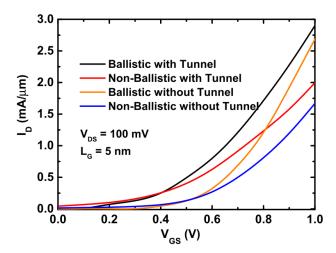


Fig. 4. I_{DS} vs. V_{GS} at low drain bias with and without considering S/D tunneling, and ballistic or diffusive transport description.

For a better understanding of how S/D tunneling affects the motion of the electrons, it is necessary to study its position after each free flight. When an electron near the potential barrier suffers this tunnel effect it goes through the barrier instead of rebounding from it. For this reason, it is essential to study the population of each subband insofar as the total energy and position in the transport plane of each electron are concerned. Figure 5 represents the population of each

subband in relation to the total energy and the position along the transport plane for ballistic (top) and non-ballistic (bottom) transport conditions. When S/D tunneling is included, the population under the potential barrier of this subband, which is a forbidden region for electrons, is not zero whereas when this mechanism is not considered it is empty. Our simulations shows that this change modifies the height of the potential barrier and increases the drain current. This effect is of special interest when the ballistic transport is taken into account instead of a simulation with non-ballistic models because scattering reduces its effectiveness.

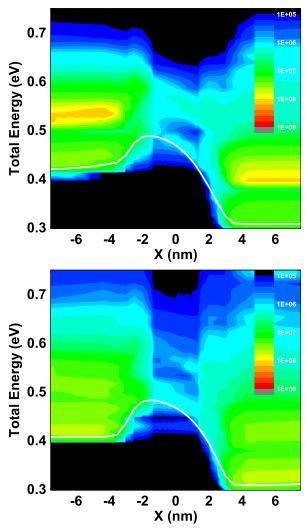


Fig. 5. Electron distribution (a.u.) as a function of total energy in the 5nm device including S/D tunneling under ballistic (top) and diffusive (bottom) transport with $V_{GS}=0.8V$ and $V_{DS}=100mV$.

The presence of charge under the barrier also affect the electrostatics of the system changing the subband profile as shown Figure 6. When this effect is taken into account, the number of electrons with enough energy to surmount the

barrier is lower because they can go through it in a lower energy state. For this reason, the potential barrier is higher when S/D tunneling is considered.

On the other hand, the reduction of V_{th} is more significant as the dimensions of the device are reduced as depicted in Figure 7. It therefore provides the importance of quantum effects in the transport direction, such as S/D tunneling, at such a small scale. This effect becomes more remarkable under ballistic transport conditions.

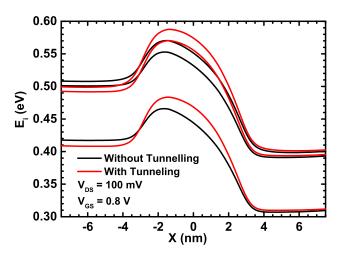


Fig. 6. Energy profile of the three first subbands with (red) and without (black) S/D tunneling.

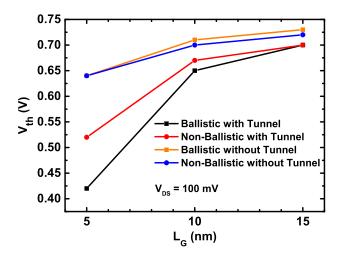


Fig. 7. V_{th} as a function of L_G with or w/o including S/D tunneling and ballistic or diffusive descriptions.

IV. CONCLUSIONS

This work presents the implementation of S/D tunneling in a MSB-EMC tool for the study of ultrascaled DGSOI devices allowing a detailed scattering description and a moderate computational cost. Our simulations show important differences in the behavior of the transistors, especially in the near-threshold operation increasing leakage current and decrasing V_{th} . The inclusion of this effect will then become mandatory as device channel length approaches to decananometer range.

V. ACKNOWLEDGMENT

The authors are grateful for the support given by the Spanish Ministry of Science and Innovation (FIS2011-26005, TEC2011-28660), CEI-BIOTIC mP-TIC-12 and Junta de Andalucía (P10-TIC-6902).

REFERENCES

- "The international Technology Roadmap For Semiconductors (ITRS)," http://www.itrs.net/, 2013.
- [2] J. W. J. Wang and M. Lundstrom, "Does source-to-drain tunneling limit the ultimate scaling of MOSFETs?" *Digest. International Electron Devices Meeting.*, pp. 707–710, 2002.
- [3] C. Sampedro, F. Gámiz, a. Godoy, R. Valín, a. García-Loureiro, and F. G. Ruiz, "Multi-Subband Monte Carlo study of device orientation effects in ultra-short channel DGSOI," *Solid-State Electronics*, vol. 54, no. 2, pp. 131–136, 2010. [Online]. Available: http://dx.doi.org/10.1016/j.sse.2009.12.007
- [4] C. Sampedro, F. Gámiz, a. Godoy, R. Valín, a. García-Loureiro, N. Rodríguez, I. M. Tienda-Luna, F. Martinez-Carricondo, and B. Biel, "Multi-Subband Ensemble Monte Carlo simulation of bulk MOSFETs for the 32 nm-node and beyond," *Solid-State Electronics*, vol. 65-66, no. 1, pp. 88–93, 2011. [Online]. Available: http://dx.doi.org/10.1016/j.sse.2011.06.036
- [5] C. Sampedro, F. Gámiz, L. Donetti, and A. Godoy, "Reaching sub-32 nm nodes: ET-FDSOI and BOX optimization," Solid-State Electronics, vol. 70, pp. 101–105, 2012. [Online]. Available: http://dx.doi.org/10.1016/j.sse.2011.11.010
- [6] C. Sampedro, F. Gámiz, and a. Godoy, "On the extension of ET-FDSOI roadmap for 22 nm node and beyond," *Solid-State Electronics*, vol. 90, pp. 23–27, 2013. [Online]. Available: http://dx.doi.org/10.1016/j.sse.2013.02.057
- [7] R. Venugopal, Z. Ren, S. Datta, M. S. Lundstrom, and D. Jovanovic, "Simulating Quantum Transport in nanoscale transistors: Real versus Mode-Space approaches," J Appl Phys., vol. 92, no. 3730, 2002.
- [8] C. Shen, L.-T. Yang, G. Samudra, and Y.-C. Yeo, "A new robust non-local algorithm for band-to-band tunneling simulation and its application to Tunnel-FET," *Solid-State Electronics*, vol. 57, no. 1, pp. 23–30, Mar. 2011. [Online]. Available: http://linkinghub.elsevier.com/ retrieve/pii/S0038110110003539
- [9] D. J. Griffiths, "Introduction to Quantum Mechanics," p. 409, 1995.
- [10] G. D. L. Sun, X. Y. Liu and R. Q. Han, "Monte Carlo Simulation of Schottky contact with direct tunneling model," *Semiconductor Science* and Technology, vol. 18, pp. 576–581, 2003.
- [11] A. Revelant, P. Palestri, P. Osgnach, and L. Selmi, "Calibrated multi-subband Monte Carlo modeling of tunnel-FETs in silicon and III-V channel materials," Solid-State Electronics, vol. 88, pp. 54–60, Oct. 2013. [Online]. Available: http://www.sciencedirect.com/science/ article/pii/S0038110113001792
- [12] Z. Huang, T. E. Feuchtwang, P. H. Cutler, and E. Kazes, "Wentzel-Kramers-Brillouin method in multidimensional tunneling," *Physical Review A*, vol. 41, no. 1, pp. 32–41, 1990.