Mechanical Simulation of Stress Engineering Solutions in Highly Strained p-type FDSOI MOSFETs for 14-nm Node and beyond

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***Abstract*— Stress engineering is a powerful tool to enhance nanoscale device performances. In this study we developed a methodology of 14nm strained pMOS FDSOI device mechanical simulation in order to carefully evaluate different stress effects on device performances. Mechanical simulation results are presented for different process solutions, such as Gate-First (GF) and Gate-Last (GL) processes but also for variation of germanium contents in source/drain and channel regions.**

Keywords—Technology Computer Aided Design (TCAD), Fully-Depleted-Silicon-On-Insulator (FDSOI), Gate-First (GF), Gate-Last (GL), Self-Aligned In-Plane Stressors (SAIPS), Shallow Trench Isolation (STI).

I. INTRODUCTION

TCAD simulation has been used to provide guidelines for strain engineering, as a major mobility booster [1, 2], in the channel for advanced nodes. Considering their strong influence on strain, geometry and processing details have been precisely accounted for, based on realistic process flow [3] and device topology. Innovative variants, such as Gate-Last (GL) process [4], or Self-Aligned In-Plane Stressors (SAIPS) where Ge content is increased below Source/Drain contacts (S/D) to further compress the channel [5], have additionally been explored.

The paper is organized as follow: in Section II, process assumptions and device geometries are detailed, especially concerning the SAIPS technique, which aims at enhancing compressive stress in the channel. In section III, we analyze the main process steps and some possible solutions to boost stress. Finally in section IV, we detail the influence of the STI and provide a global discussion on our results.

II. DEVICE UNDER STUDY

TCAD simulations were performed with Synopsys Sentaurus Process tool [6] following the fabrication process of p-type MOS transistors described in [3, 45]. We used plane strain and purely elastic materials assumptions. Two kinds of structure were studied here. The "isolated device" is defined after STI deposition where SA is the distance between gate and active edges (Fig. 1b). The "regular device" depends on the gate pitch where SD varied between 64nm and 100nm (Fig. 1a).

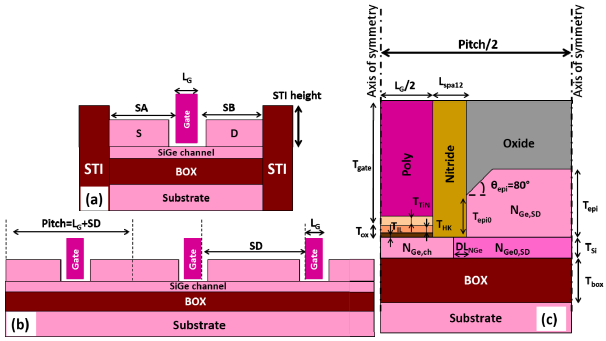

Fig. 1. (a) isolated device (delimited by STI) and (b) re (c) ice (delimited by adjacent device), where SA and SD are the act ion of epitaxy length. (c) Half structure of final device including SAIPS. Where T_{si}=6nm, θ_{epi}=80°, $T_{ox}=T_{IL}+T_{Hk}$=3.3nm, T_{TiN}=3.5nm, T_{spa12}=9nm, T_{epi}=18nm, T_{box}=20nm, $T_{gate}=T_{TiN}+T_{poly}$=25nm, T_{epi0}=10nm, DL_{NGe}=0-3-6nm, $N_{Ge,ch}$=23%, $N_{Ge,SD}$=30%, and $N_{Ge0,SD}$=23-38-53%.

Fig. 1.c shows the structure resulting from process simulation with main parameters description: Ge content in the channel is $N_{Ge,Ch}$=23% and $N_{Ge,SD}$=30% in S/D. For SAIPS, Ge concentration below S/D ($N_{Ge0,SD}$) was varied between 23% and 53% and DL_{NGe} quantifies lateral penetration distance under vertical spacers. A neutral CESL was therefore deposited after S/D epitaxy. The mechanisms for stress generation includes lattice mismatch between silicon and SiGe layers [7] as well as thermal mismatch [8] and intrinsic stress [9], which depend on deposition techniques. It is known experimentally that TiN film is deposited by PVD process during Gate-First integration for 14nm pMOS FDSOI devices, and its average intrinsic stress values can drastically vary as demonstrated by S. Baudot [9]. In this work and from experimental data, the intrinsic stress value in TiN before gate patterning was set at a value of -2.35GPa. Note that stress is partially relaxed along longitudinal direction (y-axis) by gate patterning, as previously demonstrated [10]. Table I summarizes the residual stress values in gate stack materials used in our approach based on published results.

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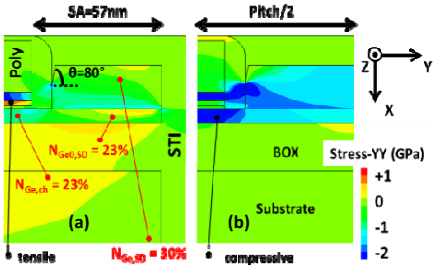

Fig. 2. GF integration: 2D cartographies of the longitudinal stress for isolated (a) and regular (b) devices, with L_G=24nm.

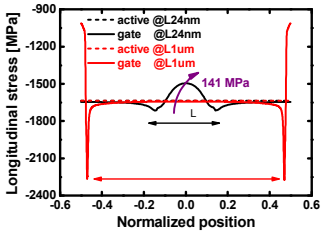

Fig. 3. Gate length impact: Longitudinal stress with GF integration after active and gate patterning where normalized position is Y-position/ gate pitch.

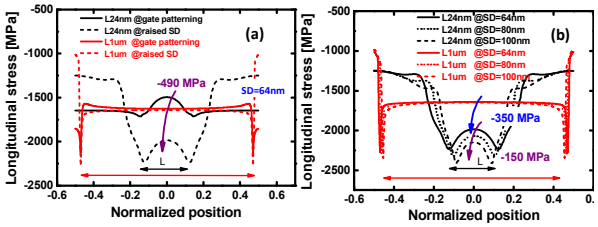

Fig. 4. Raised SD impact: Longitudinal stress with GF integration for regular structure (a) after gate patterning and after S/D growth, (b) and for SD lengths increase from 64 to 100nm (after epitaxial growth).

2D maps of the longitudinal stress (σ_L) resulting from process simulation are shown in Fig. 2 for both isolated and regular structures with shortest gate length (L_G=24nm).This figure basically shows the difference between isolated and regular structures; the STI trench strongly influences the spatial variation of the stress mapping. In the following, we first investigate the impact of different stress engineering solutions but also the STI impact on stress level into the channel. For convenience, 1D stress profiles are extracted in channel direction (y-axis), 1nm bellow channel-SiO_2 interface.

III. PROCESS TECH. TO BOOST STRESS

In present case, the impact of the main process steps is analyzed, as well as stress engineering solutions. For each process step, we show the TCAD simulations of the structures presented in section II. In order to make explanations easier, only regular devices are presented here.

TABLE I. RESIDUAL STRESS IN GATE STACK.

Gate stack	Thickness (nm)	Temperature (°C)	Residual Stress (MPa)
InterfacialOxide	1.1	800	-106
HfO_2 High-k	2.2	300	+596
PVD TiN	3.5	20	**-2350**
Poly-Si	21.5	525	0.0

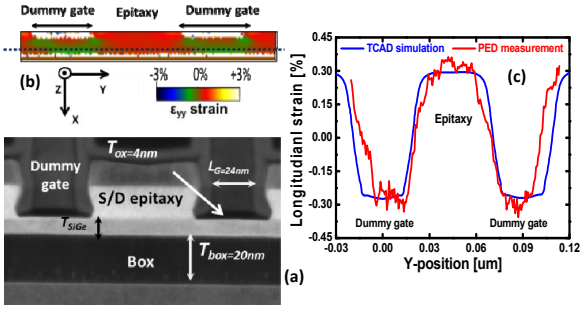

Fig. 5. GL integration: (a) TEM image of pMOSFET transistor along the channel direction, (b) corresponding strain measurement by PED and (c) comparison of the longitudinal strain profiles along Y-direction of 2D mechanical simulation and experimental PED Diffraction (i.e. εyy≈-0.3% below dummy gate).

A. *Influence of gate length and raised SiGe Source/Drain*

First, the basic processes which influence stress in the channel need to be investigated in more details. For the shortest devices, the stress variation in the channel comes basically from S/D epitaxy and from residual stress in the metal gate. No significant change in stress was obtained for the longer gate length (L_G=1µm). Fig. 3 illustrates the variation of the longitudinal stress during GF integration. For the shortest gate length (L_G=24nm), we observed a slight degradation of stress, by +141MPa, after gate patterning due to TiN relaxation. Similarly, with a given inter-gate distance SD=64nm, S/D formation enhanced longitudinal stress (by -490MPa) only for the shortest gate length values (Fig. 4.a). As expected, larger SD regions enhance longitudinal stress more, thanks to better stress transfer into the channel; as illustrated on Fig. 4.b, a stress enhancement of -150MPa was obtained when SD varied from 64nm to 100nm. Ideally, the best configuration for large compressive stress corresponds to the shortest gate lengths and longest S/D contacts.

B. *Gate Last versusGate first*

In the case of regular devices, it was possible to compare our TCAD simulation results with experimental strain maps obtained by Precession Electron Diffraction (PED) before dummy gate removal. In GL process, very close agreement was obtained (Fig. 5). As illustrated on Fig. 6, dummy gate removal gave rise to an additional enhancement of longitudinal stress by -387MPa compared to GF process. This is due to the relaxation of residual compressive stress in raised S/D regions. The enhancement can be slightly larger after metal deposition and CMP as demonstrated by Morvan *et al.* [4].

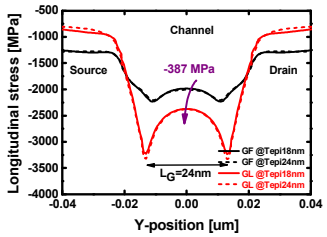

Fig. 6. Gate Last vs Gate First impact: comparison of longitudinal stress between GL (after poly-Si removal) and GF (after S/D epitaxy) for regular device.

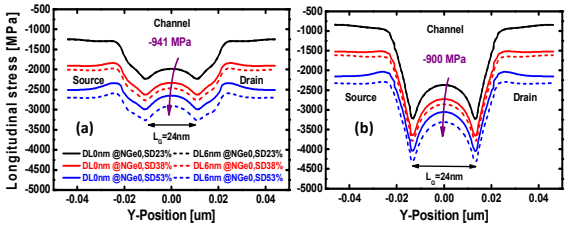

Fig. 7. SAIPS impact: comparison of longitudinal stress profiles between (a) GF (after epitaxial growth) and (b) GL (after poly-Si removal) processes for regular device.

C. *Self-Aligned In-Plane Stressors*

As previously explained in reference [5], engineering local concentration of germanium ($N_{Ge0,SD}$) between the raised S/D regions and the channel can provide larger longitudinal stress in the channel. For regular devices and during GF integration (Fig. 7.a),increasing Ge content below raised S/D ($N_{Ge0,SD}$) from 23% to 53% enhanced channel stress, by up to -670MPa. Additional improvement was obtained with larger penetration below vertical spacers, by up to –270MPa when DL_{NGe} was varied from 0nm to 6nm because of the stress increase under S/D regions close to channel. The same trends were obtained with GL integration after dummy gate removal, as shown in Fig. 7.b.

IV. SUMMARY OF STRESS ENGINEERING SOLUTIONS AND DISUSSION

A. *Isolated versus regular device: STI step height impact*

For the shortest isolated devices, stress degradation resulted from TiN stress relaxation combined with initial relaxation due to STI etching. Furthermore, the same trends were obtained for isolated and regular structures concerning the GF and GL, but also for the enhancement related to channel length or raised S/D.

In fact, the main stress difference between regular and isolated devices comes from the relaxation of the longitudinal stress in channel due to STI etching. For example in the case of GF integration, the channel stress induced by SAIPS stressor was stronger for regular (-941MPa) structures than for isolated (-498MPa) ones with $N_{Ge0,SD}$=53% and DL_{NGe}=6nm.

It is known experimentally that STI step height can vary [11]: In our simulations, it was varied from 0nm to 18nm

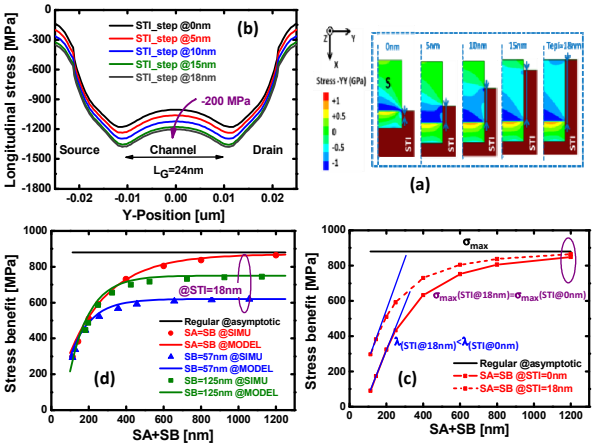

Fig. 8. STI impact: a) 2D-cartography of longitudinal stress along the S/D direction for different STI heights (from 0nm to 18nm). b) Corresponding 1D-profiles. c) Stress gain due to S/D epitaxy step for two STI step heights compared to regular device. d) Comparison of simulated (dot lines) and modeled stresses (solid lines) with fit parameter λ=220 and STI step height is equal to 18nm.

(raised S/D height = Tepi). With high STI, raised SiGe S/D mostly transferred their stress to the channel, while they were free to relax with low STI (Fig. 8.a). As a result, longitudinal stress was enhanced by -200MPa when STI was moved from top of SiGe channel to top of raised S/D (Fig. 8.b). Fig. 8.c and 8.d focus on the absolute value of stress benefit provided by raised S/D with given STI height. When active length (SA) is at least 20 times larger than epitaxial thickness (Tepi), symmetrical (SA=SB) and regular structures featured similar stress value in the channel (Fig. 8.c). Channel stress induced by raised S/D was stronger for symmetrical structures than for asymmetrical (SA≠SB) ones with same SA+SB values (Fig. 8.d).It was possible to model the stress benefit due to raised S/D for both regular and isolated devices as follows:

$$\sigma_{sym} = \sigma_{max}^{(SB=SA)}\left[1 - exp\left(-\frac{AL}{\lambda}\right)\right] \quad (1)$$

$$\sigma_{asym} = \sigma_{max}^{(SB\neq SA)}\left[1 - exp\left(-\frac{2\times AL - SB}{\lambda}\right)\right] \quad (2)$$

where σ_{sym} and σ_{asym} are the stress enhancement values taken in the middle of channel for symmetrical and asymmetrical structures respectively, AL is equal to SA+SB (active length), σ_{max} is reached for infinite active length, and 1/λ is proportional to boundary stiffness. It is known that the regular device boundaries (adjacent devices) are stiffer than isolated device boundaries (STI oxide). Therefore, 1/λ followed an appropriate behavior in this case where $1/\lambda_{STI=0nm} < 1/\lambda_{STI=18nm} < 1/\lambda_{regular}$. Fig. 8.d shows that this model correctly matched simulation results.

B. *Results summary*

All our simulation results are summarized in Table II, for different stress engineering solutions, in the case of regular and isolated p-type FDSOI MOSFETs, with active length equal to 64nm and SA=57nm respectively. The channel was initially compressive with a negative stress (≈-1.6GPa) because of the presence of 23% of Ge content ($N_{Ge,ch}$). Stress improvement is

TABLE II. SUMMARY OF STRESS ENGINEERING SOLUTIONS

Stress engineering solutions		*Stress benefits (MPa)*	
		Regular	*Isolated*
SiGe channel formation	**Ge content NGe,ch= NGe0,SD= 23%**	**-1636**	**-1636**
Active patterning	**Short (L_G=24nm)**	No impact	**607 ↘**
	Medium (L_G=100nm)	No impact	**362 ↘**
	Long (L_G=1µm)	No impact	**40 ↘**
Gate patterning *Gate length efficiency*	**Short**	**141↘(Fig. 3)**	**127↘**
	Medium	**117 ↘**	**144 ↘**
	Long	**9 ↘ (Fig. 3)**	**13 ↘**
S&D Epitaxial growth *Raised SD efficiency*	**Short**	**-490↗ (Fig. 4.a)**	**-168↗**
	Medium	**-236 ↗**	**-82 ↗**
	Long	**-14 ↗ (Fig. 4.a)**	**-9 ↗**
	Gate length↘ (from 1µm to 24nm)	-350 ↗ **(Fig. 4.b)**	-500 ↗
	Epi thickness↗ (from 18 to 24nm)	No impact **(Fig. 6)**	No impact
GL vs GF *without SAIPS*	**Short**	**-387↗ (Fig. 6)**	**-344↗**
SAIPS *(from 23 to 53% of Ge)*	**Short, GF**	**-941↗ (Fig. 7.a)**	**-498 ↗**
Total stress enhancement	**Short, GF**	**-1677 ↗**	**-275 ↗**

thus represented by a negative variation indicated by blue text and up-oriented arrow, while the stress degradation is shown by a positive variation indicated by red text and down-oriented arrow.

Table II reports the variation of compressive longitudinal stress value in the middle of the channel after each process step. During GF integration, the high level of intrinsic stress in the TiN metal gate layer degraded channel stress for shortest lengths while during GL process, the poly-Si removal step enhanced channel stress. Finally, SAIPS efficiency increased with Ge content.

V. CONCLUSION

The mechanical simulation of process steps have been correctly simulated and followed an appropriate elastic behavior. An excellent agreement in strain was achieved between experimental PED measurements and process simulations. TCAD mechanical simulations enabled us to evaluate stress behavior of p-type FDSOI MOSFET for different stress engineering techniques, and to quantify the final stress distribution. Such a study is mandatory to determine mobility booster in 14-nm node and beyond. From this study, SAIPS and Gate-Last can be considered as efficient solutions to boost stress in the channel of p-type FDSOI MOSFETs.

In the case of isolated devices, the oxide and nitride become viscous due to the temperature increase (e.g. >1000°C) during STI deposition. For this reason, in order to properly simulate its impact, a viscoelastic simulation should be performed in the future studies. But note that the stress evolution can properly be described by an elastic behavior after STI formation step.

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