Reliability aware Simulation Flow: From TCAD Calibration to Circuit Level Analysis

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Abstract— **In this paper, we present a simulation flow based on TCAD model calibration against experimental transistor measurement and doping profile reverse engineering. Further the physical astatistical variability simulations at TCAD level are also adjusted to match the statistical measurement. This is folloed up by oxide wear out reliability characterization and modelling. Finally statistical compact model libraries for fresh and aged devices are extracted from large samples of TCAD simulation results allowing the performance analysis of a 6T SRAM cell. The calibration procedure has been performed on P and NMOS transistors fabricated and characterized by IMEC, while Glasgow University performed the TCAD reverse engineering and calibration, and the statistical simulations using dedicated Gold Standard Simulations tools.**

Keywords—Compact model; aging; TCAD simulation; Statistical Variability; Statistical Reliability.

I. INTRODUCTION

With CMOS scaling, Statistical Variability (SV) -arising from the granularity of charge and discreteness of matter and from processes intrinsic limitations has become a major issue for the semi-conductor industry [1]. As a result Statistical simulation is now essential to device and circuit designers in order to properly predict products performances and yield [2]. Besides, oxide wear-out leads to interface traps activation, whose charging and discharging cause dynamic discrete fluctuations of the device performance [3]: The traping related variability adds up to the the SV resulting in Time Dependent Variability (TDV). Dedicated models and approaches capturing TDV have to be implemented at an early stage of the design flow [2].

Various approaches have been atempted in order to include TDV at circuit level, starting with equivalent circuits [4,5]. However they fail to capture the correlations between SV and aging impact. Recently a physic based approach has been developed consisting in injecting into the device characteristics the bias dependent traps impact, based on measurement of traps dynamics and electrostatic impacts [6-8]. A Verilog-A module emulate the transistor aging, following the workload [9]. However, this approach is too computationally expensive for large circuit simulations. Moreover the correlations between SV and TDV are not included in this approach contrary to TCAD based compact model extraction procedure [10].

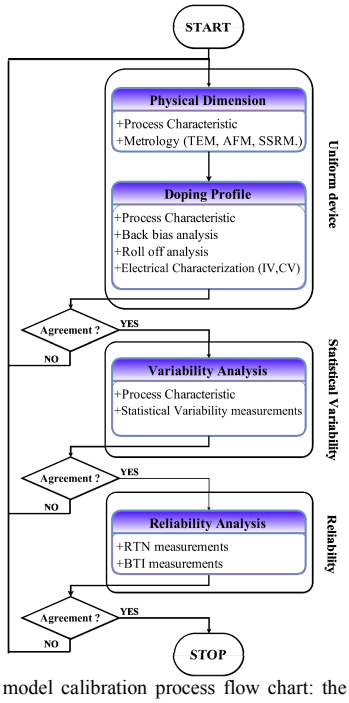

Fig. 1: TCAD model calibration process flow chart: the uniform TCAD model is extracted from several length/width ratios and used to calibrated the nominal compact model. Statistical and aging compact model are extracted from corresponding TCAD statistical simulations results.

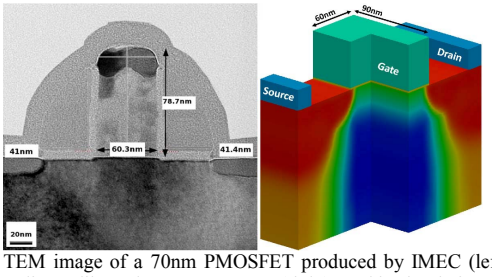

Fig. 2: TEM image of a 70nm PMOSFET produced by IMEC (left) and corresponding calibrated TCAD structure (right) used in simulation.

In this paper we present a complete methodology to capture both SV and TDV into a TCAD model, calibrated to actual statistical measurement. Based on the 'atomistic' TCAD simulations, statistical compact models are extracted at different degradation stages, allowing the monitoring of the aging circuits performances through time using statistical SPICE simulations.

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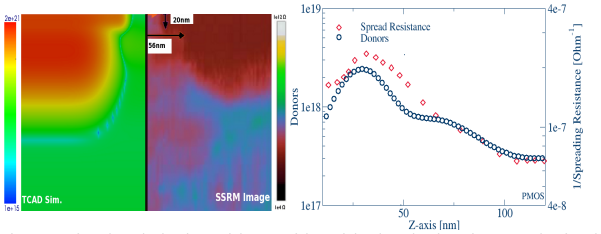

Fig. 3: Simulated doping side to side with the doping image obtained through SSR (left) and simulated doping profile in the middle of the channel, overlayed by SSR extracted results (right).

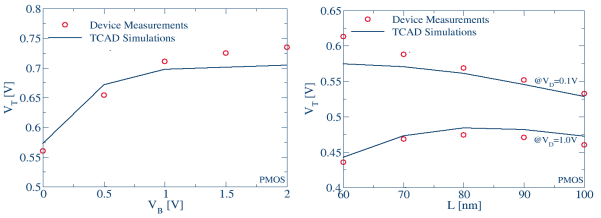

Fig. 4: Simulated and measured; V_T at different back bias: good match between simulated and implanted vertical doping profile (left) and V_T roll-off at high and low drain: relevant HALO doping level and position.

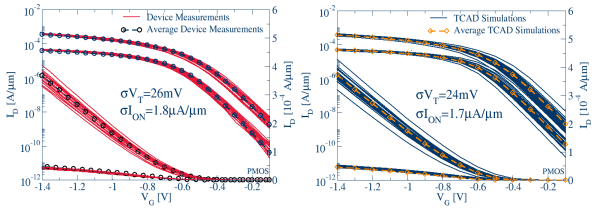

Fig. 5: I_D-V_G characteristics of device statistical measurement (left) and TCAD statistical simulations (right) for PMOS devices. TCAD simulation average matches the average measure and so are the dispersions of V_T and I_{ON} current.

II. Calibration Methodology

The investigated P and N planar MOSFETs are fabricated and characterized at IMEC. The 60x90nm long and wide channel features a $2.4x10^{18}$ cm^{-3} peak doping and $6.1x10^{20}$ cm^{-3} HALOs implantation, a 2.2nm SiON oxide layer and a polysilicon gate; this rather conservative design is preferred to obtain an all this kind work test chip; however a thick oxide enhances the traps impacts. A statistical sample of 100 microscopically different transistors has been electrically characterized to estimate the impact of statistical variability and reliability. The 4 stages of the calibration procedure are illustrated by the flowchart in Fig.1, each of them being validated by measurement as fully detailed in this paper for the PMOS device. Stages 1 and 2 are focued on the uniform device calibration, whereas stages 3 and 4 include respectively SV and TDV; in a further step compact models are extracted. In Stage 1, the device structure is extracted based on known process characteristics and metrology, so that measured dimensions from the TEM image in Fig.2 are used to define the simulation domain. In Stage 2, the doping calibration procedure starts from a doping estimate using the Spread Sheet Resistance (SSR) technique, as illustrated in Fig.3, which gives initial channel doping values and HALO positions [11]. Our in- house analytical doping implantation simulator ANADOPE [12-13] generates analytical doping profiles based on the process recipe; whereas the GSS 3D atomistic density-gradient

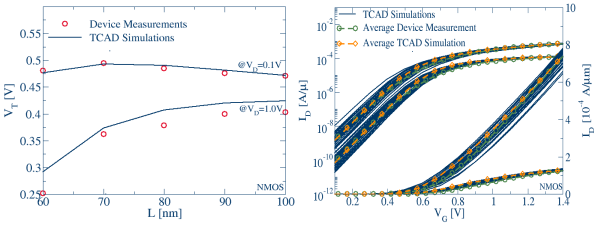

Fig. 6: Measured V_T roll-off in NMOS devices reproduced by TCAD simulations(left) and I_D-V_G characteristics of TCAD simulations whose average matches the average measure.

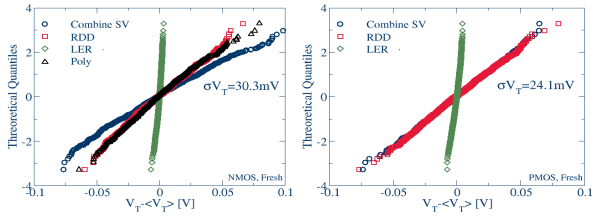

Fig. 7: Threshold voltage distributions for fresh N and PMOS devices for separated and combined variability sources.

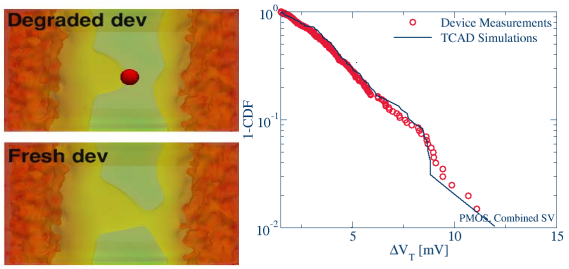

Fig. 8: Percolation path interaction with charged traps (right). Measured and Simulated RTN induced V_T shifts at the interface oxide layer (right).

corrected simulator GARAND [14] provides TCAD simulated transcharacteristics. The doping is then refined within an iterative process using successively the dependences of the threshold voltage V_T on back-bias (BB) and channel lengths (L) until a good agreement with measured values has been obtained as illustrated in Fig.4. A good agreement of threshold voltage dependence on substrate bias guarantees a realistic vertical doping profile by modulating the depth of the inversion layer. The calibration of threshold voltage dependence on channel lengths ensures the validity of the lateral doping profile by discriminating between source and drain extensions, halo implants and channel doping levels relative influences. After several iterations, a good agreement in OFF current, Subthreshold slope and DIBL is obtained and the calibration of mobility models used in Drift-Diffusion simulator is the last step of the stage 2, providing accurate simulations of the full characteristic by adjusting the ON current. Fig.5 shows the measured and simulated average device characteristics for PMOS, together with SV impacted devices The good agreement obtained for NMOS is demonstrated in Fig.6. In the third stage of the TCAD model calibration procedure 1000 atomistically different devices are simulated to gather statistics on their performances dispersion. Separated and combined impact of SV on the device performances are illustrated in Fig.7. NMOS device consist of RDD, LER and PSG as a variability sources while the latter

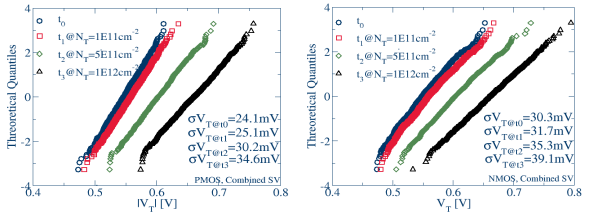

Fig. 9: Distributions of V_T at different level of BTI degradation for PMOS (left) and NMOS (right).

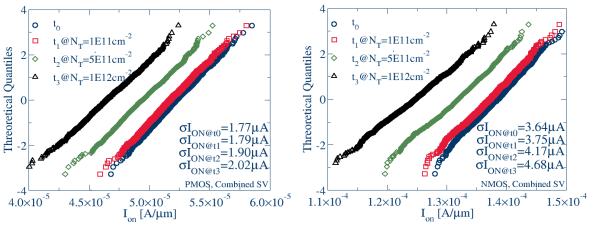

Fig. 10: Distributions of I_{ON} at different level of BTI degradation for PMOS (left) and NMOS (right).

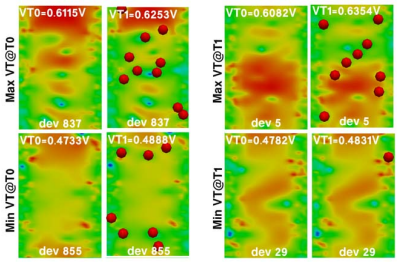

Fig. 11: Extreme device at highest and lowest threshold voltage at T_0 are replaced by other devices at T_1 after having degradation.

plays no role in PMOS SV, due to the absence of corresponding donor type interface state in the lower part bandgap, resulting in an unpinned Fermi level [15]. Note that both RDD and PSG have a major impact of statistical variability. LER, PSG dispersion parameters as well as the fine tuning of the near interface doping allow to fit the simulated SV to the measurement. Each time the doping profile is updated the previous stage needs to be repeated to ensure that the agreement between the simulations of the average device and the measures remains the same. Finally a good agreement is obtained for SV suffering devices as demonstrated in Fig.5.

III. Reliability Assessment

Based on this well calibrated TCAD model, reliability is assessed for the above transistor regarding both Random Telegraph Noise (RTN) and Bias Temperature Instabilities (BTI) steady state impacts. In RTN analysis, single charged traps are introduced at the channel oxide interface, following a uniform statistical distribution all over the channel area. SV and TDV interactions lead to drastic performances shifts when a trap occurs to block the source to drain percolation path, as illustrated in Fig.8 (left). The cumulative distribution of traps induced threshold voltage shifts ΔV_T is compared to the experimental results obtained from Time Dependent Defect Spectroscopy (TDDS) from which individual traps impact on the threshold has been extracted [6, 7, 16]. The good agreement between simulation

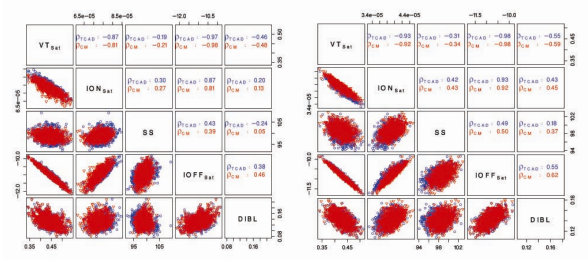

Figure 12: Distributions and correlations of TCAD and compact model figure of merit for PMOS (left) and NMOS (right)

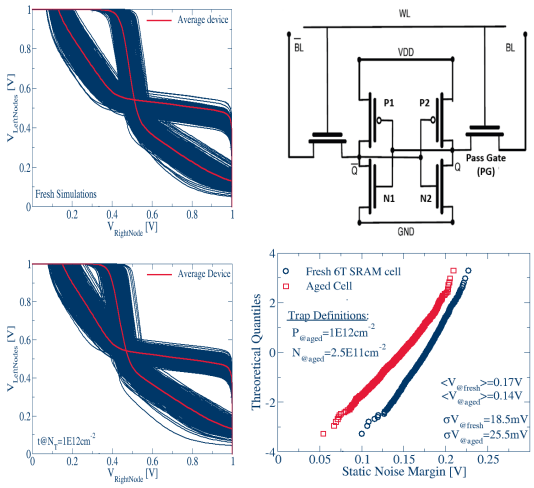

Fig. 13: Variability and reliability of a 6TSRAM cell (left) $NMOS_{Left}$ and $PMOS_{right}$ are stressed asymmetrically in the hold function of the cell; resulting SNM distribution are plotted for fresh and aged cell (bottom right).

and measurements demonstrates the correctness of the calibration process and the capabilities of the simulator in reproducing the measured variability and reliability.

In the BTI steady state analysis, the aging of the device is performed by introducing an increasing average trap density from 10^{11} to 10^{12} cm^{-2} following the experimental result from [17]. It is worth noting that a poissonian distribution of traps number has been used based on the above averages. The dispersion of the threshold voltage increases from 24mV for fresh PMOS to 35mV and from 30mV to 39mV for the NMOS, while the averages increase from 0.54V to 0.65V for PMOS and from 0.55V up to 0.66V for NMOS. As can be seen in Fig.9. The dispersion of ON current increases from 1.8µA to 2µA for PMOS and from 3.6µA to 4.7µA for the NMOS as illustrated in Fig.10. We have further analyzed the extreme cases for PMOS devices in Fig.11 (left) in which the current densities are mapped for the devices featuring the highest and lowest fresh V_T, to be compared with their current density maps with a 10^{11} cm^{-2} trap density. On the contrary, in Fig.11 (right) the extreme V_T are selected from the distribution with interface traps. It is important to mention that the extreme devices from the fresh distribution are no longer the extreme devices after the charge of the traps: whereas the former depends only on the dopants number and positions, the latter depends also on the interactions between SV and TDV as well as on the number of charged traps.

IV. CIRCUIT SIMULATION

The compact model parameter extraction is performed using GSS Mystic [14] and starts with the extraction of a nominal compact model for N and PMOSFETs from the calibrated uniform TCAD including drain, gate and backbias dependences. 1000 atomistic devices TCAD simulation results are used in the following step, each of them being separately extracted in order to preserve the correlation between their parameters. This is demonstrated in Fig.12, which shows a comparison of the device parameters distributions for TCAD and compact models simulations of fresh N and P devices. Once the compact model parameter distributions are obtained, the statistical sample of statistical compact models can be extended to reach higher sigma levels, allowing proper SRAM reliability assessments [18]. This step is repeated for different level of degradations and compact models for intermediate aging levels can be obtained in a similar way than [18].

A 6T SRAM using 1:1:1 configuration in a pass gate, pull up and pull down transistor is used as a test-bench; Fig.13 shows the fresh and degraded Static Noise Margin (SNM) distributions simulated as in [18, 19] in the hold phase of the cell, where the left NMOS and right PMOS are turned in and stressed, so that both recoverable and permanent part of the degradation are considered. For a realistic aging degradation, we assumed that degradation of NMOS is quarter than PMOS as measured in [20]. As a result, the butterfly curves in Fig.13 (left) shows a closing of the eye, reflected in the average SNM reduction and an increase in its dispersion. More degradation scenario will be presented in [21], including dynamic write margins simulations.

V. CONCLUSION

This paper presents a comprehensive methodology inclusing TCAD calibration of contemporaty CMOS transistors in presence of statistical variability and reliability and comprehensive reliability awere compact model extraction and generation technology aiming to predict a 6T-SRAM performance in circuit simulation. Each calibration stage, including transistor geometry, doping profile, statistical variability and reliability, are validated against experiment. The interaction between traps and percolation paths results in a reordering of V_T distributions, depending on number and positions of traps, relative to the intial doping configuration. The compact model extraction consists of 3 stages including uniform model extraction, statistical model extraction and finally reliability model extraction. These models are extracted from large statistical samples at different level of degradation while preserving the correlation between statistical parameter and figure of merit of the transistor. Finally, we performed an SNM degradation analysis using 6T-SRAM circuits in statistical SPICE simulation at arbitrary stress time.

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