Origin of Mobility Degeneration at High Gate Bias in Organic Thin Film Transistors Based on Carriers' Freeze to Surface Charges

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Abstract—**Traditionally, mobility of the bulk organic semiconductor materials was thought to increase with the increase of carriers' concentration. However, the experimental results show that the field effect mobility in OTFTs degenerate with the increasing gate voltage at high gate bias. Recently, even the source/drain current was found to decrease at high gate voltage bias. To interpret this phenomenon, we proposed a model based on carriers' freeze to surface charges. According to this model, the charge carriers' concentration in semiconductor layer as well as surface charges, would increase with the increase of the gate voltage, and combination of them results in the mobility firstly to increase then to decrease with the increasing the gate voltage.**

Keywords—Organic Thin Film Transistors (OTFTs); Mobility Degeneration; Surface Charges; Carriers' Freeze

I. Introduction

Organic thin film transistors (OTFTs) show great potential in application of flexible, transparent, and large area electronics, whereas lots of abnormal behaviors were found and needed a further study to unveil its device physics. Carrier concentration plays an important role for the mobility in organic semiconductor materials, and in a traditional view, higher carrier concentration would result in higher mobility, which has been experimental observed and theoretical explained in both OTFTs and organic light-emitting diodes (OLED) [1,2]. Charge carrier mobility is the result of carrier hopping from Fermi level to transport energy, with the increasing of carrier concentration, which is corresponding to the increasing of Fermi level, the energy gap between Fermi level and transport energy will decrease, this will lead to the mobility increasing. For OTFTs, with this view, it is obvious to conclude that higher gate voltage, which cause a higher carrier concentration in the channel, would result in a higher field effect mobility. However, several experimental results show abnormity from this perspective that the field effect mobility in OTFTs degenerate with the increasing gate voltage at high gate bias [3,4]. Recently, it was reported that even the source/drain current was found to decrease at high gate voltage bias in electrolyte-gated OTFTs [5]. Actually, it's a common phenomenon [6], which is easier for observation when using high-k dielectric layer or organic semiconductor layer with lower carrier concentration.

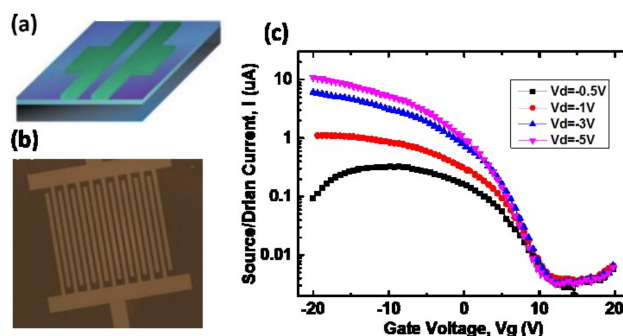

Fig. 1 (a) Schematic diagram of the structure and (b) optical image of OTFTs. (c) Transfer characteristics of OTFTs under different source/drain voltages. Inset: extracted field effect mobility as the function of gate voltage.

In this letter, a mechanism based on carriers' freeze to surface charges was proposed to uncover the physics behind those phenomenon. There were a large amount of surface states in the interface of dielectric layer and organic semiconductor layer, which would trap a certain amount of charges related to the gate voltage. And those trapped charges in surface states would freeze some of the charge carriers in channel, thus affect the performance of the OTFTs. Including this mechanism within percolation theory in OTFTs, we would found that the charge carriers' concentration in semiconductor layer as well as surface charges, would increase as the gate voltage increases, and combination of them results in the mobility firstly to increase then to decrease with the increasing the gate voltage.

II. Experimental Details

The Figure 1a illustrated the structure of OTFTs. The heavily doped, P-type Si substrate with a thermally oxidized 100 nm-thick SiO2 was used as the gate dielectric. the fabrication process of the device, which was accomplished by the following steps: i) The wafer was successively ultrasonically washed by acetone, alcohol, and deionized water for about 10 minutes at each step; ii) About 1.8 um thick photo resist was cast on the SiO2 surface and was patterned by photolithography. iii) The PPy film was in-situ polymerized in the patterned area [7]. iv) OTS was modified at 120℃ for 2 hours in a vacuum oven. Finally, pentacene with a thickness of 50nm was deposited onto the substrate. In addition,

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the channel width and length of the OTFTs invested here are 500um and 10um respectively.

As shown in Fig. 1c, in very small source/drain voltage bias (V_D), source/drain current would decrease with the increase of gate inverse voltage, at high voltage bias. Similar result can be seen from Yu Xia etc. Additionally, in our experimental data, we can find that, in high V_D situation, this effect of current degeneration is suppressed. As for field effect mobility, it becomes tricky here, since the traditional method for mobility extraction, $\mu = \partial I/\partial V_g$, which would result negative field effect mobility, is no longer suitable. Extraction of the field effect mobility in terms of transconductance $\mu = (C_i V_D L/W) I/|V_g - V_t|$, seems more suitable in this situation. The extracted mobility as the function of gate voltage were given in the inset of Fig. 1c, where one can see that when current normally increase with the gate voltage (V_D=-1V), abnormal field effect mobility degeneration may occur. That gives an explanation for that mobility degeneration in gate high voltage bias are more commonly reported than source/drain current degeneration.

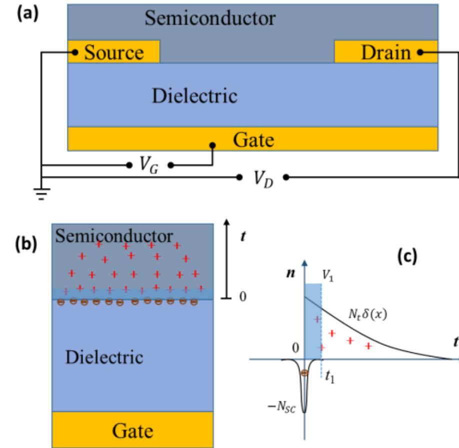

Fig. 2 (a) Schematic diagram of the structure of OTFTs and measurement setup. (b) Schematic diagram of the surface charge and distribution of the charge carriers' distribution in organic layer. (c) Schematic diagram of the surface charge freeze the carriers in organic layer near the interface (blue shadow area).

III. Modeling

The details of the model were illustrated in Fig. 2. Fig. 2a shows the typical structure and operation bias setup for the OTFT. With a voltage bias V_G applied in the gate electrode, a charge carriers' distribution was built in the organic semiconductor layer, as shown in Fig. 2b and 2c, which formed a channel near the interface of the organic semiconductor and dielectric layers. The distribution of carrier in organic layer can be described as,

$$n(x) = N_t \delta(x) = N_t \delta_0 exp\left(\frac{eV(x)}{k_B T_0}\right), \quad (1)$$

where, N_t is the total number of states per unit volume, $\delta(x)$ is carrier occupation at position x, e is element charge, $V(x)$ is potential distribution, k_B is Boltzmann's constant, T_0 is a parameter that indicates the width of the exponential distribution of states (DOS) per unit volume, and δ_0 is the carrier occupation far from the interface of semiconductor and dielectric, where $V(x) = 0$.

In the meantime, the surface states in the interface of the organic semiconductor and dielectric layers would also be occupied. For simplicity, we first assume the surface states are in the same energy level with doubly degeneration (other complex types density of surface states would be discussed in III. 2). Then, the surface charge concentration would be,

$$N_{sc} \approx 2N_s exp\left(\frac{eV(0)}{k_B T}\right), \quad (2)$$

where N_s is the total number of surface states, and $V(0)$ is the surface potential at the semiconductor-dielectric interface with $x = 0$. The potential distribution $V(x)$ and carrier occupation $\delta(x)$ can be obtained by solving Poisson equation. Thus, for accumulation layer, where $\delta(x) \propto \delta_0$, the relationship between electric field $\mathrm{F(x)} = -\mathrm{dV(x)/dx}$ and $\delta(x)$ should be,

$$F^2(x) = 2k_B T_0 N_t \delta(x)/\varepsilon_s, \quad (3)$$

where ε_s is the dielectric constant of organic semiconductor layers. The interface electric field $F(0)$ is related to gate voltage V_G and insulator capacitance per unit area C_i given by Gauss' law,

$$F(0) = C_i(V_G - V_{ON})/\varepsilon_s = \sqrt{2k_B T_0 N_t \delta(0)/\varepsilon_s}, \quad (4)$$

where V_{ON} is on voltage of the OTFTs.

Due to the Coulomb interaction, we assume that the surface charges' concentration would freeze equal amount of charge carriers in the organic layers near the interface. In other word, within a specific thickness t_1 of the organic semiconductor layer, as shown in Fig. 2b and 2c, would not contribute the source/drain current of the TFTs. The thickness t_1 can be given by,

$$N_{sc} \approx N_t \int_0^{t_1} \delta(x)dx = N_t \int_0^{t_1} \delta_0 \exp\left(\frac{eV(x)}{k_B T_0}\right) dx$$
$$= \frac{1}{e}\sqrt{2k_B T_0 N_t \delta(0)\varepsilon_s}[\exp\left(\frac{eV(0)}{2k_B T_0}\right) - \exp\left(\frac{eV_1}{2k_B T_0}\right)], \quad (5)$$

where V_1 is the potential at the position of x=t_1.

According to the percolation theory, the conductivity of organic semiconductor can be represented as a function of the occupation δ [8,9],

$$\sigma(\delta) = \sigma_0\left(\frac{\pi N_t \delta (T_0/T)^3}{(2\alpha)^3 B_C \Gamma(1-T/T_0)\Gamma(1+T/T_0)}\right)^{T_0/T}, \quad (6)$$

where σ_0 is an unknown prefactor, α is an effective overlap parameter of tunneling process between localized states, and B_C is a critical number in percolation theory approximate to 2.8 [10]. Since only the carriers out of the freeze would contribute to the source/drain current, the final source drain current would be

$$I = \frac{WV_D}{L}\int_{t_1}^{t} \sigma(\delta(x))dx, \quad (7)$$

where W is the channel width of OTFT, L is the channel length of OTFT, V_D is the source/drain voltage applied to the OTFT, and t is the thickness of organic semiconductor layer.

Combine Equation 1-5 to Equation 6 and 7, the final expression for source/drain current would be,

$$I = \frac{WV_D}{L}\sigma_0\left(\frac{\pi (T_0/T)^3}{(2\alpha)^3 B_C \Gamma(1-T/T_0)\Gamma(1+T/T_0)}\right)^{T_0/T} \frac{\sqrt{2k_B T_0 \varepsilon_S}}{e(2T_0/T-1)}$$

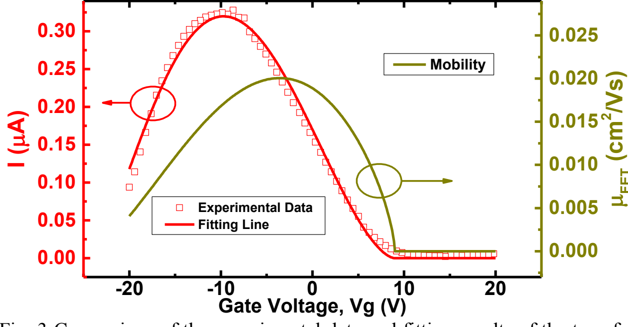

Fig. 3 Comparison of the experimental data and fitting results of the transfer characteristic of the OTFTs, as well as the mobility as the function of gate voltage for the OTFTs.

$$\times\left[\frac{C_iV_G}{\sqrt{2k_BT_0\varepsilon_s}}-\frac{2N_se}{\sqrt{2k_BT_0\varepsilon_s}}\left[\frac{(C_iV_G)^2}{2k_BT_0N_t\delta_0\varepsilon_s}\right]^{T_0/T}\right]^{2T_0/T-1}, \quad (8)$$

which can be rewrite as

$$I=a[b(V_G-V_{ON})-c(V_G-V_{ON})^{2T_0/T}]^{2T_0/T-1}, \quad (9)$$

with the parameters' value of

$$\begin{cases} a=\frac{WV_D}{L}\sigma_0\left(\frac{\pi(T_0/T)^3}{(2\alpha)^3B_c\Gamma(1-T/T_0)\Gamma(1+T/T_0)}\right)^{T_0/T}\frac{\sqrt{2k_BT_0\varepsilon_s}}{e(2T_0/T-1)} & (10)\\ b=\frac{C_i}{\sqrt{2k_BT_0\varepsilon_s}} & (11)\\ c=\frac{2N_se}{\sqrt{2k_BT_0\varepsilon_s}}\left[\frac{C_i^2}{2k_BT_0N_t\delta_0\varepsilon_s}\right]^{T_0/T} & (12)\end{cases}$$

When V_D V_G is relatively small, the field-effect mobility can be obtain by

$$\mu_{FE}=\frac{L}{C_iWV_D}\frac{I}{V_D-V_{TH}}, \quad (13)$$

where V_{TH} is the thresh voltage of the OTFT.

IV. Results and Disscussion

For a typical OTFT whose structure shown in Fig. 1a, with heavily doped silicon as gate, 100nm thermal oxidized silicon as dielectric layer, polypyrrole (PPy) as source/drain electrode, pentacene as the semiconductor, the presented model can well fit its transfer characteristics, in which the source drain current shows degeneration with the increase of the negative gate voltage, as shown in Fig. 3, with the parameters' value of T_0=400K, $\sigma_0=1\times10^{11}$ S/m , α^{-1} =0.23nm, N_t=1.8 $\times$ 10^{17}/cm^3, N_S=4 $\times$ 10^{16}/cm^2, δ_0=1 $\times$ 10^{-5}, V_{ON}=9V, and $\varepsilon_s=5\varepsilon_0$, where ε_0 is vacuum permittivity, in Equation 9.

The field effect mobility of the OTFT was also demonstrated in Fig. 3. One can see that the mobility degeneration would be prior to the degeneration of source/drain current, as the gate voltage increasing. This agrees well with previous discussion in this article (Fig. 1c and its inset) and result of ref. It is believed as the reason that the mobility degeneration was more commonly mentioned in literatures.

Calculated the number of carriers in organic layers and the number of surface charges as the function of gate voltage, with the parameters' value same as the fitting line in Fig. 3, as shown in Fig. 4, we can see that, the number of carriers in organic layers shows linear relationship with the gate voltage, which is response for the increase of the source/drain current in low gate voltage. However, as the gate voltage increase, the number of

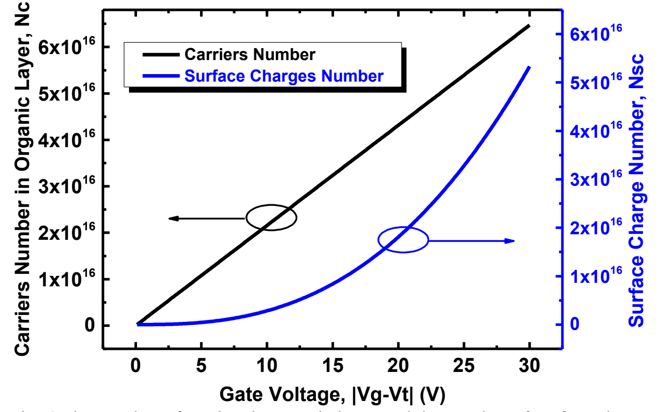

Fig. 4 The number of carriers in organic layer and the number of surface charge as the function of gate voltage.

the surface charges, which increases faster than the carriers', would freeze a larger amount of carriers' in the channel. The numbers remaining movable carriers would decrease as the increase of the gate voltage, which causes the decrease of the source/drain current and field effect mobility of the OTFT in the high gate voltage region.

It is clear that the number of surface states, N_S, is a key factor for the current degeneration in high gate voltage bias. For large N_S, source/drain current would reduce with the increase of negative gate voltage, in high gate voltage region, however for low N_S situation (=1 $\times$ 10^{12}/cm^3), this effect the transfer current curve would more likely be a conventional type, continuing increase with the increase of negative gate voltage. Thus, reducing surface states in the dielectric-semiconductor interface, would a key strategy to improve the performance of OTFTs.

For a more realistic situation, the surface states can be describe as an exponential DOS,

$$g_s(E)=\frac{N_s}{k_BT_s}\exp\left(\frac{E}{k_BT_s}\right) \qquad -\infty<E\le0, \quad (14)$$

where T_S is a parameter that indicates the width of the exponential distribution. Then the surface charge concentration in Equation 2, should be rewrite as,

$$N_{SC}\approx\int_{-\infty}^{0}\frac{g_s(E)}{1+\exp\left(\frac{E-(eV-E_{F0})}{k_BT}\right)}dE$$
$$=N_s\exp\left(\frac{eV(0)-E_{F0}}{k_BT_s}\right)\Gamma(1-T/T_s)\Gamma(1+T/T_s) \quad (15)$$

With this equation substituting the Equation 2, the final current would be

$$I=\alpha[\beta V_G-\gamma V_G{}^{2T_0/T_s}]^{2T_0/T-1} \quad (16)$$

It is clear that, for small T_S, $2T_0/T_S>1$, the source/drain current would eventually decrease with the increase of gate voltage at high gate bias. For large T_S, a broader distribution of surface states, if $2T_0/T_S<1$, those effects would not emerge. So that the degeneration of source/drain current in high gate voltage bias, is more likely to occur, when the total surface states N_S is larger and the distribution of it is narrower.

From the experimental results, we would find that for large source/drain voltage, V_D, the effects of current degeneration in high gate voltage situation, would be suppressed. To interrupt this phenomenon, electric-field dependent percolation theory

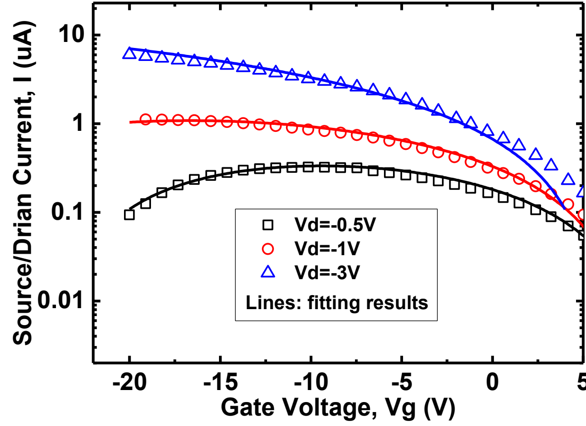

Fig. 5 Comparison between experimental and calculation results of the gate voltage dependent source/drain current of OTFTs at different source/drain voltages.

should be applied in high source/drain voltage situation. Due to the fact that electrostatic potential will be affected by the strong source/drain voltage, and therefore the density of states, Equation 1 should be rewrite as

$$n'(x) = N_t\delta'(x) = N_t\delta_0 exp\left(\frac{eV(x)}{k_BT_0}\right) exp\left(\frac{eFr}{k_BT_0}\right), \quad (17)$$

where r is hopping distance, and the final source/drain current would be

$$I' = a[bV_G - c'V_G{}^{2T_0/T}]^{2T_0/T-1} \quad (18)$$

with the parameters' value of

$$c' = exp\left(\frac{-eFr}{k_BT_0}\right)\frac{2N_se}{\sqrt{2k_BT_0\varepsilon_s}}[\frac{C_i{}^2}{2k_BT_0N_t\delta_0\varepsilon_s}]^{T_0/T}. \quad (19)$$

Since the $T_{eff} > T$, compared Equation 18-19 with Equation 9-10, we could conclude that with larger source/drain voltage, the second term in Equation 18 would be less effective to the total current, and the source/drain current is less likely to degeneration in high gate voltage bias. Fig. 5 shows the comparison between experimental data and calculation results (based on Equation 18) of the gate voltage dependent source/drain current of OTFTs for different source/drain voltages.

V. Conclusions

In conclusion, the physical mechanism behind the field effect mobility degeneration at high gate bias in OTFTs was proposed based on the assumption that carriers would freeze to the surface charge in the interface of dielectric and semiconductor layer. Based on this mechanism, a percolation model of the I-V characteristic of OTFTs was derived. It agrees well with the experimental data. The model indicates that high surface density of states (DOS) is the origin of the mobility and source/drain current degeneration at high gate voltage of OTFTs, and must be reduced to get an OTFT with higher performance.

VI. Acknowledgements

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