Advanced Methodology for Fast 3-D TCAD Electrothermal Simulation of Power HEMTs Including Package

Aleš Chvála, Daniel Donoval, Marián Molnár, Juraj Marek, and Patrik Príbytný
Institute of Electronics and Photonics,
Slovak University of Technology in Bratislava, Slovakia
812 19 Bratislava, Slovakia
E-mail: ales.chvala@stuba.sk

***Abstract*—This paper introduces an advanced methodology for fast 3-D TCAD electrothermal simulation for the analysis of complex power devices including package and cooling assemblies. The proposed methodology is based on coupling a 3-D finite element method (FEM) thermal model of the package, 3-D FEM electrical model of the metallization layers and circuit electrical model using a mixed-mode setup in Synopsys TCAD Sentaurus environment. This approach combines the speed and accuracy, and couples temperature and current density nonuniformity in structure and metallization layers. A power InAlN/GaN high-electron mobility transistor (HEMT) is used to perform validation of the designed electrothermal simulation. The simulation results are compared with measured data and 2/3-D FEM simulations. The low time consuming simulation approach helps to optimize more complex power structures and systems including all main fabrication parameters from semiconductor layers, metallization, package, and up to cooling assemblies.**

Keywords—3-D electrothermal simulation, power high-electron mobility transistor (HEMT), TCAD modeling

I. Introduction

Recent progress in GaN-based high-electron mobility transistors (HEMTs) has confirmed them to be the leading transistor technology for future high-power devices at high-frequency operation utilizing their excellent electronic properties, high electron saturation velocity, and high breakdown voltage [1]–[3]. To extract and exploit effectively the favorable GaN material properties, however, there are still a lot of areas to be investigated. Among them the most important is to develop new GaN specific processes, structure design, and characterization techniques. Multifinger devices with compact layout are required for high-power operation, however, self-heating induced thermal crosstalk between individual gate fingers becomes serious, which degrades device performance or results in irreversible damage [4]. Therefore, thermal management is crucially important to the viability of power HEMTs and the fact that many properties of power semiconductor devices are strongly temperature dependent [4]–[18]. However, electrothermal simulations based on the finite element method (FEM) are very time consuming and require powerful hardware particularly for complicated 3-D structures. The separately solved thermal equation in FEM thermal model of package and electrical equations in equivalent circuit device model by two different software is wide applied for power systems and integrated circuits to reduce the simulation time [6]–[10]. However, the complex solution requires a proper synchronization and data transfer.

Our designed electrothermal simulation is based on direct coupling between FEM thermal and circuit electrical simulation using mixed-mode setup [11]–[13] supported in Synopsys TCAD Sentaurus environment [14]. The mixed-mode setup allows direct interconnection of a 3-D FEM thermal model of the whole system (semiconductor layers, package, printed circuit board (PCB) up to cooling assemblies), 3-D FEM electrical model of the metallization layers and an equivalent electrical temperature dependent circuit model of the HEMT. The electrothermal simulation in mixed-mode setup runs simultaneously and no synchronization and data transfers between two different tools are required. This approach couples temperature nonuniformity of the structure and nonuniformity caused by parasitic resistance of the metallization to the active device electrothermal behavior. The advantages of the proposed method are in the high speed of simulation and simplicity of implementation for complete, high complexity structure analysis.

In this paper, we present our simulation methodology validated by InAlN/GaN power HEMT. Simulation results are compared with the measured data, and the results of standard 2-D and 3-D FEM electrothermal simulations. The features and limitations of the methods are analyzed and presented.

II. Structure Description and 2/3-D FEM Simulation

The structure under investigation is the power InAlN/GaN HEMT packaged in DPAK 2 and placed on the PCB including a cooler (Fig. 1). The device consists of a 300 nm thick AlN nucleation layer grown on a 6H-SiC substrate followed by a 2.5 µm GaN buffer layer with a 1 nm AlN spacer layer and a 7 nm $In_{0.14}Al_{0.86}N$ barrier layer on top [15]. The drain and source contacts are prepared by evaporation of a Ti/Al/Ni/Au metal stack with subsequent rapid thermal annealing, while the

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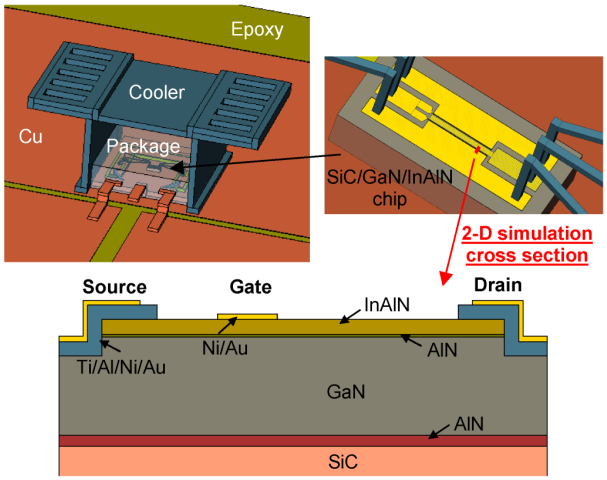

Fig. 1. 2-D cross section and 3-D view of the structure and metallization of the HEMT with a fork-shaped gate electrode.

gate contact is formed using Ni/Au metallization. The metallization layout has a fork-shaped gate electrode.

The 2-D and 3-D models of the HEMT for electrothermal FEM simulations are created in Sentaurus Device Editor (SDE) [16] according to the structure geometry. A thermodynamic transport model implemented in Sentaurus Device is used for simulation of the HEMT characteristics. The simulated characteristics have been used for analysis of the internal behavior and extraction of the equivalent electrical circuit model parameters. Both are important for build up the proposed mixed-mode electrothermal simulation. Location of the spot, where heat generation occurs, determines the placement of the heat sources in the thermal model. While the equivalent electrical circuit model replaces the electrical behavior of the FEM model.

III. 3-D Mixed-Mode Electrothermal Simulation

Our proposed methodology for the fast 3-D electrothermal simulation combines the thermal model of the whole system, the temperature dependent equivalent electrical circuit model of the structure and the electrical model of the metallization layers using the mixed-mode setup. This setup is built to allow heat flux calculated in the circuit model to the thermal contacts of the 3-D thermal model via thermal nodes. The current density distribution and the voltage drop on parasitic resistances are solved in 3-D electrical model of the metallization. The short time of simulation is assured by solving only the heat equation in the 3-D FEM model of the package and Poisson equation in the metallization layer, and fast solving of the equivalent circuit electrical model.

The HEMT equivalent circuit model is a behavioral compact model [13], [17], with included Schottky gate current sources (D_{GS} and D_{GD}), drain–source current source I_{DS}, and resistors R_{Sa} and R_{Da} which represent the resistivity of the drain/source access regions. All components are temperature dependent and implemented to Sentaurus Device using Compact Model Interface (CMI) which provides

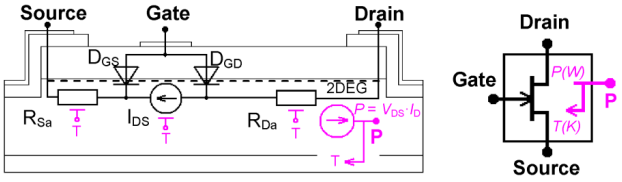

Fig. 2. Equivalent circuit model of the HEMT structure consisting of resistors and current sources representing parasitic resistance of 2-D electron gas (2DEG), Schottky gate current, and drain–source current. The components are temperature dependent and driven by the temperature on the P thermal node.

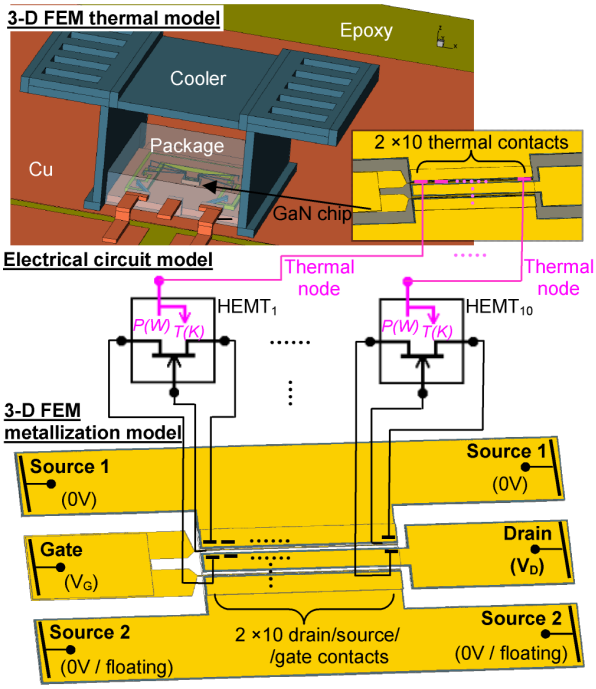

Fig. 3. Circuit diagram of the electrothermal mixed-mode simulation. Equivalent HEMT circuit model is connected to 3-D thermal model by the thermal nodes. Heat flux and temperature exchange is provided via thermal nodes. The current density distribution and the voltage drop on parasitic resistances are solved in 3-D electrical model of the metallization.

implementation of user-defined compact models in C++ and they are linked to Sentaurus Device at runtime [16]. The thermal pin of the HEMT circuit model, which represents the heat source of dissipated power, is connected to the thermal contacts of the 3-D FEM thermal model by the thermal node (Fig. 3). The thermal contacts are placed under the gate electrode edge at the drain side, where the heat generation occurs during the ON-state operation [13]. Heat generation and heat transfer are calculated in the FEM model. The temperature on the thermal nodes (which is equal to the temperature on the thermal contacts of the thermal model) drives the nonlinear temperature dependent electrical parameters of the HEMT circuit model.

In this work, the analyzed structure is split into ten segments along the gate electrode width for the simulation of

an inhomogeneity in the third dimension. Each segment represents one circuit model connected with corresponding thermal contacts. The HEMT segments are electrically connected to the 3-D FEM electrical model of the metallization which calculates the current density distribution and the voltage drop on parasitic resistances of the drain, source, and gate metallization.

IV. Simulation Results and Validation

The proposed methodology of electrothermal simulation has been used to analyze the properties of a power GaN HEMT. Fig. 4 shows a comparison of the measured and simulated output characteristics for two different measurement setups. The first setup connects only Source 1 to the ground and only one gate finger is active. The second setup connects both sources to the ground and both gate fingers are active. The temperature interaction between the gate fingers for the second setup shows a drop of the output characteristics, which is caused by a higher structure temperature compared to the first setup (Fig. 5 (Cross section A)). Moreover, there is an additional voltage drop due to the metal resistance caused by doubled current flowing through drain metallization layer (Fig. 6). Its main impact is in the linear region of the output characteristics. The proposed 3-D electrothermal simulation splits the structure along the gate into several parts, which allows analysis of the inhomogeneous distribution of temperature and of the electrical properties. The inhomogeneous distributions of temperature and current along the gate electrode are shown in Fig. 5 (Cross section B). The lower temperature and higher current density at the HEMT edge segments are caused by more effective cooling of the structure edges compared with the central segment.

Table I compares the simulation results of the proposed methodology with the standard 2-D and 3-D FEM electrothermal simulations. In the case of the 2-D simulation and assumption that the current is proportional to the total gate width, there is no difference between employing only one and both sources. Moreover, the 2-D device simulation considers homogeneous distributions of all parameters in the third dimension. The 3-D heat flow and inhomogeneous behavior along the whole structure are neglected. As for other

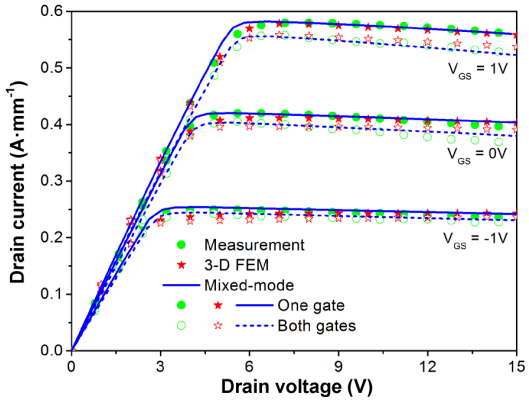

Fig. 4. Comparison of measured and simulated output characteristics for one and both gate fingers active.

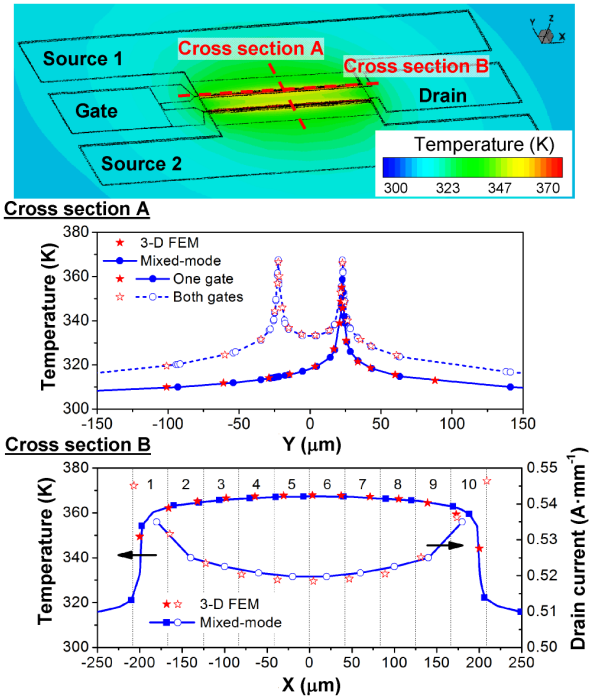

Fig. 5. Temperature distribution of the HEMT for $V_{DS} = 15$ V and $V_{GS} = 1$ V (top). (Cross section A) Comparison of the temperatures across the gate electrodes for one and both gate fingers active. (Cross section B) Temperature and current distributions inside the HEMT structure along the gate electrode.

heterostructure transistors, the designed mesh must be sufficiently tight around heterointerfaces, especially where large variations in carrier concentration are observed within short distances, for example in the 2DEG [18]. The dense mesh and large dimensions of the HEMT make a full 3-D TCAD approach very time consuming. The reduction of the mesh causes low accuracy and convergence problem. The advantages of our proposed method are in the high speed of simulation for complete, high complexity structure analysis.

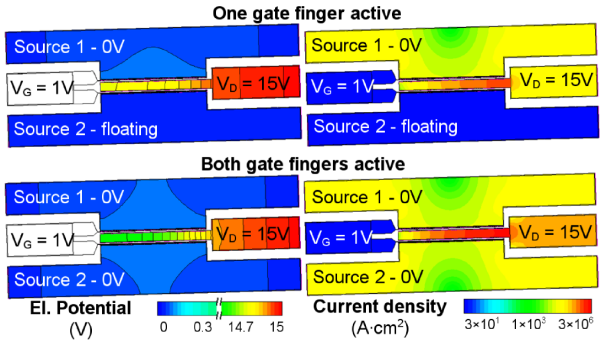

Fig. 6. Electrostatic potential and current density distribution in the metallization for one and both gate fingers active. For both gate fingers active is an additional voltage drop due to the metal resistance caused by doubled current flowing through drain metallization layer.

TABLE I. COMPARISON OF SIMULATION RESULTS OF THE PROPOSED METHODOLOGY WITH THE STANDARD 2-D AND 3-D FEM ELECTROTHERMAL SIMULATIONS

Simulation	Mesh elements	Simulation time	Limitations/Advantages
2-D FEM	16 500	5 min	No 3-D thermal flow No inhomogeneity in third dimension
3-D FEM	500 000	5 hours	Slow Reduced mesh –› low accuracy and convergence problem
Mixed-mode	Package: 140 000 Metallization: 4 500 Circuit: 20 HEMTs	2 min	Fast Allows 3-D heat flux in whole system Calculates current distribution in metallization

The analysis of thermal and electrical behavior can help during the design and optimization of parameters and geometry from semiconductor layers, metallization, package, and up to cooling assemblies.

V. CONCLUSION

Fast 3-D electrothermal simulation based on the direct coupling FEM thermal and circuit electrical simulation in the mixed-mode Sentaurus device setup was designed and verified. The designed methodology is developed for Synopsys TCAD Sentaurus environment and allows decreasing of the simulation time for complicated 3-D structures. The power InAlN/GaN HEMT was used to perform validation of the proposed electrothermal simulation. The simulation approach helps to assess the device properties by means of evaluating both temperature and current distributions in the HEMT structures operating under different conditions and topology. In comparison with 2-D FEM electrothermal simulations, the implemented 3-D thermal flow and distributed parameters of the HEMT provide more realistic simulation results. The advantages of the proposed method are the relative simplicity of implementation, the speed of simulation, and the capability of a full analysis of complex structures. A very good agreement between the simulation and the measurement confirms the validity of the proposed methodology.

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