Toward RF-linearity for planar local back- and top-gate SB-CNTFETs

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***Abstract*—RF-linearity at device level is becoming increasingly valuable for future communication systems. It has recently been reported that Schottky barrier (SB) CNTFETs offer high linearity under realistic conditions. In this paper, the potential of SB-CNTFETs for high RF-linearity is studied. The latter demands a compromise between excellent Schottky barrier control and high extrinsic high-frequency performance. Depending on the actual gate architecture, different design rules toward high RF-linearity for top- and local back-gate devices are elaborated.**

***Index Terms*—Carbon nanotube, Schottky barrier CNTFET, RF-linearity, semiclassical transport, Boltzmann transport equation, top-gate, local back-gate**

I. Introduction

Among the emerging FET technology options, CNTFETs have the highest transconductance at a reasonably low channel capacitance and, thus, let expect the best RF performance under loaded conditions typically encountered in RF circuits [1]. Compared to planar CMOS FETs, CNTFETs also offer a high potential for linearity which is becoming increasingly valuable for future communication systems, in which the inherent non-linearity (i.e. distortion) of incumbent devices limits spectral efficiency and battery lifetime.

Recently, realistic conditions for high linearity in SB-CNTFETs have been reported [2] based on a BTE-Poisson solver. It is claimed that high device linearity in terms of a bias-independent transconductance $g_\mathrm{m} = \mathrm{d}I_\mathrm{d}/\mathrm{d}V_\mathrm{gs}$ and bias-independent quantum capacitance $C_\mathrm{g} = \mathrm{d}Q_\mathrm{cnt}/\mathrm{d}V_\mathrm{gs}$ can be achieved within a certain bias region by *contact engineering* without meeting previously reported ideal conditions [3] such as ohmic contacts, single subband ballistic transport, and, in particular, operation within the quantum capacitance limit.

While in [2] the basic idea of contact engineering for tuning the device linearity has been reported, the impact of the device architecture on the RF-linearity is studied here. Recently first prototype devices showing an extrinsic GHz operating frequency for a top-gate [1] and a local back-gate device architecture have been reported. Both architectures are sketched in Fig. 1. The critical point for RF-linearity is to find a compromise between excellent Schottky barrier control and good high-frequency device performance. While the latter typically demands well separated metal contacts to minimize the parasitic capacitances between the contacts, an excellent barrier control, however, is only achievable if the gate is typically located nearby the Schottky barrier.

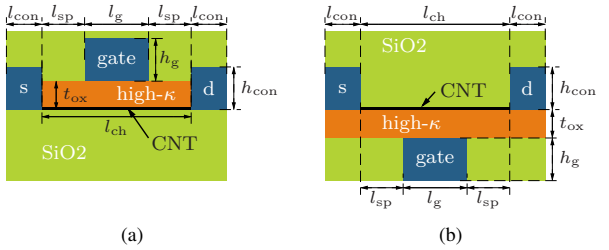

Figure 1. Cross section of a CNTFET with **(a)** a top-gate and **(b)** a planar local back-gate. The reference parameters for simulation are $l_\mathrm{ch} = 800\,\mathrm{nm}$, $l_\mathrm{con} = 50\,\mathrm{nm}$, $l_\mathrm{sp} = 200\,\mathrm{nm}$, $l_\mathrm{g} = 400\,\mathrm{nm}$, $h_\mathrm{con} = 20\,\mathrm{nm}$, $t_\mathrm{ox} = 20\,\mathrm{nm}$, $h_\mathrm{g} = 200\,\mathrm{nm}$.

II. Model

For the simulation studies shown here, a recently developed BTE-Poisson solver has been employed which enables a self-consistent solution of the semiclassical BTE and the 3D Poisson equation [2]. The one-dimensional BTE is solved along the CNT by the multi-particle Monte-Carlo method and takes into account acoustic and optical phonon scattering as described in [2]. The phenomenological contact model described in [4] inspired the contact model used for the BTE. It allows among others to consider tunneling through Schottky barriers by the WKB method. For the solution of the Poisson equation, the charge on the CNT is treated as a one-dimensional line charge. This simplification has to be revisited for thinner gate oxides in the future.

In case scattering is ignored, the BTE is solved deterministically which reduces the computational burden significantly. These ballistic BTE simulations can guide the identification of suitable contact geometries since scattering does not affect the linearity in terms of g_m for SB-CNTFETs [2]. Fine tuning of the contact is then pursued by means of non-ballistic BTE simulations, where scattering is considered.

The parasitic capacitance C'_par between the contacts is calculated based on the solution of the Laplace equation.

III. Device design

Ohmic-like and SB-CNTFETs differ in the mechanism how the current is controlled by the gate. While for ohmic-like

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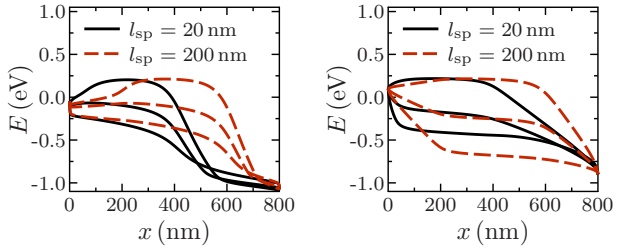

Figure 2. Conduction band profile for different $V_{\rm gs}$ and spacer lengths $l_{\rm sp}$ for **(a)** ohmic-like CNTFET and **(b)** SB-CNTFET.

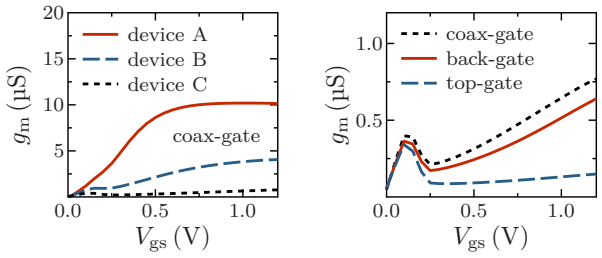

Figure 3. Transconductance for different devices with $l_{\rm sp} = 200\,$nm and $l_{\rm g} = 400\,$nm. **(a)** Different coaxial-gate structures: device A has completely filled spacers with an high-κ oxide, in device B the high-κ oxide height is reduced to 20 nm in the spacers, in device C the contact height is increased to 20 nm, **(b)** different gate architectures.

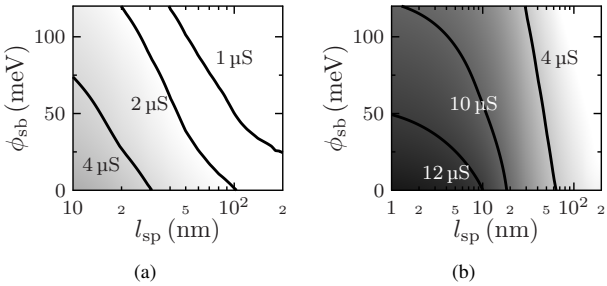

Figure 4. Transconductance $g_{\rm m,lin}$ at $V_{\rm gs} = 0.75\,$V and $V_{\rm ds} = 1\,$V for **(a)** a top-gate and **(b)** a local back-gate structure with $h_{\rm con} = 20\,$nm, $t_{\rm ox} = 20\,$nm, $h_{\rm g} = 200\,$nm and $l_{\rm g} = 800\,{\rm nm} - 2 \cdot l_{\rm sp}$ for different spacer lengths and Schottky barrier heights.

contacts the current is controlled by the potential barrier in the channel underneath the gate, the current in a SB-CNTFET is controlled by the height and the gate bias-dependent width of the Schottky barrier at the contacts. Depending on the contact type different design rules need to be employed for optimizing the device behavior. In Fig. 2 typical conduction band profiles for the two different contact types are shown. Optimizing the electrostatic control of the gate over the CNT close to the contacts (reducing the spacer length $l_{\rm sp}$) is crucial for the SB-CNTFET, to improve the control over the contact barrier, whereas for the ohmic-like CNTFET the important point is to control the barrier in the channel.

To improve the electrostatic gate control over the Schottky barrier of the injection contact (typically the source contact) one has various options: (*i*) decrease of the distance between the source and the gate contact by reducing the spacer length $l_{\rm sp}$ and the oxide thickness $t_{\rm ox}$, and (*ii*) enlargement of the gate contact height and the dielectric constant of the oxide between source and gate to increase the fringing fields to the tube. Another option is to decrease the source contact height in order to reduce the shielding of the electric fields from the gate by the source contact.

In [2] high RF-linearity in terms of bias-independent $g_{\rm m}$ and $C_{\rm g}$ has been reported for a coaxially gated 800 nm long SB-CNTFET with a Schottky barrier height of $\phi_{\rm sb} = 0.11\,$eV and 200 nm long spacers left and right to a 400 nm long gate contact. Despite these long spacers, an excellent Schottky barrier control has been achieved by reducing the source contact height to a minimum of 4 nm and filling the spacer regions with a high κ-oxide up to the top of the gate contact.

However, at the moment such small contact heights are difficult to fabricate and would increase the risk to not completely cover the CNTs which would be associated with a high contact resistance. In addition, coaxial-gate devices are technologically challenging. Local back- and top-gate structures are easier to fabricate albeit providing less gate control.

A good measure for the gate control is the transconductance $g_{\rm m}$ which is shown in Fig. 3 for different device architectures. The coaxial-gate device structure with completely filled 200 nm long spacers and 4 nm high contacts as reported in [2] is labeled in Fig. 3(a) as device A. Compared to this device, $g_{\rm m}$ drastically drops and becomes non-flat if the high-κ oxide height in the spacers is reduced to 20 nm (device B) and if the source contact height is additionally increased to 20 nm (device C). Fig. 3(b) compares $g_{\rm m}$ of the coaxial-gate device C with the transconductance of a top- and a local back-gate structure with the same dimensions. As expected, $g_{\rm m}$ is smaller for the latter two gate architectures.

Below it will be argued that by optimizing the Schottky barrier height as well as the spacer length, the contact height and the oxide thickness of the top-gate and local back-gate structures, a high transconductance as needed for high-frequency applications and a flat transconductance as needed for high RF-linearity can be obtained. Interestingly, the design rules for obtaining the best result are different for the two structures.

Fig. 4 shows the impact of the spacer length and the Schottky barrier height on $g_{\rm m,lin}$ (i.e. the transconductance $g_{\rm m}$ extracted in the region of highest linearity at $V_{\rm gs} = 0.75\,$V) for the top-gate and the local back-gate structure. It can be seen that in general a shorter spacer length and a lower Schottky barrier height increases $g_{\rm m,lin}$ because the gate control on the barrier is improved in both structures. However, $g_{\rm m,lin}$ of the local back-gate structure is more than two times larger than $g_{\rm m,lin}$ of the top-gate structure. This can be explained by the 20 nm high source contact, which shields the source Schottky barrier from the top-gate fringing fields.

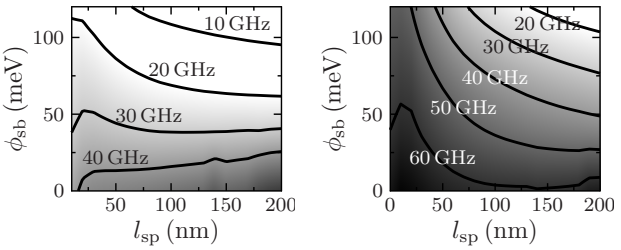

Figure 5. External transit frequency $f_{T,lin}$ in region of highest linearity at $V_{gs} = 0.75\,V$ and $V_{ds} = 1\,V$ for **(a)** a top-gate and **(b)** a local back-gate structure with $h_{con} = 20\,nm$, $t_{ox} = 20\,nm$, $h_g = 200\,nm$ and $l_g = 800\,nm - 2 \cdot l_{sp}$ for different spacer lengths and Schottky barrier heights.

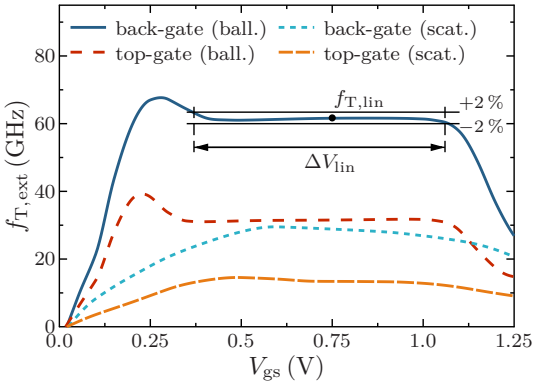

Figure 6. External transit frequency for optimized 800nm long top- and local back-gate SB-CNTFET. The device parameters are: $h_{con} = 20\,nm$, $t_{ox} = 20\,nm$, $h_g = 200\,nm$, for top-gate: $l_{sp} = 20\,nm$, $l_g = 760\,nm$, $\phi_{sb} = 40\,meV$ and for local back-gate: $l_{sp} = 40\,nm$, $l_g = 720\,nm$, $\phi_{sb} = 15\,meV$. The impact of scattering is also shown. In addition, the region of highest linearity is indicated.

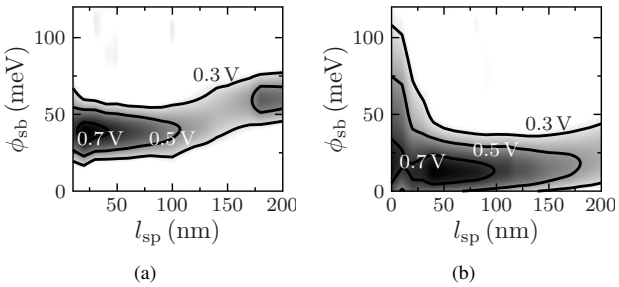

Figure 7. Width V_{lin} of linear region of $f_{T,ext}$ for **(a)** a top-gate and **(b)** a local back-gate structure with $h_{con} = 20\,nm$, $t_{ox} = 20\,nm$, $h_g = 200\,nm$ and $l_g = 800\,nm - 2 \cdot l_{sp}$ for different spacer lengths and Schottky barrier heights.

The external transit frequency $f_{T,ext}$ which combines the bias-dependence of the transconductance and gate capacitance of the channel as well as the parasitic capacitance between the contacts is an important figure of merit for high-frequency applications. For the calculation of $f_{T,ext}$, a multi-tube channel with a tube density ρ_t of $20\,\mu m^{-1}$ is assumed. Further, all tubes are semiconducting, identical, perfectly aligned and do not interact with each other. The calculation of $f_{T,ext}$ is than reduced to

$$f_{T,ext} = \frac{\rho_t g_m}{2\pi(\rho_t C_g + C'_{par})} \tag{1}$$

where g_m and C_g are the values for a single tube and C'_{par} is the total parasitic capacitance per unit width. A figure of merit for RF-linearity is the width ΔV_{lin} of the flat region, where $f_{T,ext}$ only deviates by 2 % from the value $f_{T,lin}$ extracted at $V_{gs} = 0.75\,V$ (see Fig. 6).

Fig. 5 shows $f_{T,lin}$ in dependence on l_{sp} and ϕ_{sb}. One can see that the local back-gate outperforms the top-gate structure where the finite source contact height shields the Schottky barrier at the source contact. For the same channel length of 800 nm, $f_{T,lin}$ can be further increased by about 30 % (not shown here) if the gate length is divided by two while at the same time the gate-source spacer is constant and the gate-drain spacer is increased.

Fig. 7 shows ΔV_{lin} in dependence on the spacer length and the Schottky barrier height. For the top-gate structure a region of high linearity (i. e. high value of ΔV_{lin}) can be identified for Schottky barrier heights of about 30 meV to 50 meV. The best result is achieved for $\phi_{sb} = 40\,meV$ and $l_{sp} = 20\,nm$. For these parameters ΔV_{lin} equals 0.72 V. In contrast, the local back-gate device has a sweet spot with $\Delta V_{lin} = 0.7\,V$ at $\phi_{sb} = 15\,meV$ and $l_{sp} = 40\,nm$. Comparing both architectures, the local back-gate architecture is less restrictive in terms of spacer lengths.

Fig. 8 shows the impact of the source contact height on various device performance indicators. Besides $f_{T,lin}$, ΔV_{lin} and $g_{m,lin}$, the parasitic capacitance C'_{par} is evaluated, too. Since a higher contact metal shields the fringing fields from the gate, the top-gate structure is more sensitive to changes of the contact height. Moreover, the dependence of the parasitic capacitance on h_{con} is larger for the top-gate structure since the overlap between the source contact and the gate is higher. However, for both device architectures the width ΔV_{lin} of the linear region, i. e. the RF-linearity, is hardly changed with the contact height.

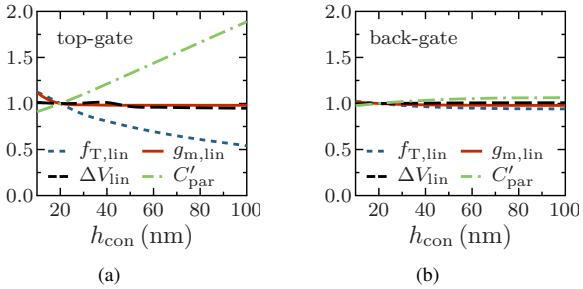

Figure 8. Impact of contact height on different RF-linearity performance indicators normalized to their values at $h_{con} = 20\,nm$ for **(a)** a top-gate and **(b)** a local back-gate structure.

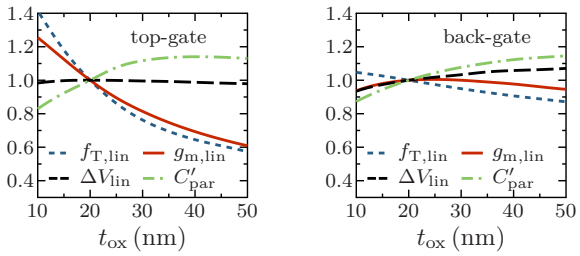

Figure 9. Impact of oxide thickness on different figures of merits normalized to the corresponding values at $t_{ox} = 20\,\text{nm}$ for **(a)** a top-gate and **(b)** a local back-gate structure.

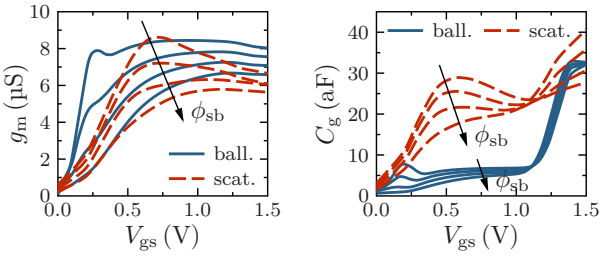

Figure 10. **(a)** g_m and **(b)** C_g for BTE simulations with and without scattering and different values of ϕ_{sb} for a local back-gate structure.

The gate height h_g has an almost negligible impact on the device characteristics for both device structures (not shown here). Since the gate is already close to the source contact, the enhancement of the gate fringing fields due to the higher gate is negligible.

Fig. 9 shows the impact of the oxide thickness on the device characteristics. Interestingly, for both device structures the parasitic capacitance becomes smaller for thin high-κ oxides and tiny gaps in between the contacts. Since the area of the high-κ oxide is also reduced, the effective dielectric constant of the oxide between the source and the gate, and, thus, the parasitic capacitance is decreased. In general, the local back-gate architecture is less sensitive to changes of the oxide height.

All the optimization results shown so far are obtained by means of the deterministic but ballistic BTE-Poisson solver. As already mentioned, the computational burden for this solver is very low, which allows to perform thousands of simulations as needed for device optimization. Moreover, the predicted bias dependence of the transconductance is in good agreement with non-ballistic BTE simulations where scattering is taken into account. Yet, the device performance in terms of $f_{T,ext}$ is typically overestimated. In Fig. 6 simulation results of the ballistic and the non-ballistic BTE-Poisson solver are compared for the top-gate and the local back-gate device architectures showing the highest RF-linearity. While non-ballistic transport leads to a 50 % decrease of $f_{T,ext}$, the good RF-linearity is maintained. Fig. 10 shows the related transconductance and gate capacitance for the optimized device architecture. The gate capacitance is increased, since scattering in the channel leads to an increase of the channel charge. By means of an additional optimization of the Schottky barrier height, the RF-linearity can be further improved (not shown here).

IV. Conclusion

In this paper design rules for obtaining highest RF-linearity with top-gate and local back-gate SB-CNTFETs are derived. It turned out that a small Schottky barrier height in the range of 10 meV to 50 meV and a spacer between the source contact and the gate of not more than 100 nm depending on the actual gate architecture are needed for providing highest RF-linearity. Different device performance indicators for RF-linearity are studied. Interestingly, the high parasitic capacitance due to the small spacer are overcompensated by the improved gate control over the Schottky barrier leading to a high transconductance. In addition, the study has shown that the local back-gate device architecture outperforms the top-gate architecture in terms of highest RF-linearity. Moreover, the local back-gate architecture is less restrictive in terms of contact heights and spacer lengths and is less sensitive to geometry variations.

V. Acknowledgements

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